SP02 to/from DT Interface Test

1. Hardware

- 9U VME Track Finder Crate
- Clock and Control Board (CCB), running under the TTC clock of 40.079 MHz (otherwise the SP02 PLL will not lock to the CCB clock!)
- Sector Processor (SP02)
- 9U VME Crate with Transition cage for 240 mm wide cards installed
- Transition Board (SP02_TB)
- 1 (or 2) 5 m cable assembly with angled and straight 68-pin SCSI-2 plugs
- 2 (or 4) 5 m cable assemblies with straight 68-pin SCSI-2 plugs
- Cross (Test) Board (SP02_CB)
- Other details on cable interconnections can be found at http://www.phys.ufl.edu/~uvarov/CERN/VG-CSC_DTR_04.pdf

2. Firmware

- Use sp_040620.evf and vm_fa_dd_040620.evf firmware files
- Details on SP02 VME and CCB interfaces can be found at http://www.phys.ufl.edu/~uvarov/CERN/LU-SP02_Backplane_Interfaces_040601.pdf
- References to Tables in the text below are references to tables in the above document

3. DT Interface Loopback Test

Test data injected into the LCT data-path from the FRONT_FPGA test FIFO pass Local LUT, DT LUT, SP02-to-TB backplane connector, and shows up at the output connectors of the Transition Board. External cable connections loop this data back to the Transition Board input connectors through a passive Cross Board. Test data goes through the TB-to-SP backplane connector and is registered in the SP_FPGA Spy FIFO. The above configuration allows validating only one pair of TB output connectors at a time, driving by either F1_FPGA or by F2_FPGA. F1_FPGA signals are with S1 (ME1A), S2 (ME1B) and S3 (ME1C) identifiers, and F2_FPGA signals are with S4 (ME1D), S5 (ME1E), and S6 (ME1F) identifiers.
The Table 2 test pattern is a so called “Running 1” test pattern, when logical one runs from LSB to MSB of the SP/M1/DAT_SFB first frame, making a 1-bit move on every RF clock. Then “Running 1” moves through the SP/M1/DAT_SFB second frame, the SP/M2/DAT_SFB first frame and finally through the SP/M2/DAT_SFB second frame. The DT-to-SP interface is specified only for 25 data lines plus clock, so 6 out of 32 bits in the SP/M1/DAT_SFB format are always zeros. There are 7 zeros in the SP/M2/DAT_SFB data format, since second muon clock is used to latch data in the barrel spy FIFO for both M1 and M2 muons.
Using the correspondence between FRONT_FPGA test FIFO data and DT interface signals set in Table 2, the user can generate his own sets of test data, if needed.

#	R/w	Register	Data	Comment
3.1				Make connections shown at http://www.phys.ufl.edu/~uvarov/CERN/LU-SP02_TB2_Setup.pdf
3.2	Write	VM/MA/CSR_FCC	0x0100	Put SP02 under the VME control
3.3	Write	FA/MA/CSR_FCC	0x0040	Prepare FA for the DT Loopback test
3.4	Write	SP/MA/CSR_FCC	0x0040	Prepare SP for the DT Loopback test
3.5	Write	F1/MA/DAT_DT and F2/MA/DAT_DT	From Table 1	Prepare DT LUTs for "Running 1" test
3.6	Write	FA/MA/ACT_XFR	0x0002	Reset FRONT_FPGA Test FIFOs
3.7	Write	FA/MX/DAT_TF	From Table 2	Prepare F1 and F2 Test FIFOs for "Running 1" test by loading 128 data words from Table 2 into M1, 128 words into M2 and 128 words into M3.
3.8	Write	FA/MA/CSR_TFC	0xA03F	Configure FRONT_FPGA Test FIFOs to inject data for 64BX
3.9	Write	SP/MA/CSR_TFC	0x0000	Disable SP_FPGA Test FIFOs
3.10	Write	VM/MA/CSR_SFC	0xA000	Enable spying on Inject Test Patterns
3.11	Write	SP/MA/CSR_SFC	0x004F	Configure SP_FPGA Spy FIFOs to record data for 80BX
3.12	Write	SP/MA/CSR_AFD	0x0000	Set Additional DT Data Delay to zero
3.13	Write	SP/MA/ACT_XFR	0x0004	Reset SP_FPGA Spy FIFOs
3.14	Write	VM/MA/ACT_FCC	0x00BC	Inject test pattern
3.15	Read	SP/M1/CSR_SFB and SP/M2/CSR_SFB	Expect 0x00A0	Check how many data words the Barrel Spy FIFO is holding
3.16	Read	SP/M1/DAT_SFB and SP/M2/DAT_SFB	Expect Data shown in last two columns of Table 2	Read back Spy FIFO data, number of readout words should be equal to the CSR_SFB data in the previous step

Table 1: DT LUT data for "Running 1" Loopback test.

Address Range (hex)	Addresses (dec)	Data
0x00000 - 0x07FFF	32768	0x0000
0x08000 - 0x0FFFF	32768	0x0001
0x10000 - 0x17FFF	32768	0x0002
0x18000 - 0x1FFFF	32768	0x0004
0x20000 - 0x27FFF	32768	0x0008
0x28000 - 0x2FFFF	32768	0x0010
0x30000 - 0x37FFF	32768	0x0020
0x38000 - 0x3FFFF	32768	0x0040

0x40000 – 0x47FFF	32768	0x0080
0x48000 – 0x4FFFF	32768	0x0100
0x50000 – 0x57FFF	32768	0x0200
0x58000 – 0x5FFFF	32768	0x0400
0x60000 – 0x67FFF	32768	0x0800
0x68000 – 0x7FFFF	98304	0x0000
Total	**524288**	

Table 2: FRONT_FPGA Test Data and SP_FPGA Spy Data for "Running 1" Loopback test.

BX #	FR #	FA/M1/ DAT_TF	DAT FIELD	FA/M2/ DAT_TF	DAT FIELD	FA/M3/ DAT_TF	DAT FIELD	TB OUT TEST POINT	TB IN TEST POINT	SP/M1/ DAT_SFB	SP/M2/ DAT_SFB
1	1	0		0		0		ME_S2 _PHI1	MB1A _Q0	0x0001	0
	2	0		0x2000	CSC_ID=2	0				0	0
2	1	0		0		0		ME_S2 _PHI2	MB1A _Q1	0x0002	0
	2	0		0x3000	CSC_ID=3	0				0	0
3	1	0		0		0		ME_S2 _PHI3	MB1A _Q2	0x0004	0
	2	0		0x4000	CSC_ID=4	0				0	0
4	1	0		0		0				0	0
	2	0		0		0				0	0
5	1	0x4000	Q=8	0		0		ME_S1 _ETA	MB1A _PHIB0	0x0010	0
	2	0		0		0				0	0
6	1	0x0800	Q=1	0		0		ME_S1 _Q0	MB1A _PHIB1	0x0020	0
	2	0		0		0				0	0
7	1	0x1000	Q=2	0		0		ME_S1 _Q1	MB1A _PHIB2	0x0040	0
	2	0		0		0				0	0
8	1	0x2000	Q=4	0		0		ME_S1 _Q2	MB1A _PHIB3	0x0080	0
	2	0		0		0				0	0
9	1	0		0		0		ME_S2 _PHI0	MB1A _PHIB4	0x0100	0
	2	0		0x1000	CSC_ID=1	0				0	0
10	1	0		0		0				0	0
	2	0		0		0				0	0
11	1	0		0		0				0	0
	2	0		0		0				0	0
12	1	0		0		0				0	0
	2	0		0		0				0	0
13	1	0		0		0		ME_S2 _PHI4	MB1A _FL	0x1000	0
	2	0		0x5000	CSC_ID=5	0				0	0
14	1	0		0		0		ME_S2 _PHI5	MB1A _CAL	0x2000	0
	2	0		0x6000	CSC_ID=6	0				0	0
15	1	0		0		0				0	0
	2	0		0		0				0	0
16	1	0		0		0				0	0
	2	0		0		0				0	0
17	1	0		0		0		ME_S1 _PHI0	MB1A _PHI0	0	0
	2	0x1000	CSC_ID=1	0		0				0x0001	0

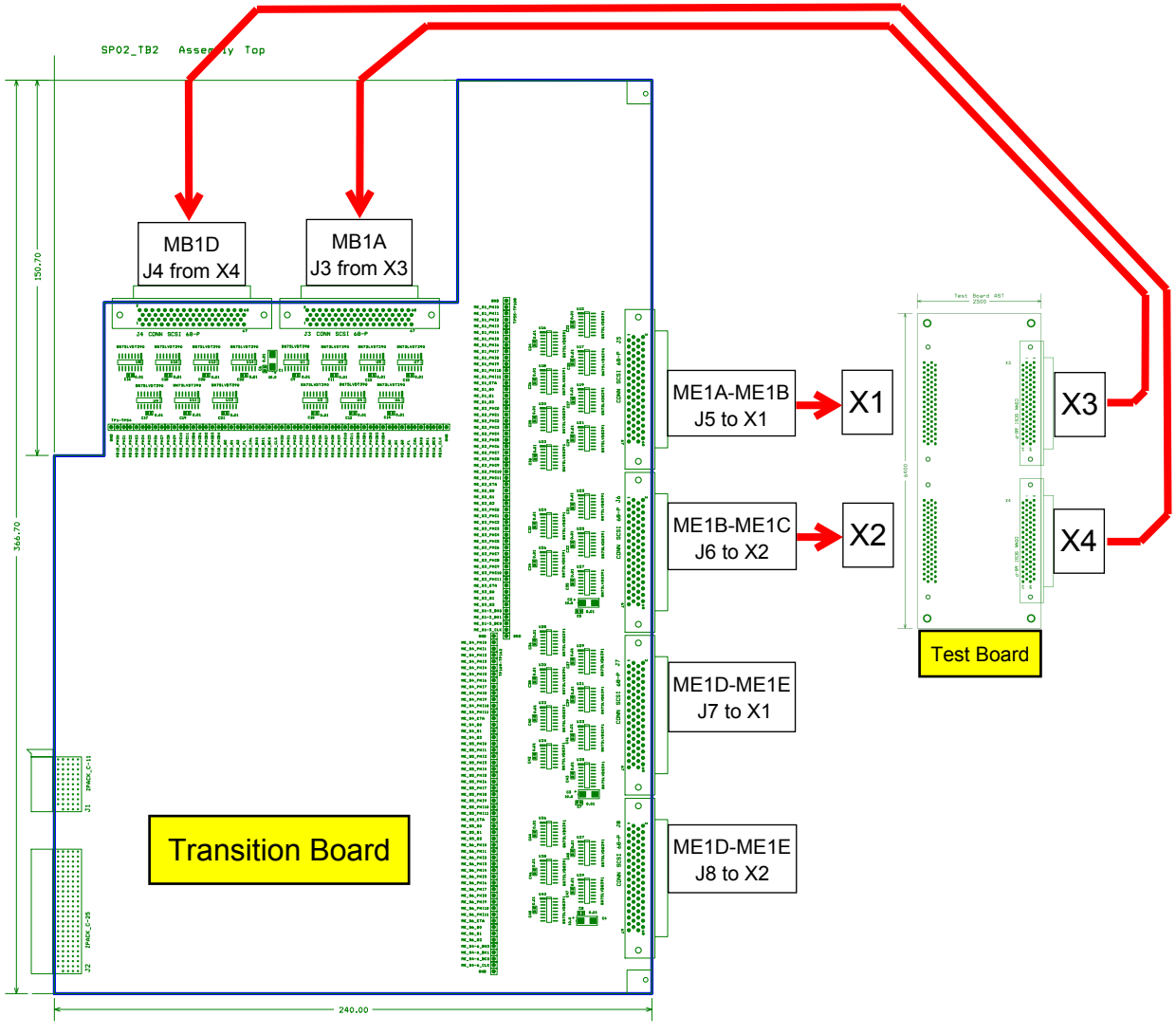
BX #	FR #	FA/M1/ DAT_TF	DAT FIELD	FA/M2/ DAT_TF	DAT FIELD	FA/M3/ DAT_TF	DAT FIELD	TB OUT TEST POINT	TB IN TEST POINT	SP/M1/ DAT_SFB	SP/M2/ DAT_SFB
18	1	0		0		0		ME_S1 _PHI1	MB1A _PHI1	0	0
	2	0x2000	CSC_ID=2	0		0				0x0002	0
19	1	0		0		0		ME_S1 _PHI2	MB1A _PHI2	0	0
	2	0x3000	CSC_ID=3	0		0				0x0004	0
20	1	0		0		0		ME_S1 _PHI3	MB1A _PHI3	0	0
	2	0x4000	CSC_ID=4	0		0				0x0008	0
21	1	0		0		0		ME_S1 _PHI4	MB1A _PHI4	0	0
	2	0x5000	CSC_ID=5	0		0				0x0010	0
22	1	0		0		0		ME_S1 _PHI5	MB1A _PHI5	0	0
	2	0x6000	CSC_ID=6	0		0				0x0020	0
23	1	0		0		0		ME_S1 _PHI6	MB1A _PHI6	0	0
	2	0x7000	CSC_ID=7	0		0				0x0040	0
24	1	0		0		0		ME_S1 _PHI7	MB1A _PHI7	0	0
	2	0x8000	CSC_ID=8	0		0				0x0080	0
25	1	0		0		0		ME_S1 _PHI8	MB1A _PHI8	0	0
	2	0x9000	CSC_ID=9	0		0				0x0100	0
26	1	0		0		0		ME_S1 _PHI9	MB1A _PHI9	0	0
	2	0xA000	CSC_ID=10	0		0				0x0200	0
27	1	0		0		0		ME_S1 _PHI10	MB1A _PHI10	0	0
	2	0xB000	CSC_ID=11	0		0				0x0400	0
28	1	0		0		0		ME_S1 _PHI11	MB1A _PHI11	0	0
	2	0xC000	CSC_ID=12	0		0				0x0800	0
29	1	0		0		0		ME_S2 _PHI6	MB1A _BX0	0	0
	2	0		0x7000	CSC_ID=7	0				0x1000	0
30	1	0		0		0		ME_S2 _PHI7	MB1A _BX1	0	0
	2	0		0x8000	CSC_ID=8	0				0x2000	0
31	1	0		0		0		ME_S2 _PHI8	MB1A _BC0	0	0
	2	0		0x9000	CSC_ID=9	0				0x4000	0
32	1	0		0		0		ME_S2 _PHI9	MB1A _CLK	0	0
	2	0		0xA000	CSC_ID=10	0				0x8000	0
33	1	0		0		0		ME_S3 _PHI11	MB1D _Q0	0	0x0001
	2	0		0		0xC000	CSC_ID=12			0	0
34	1	0		0		0x4000	Q=8	ME_S3 _ETA	MB1D _Q1	0	0x0002
	2	0		0		0				0	0
35	1	0		0		0x0800	Q=1	ME_S3 _Q0	MB1D _Q2	0	0x0004
	2	0		0		0				0	0
36	1	0		0		0				0	0
	2	0		0		0				0	0
37	1	0		0		0		ME_S3 _PHI6	MB1D _PHIB0	0	0x0010
	2	0		0		0x7000	CSC_ID=7			0	0

BX #	FR #	FA/M1/ DAT_TF	DAT FIELD	FA/M2/ DAT_TF	DAT FIELD	FA/M3/ DAT_TF	DAT FIELD	TB OUT TEST POINT	TB IN TEST POINT	SP/M1/ DAT_SFB	SP/M2/ DAT_SFB
38	1	0		0		0		ME_S3 _PHI7	MB1D _PHIB1	0	0x0020
	2	0		0		0x8000	CSC_ID=8			0	0
39	1	0		0		0		ME_S3 _PHI8	MB1D _PHIB2	0	0x0040
	2	0		0		0x9000	CSC_ID=9			0	0
40	1	0		0		0		ME_S3 _PHI9	MB1D _PHIB3	0	0x0080
	2	0		0		0xA000	CSC_ID=10			0	0
41	1	0		0		0		ME_S3 _PHI10	MB1D _PHIB4	0	0x0100
	2	0		0		0xB000	CSC_ID=11			0	0
42	1	0		0		0				0	0
	2	0		0		0				0	0
43	1	0		0		0				0	0
	2	0		0		0				0	0
44	1	0		0		0				0	0
	2	0		0		0				0	0
45	1	0		0		0x1000	Q=2	ME_S3 _Q1	MB1D _FL	0	0x1000
	2	0		0		0				0	0
46	1	0		0		0x2000	Q=4	ME_S3 _Q2	MB1D _CAL	0	0x2000
	2	0		0		0				0	0
47	1	0		0		0				0	0
	2	0		0		0				0	0
48	1	0		0		0				0	0
	2	0		0		0				0	0
49	1	0		0		0		ME_S2 _PHI10	MB1D _PHI0	0	0
	2	0		0xB000	CSC_ID=11	0				0	0x0001
50	1	0		0		0		ME_S2 _PHI11	MB1D _PHI1	0	0
	2	0		0xC000	CSC_ID=12	0				0	0x0002
51	1	0		0x4000	Q=8	0		ME_S2 _ETA	MB1D _PHI2	0	0
	2	0		0		0				0	0x0004
52	1	0		0x0800	Q=1	0		ME_S2 _Q0	MB1D _PHI3	0	0
	2	0		0		0				0	0x0008
53	1	0		0x1000	Q=2	0		ME_S2 _Q1	MB1D _PHI4	0	0
	2	0		0		0				0	0x0010
54	1	0		0x2000	Q=4	0		ME_S2 _Q2	MB1D _PHI5	0	0
	2	0		0		0				0	0x0020
55	1	0		0		0		ME_S3 _PHI0	MB1D _PHI6	0	0
	2	0		0		0x1000	CSC_ID=1			0	0x0040
56	1	0		0		0		ME_S3 _PHI1	MB1D _PHI7	0	0
	2	0		0		0x2000	CSC_ID=2			0	0x0080
57	1	0		0		0		ME_S3 _PHI2	MB1D _PHI8	0	0
	2	0		0		0x3000	CSC_ID=3			0	0x0100

BX #	FR #	FA/M1/ DAT_TF	DAT FIELD	FA/M2/ DAT_TF	DAT FIELD	FA/M3/ DAT_TF	DAT FIELD	TB OUT TEST POINT	TB IN TEST POINT	SP/M1/ DAT_SFB	SP/M2/ DAT_SFB
58	1	0		0		0		ME_S3 _PHI3	MB1D _PHI9	0	0
	2	0		0		0x4000	CSC_ID=4			0	0x0200
59	1	0		0		0		ME_S3 _PHI4	MB1D _PHI10	0	0
	2	0		0		0x5000	CSC_ID=5			0	0x0400
60	1	0		0		0		ME_S3 _PHI5	MB1D _PHI11	0	0
	2	0		0		0x6000	CSC_ID=6			0	0x0800
61	1	0		0		0		ME_S1-3 _BX0	MB1D _BX0	0	0
	2	0x0400	BX0	0		0				0	0x1000
62	1	0		0		0		ME_S1-3 _BX1	MB1D _BX1	0	0
	2	0x0200	BX1	0		0				0	0x2000
63	1	0		0		0		ME_S1-3 _BC0	MB1D _BC0	0	0
	2	0x0800	BC0	0		0				0	0x4000
64	1	0		0		0				0	0
	2	0		0		0				0	0

4. SP02 -> DT Test – Inject LCTs

A slight change in the SP02 configuration is required to generate LCT data.
- Local PHI LUT should be loaded with real mapping table
- Global DT LUT should be loaded with real mapping table
- SP/MA/CSR_FCC should be loaded with 0x0000
- depending on whether BX[0:1] and BC0 timing bits are required by DT logic along with the LCT data, FA/MA/CSR_FCC either may stay at 0x0040 or be reset to 0x0000.



Transition Board and Test Board Interconnect for a DT Interface Loopback Test