Update on SP02 Interfaces

by Victor Golovtsov & Lev Uvarov

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SP02 Interfaces

- VME Interface
- CCB Interface
- MPC Interface
  - ➔ MPC Data Validation
- DDU Interface
- FM Interface
  - ➔ Fast Monitoring Signals
- MS Interface
- DT Interface

VME Interface (P1/J1)

VME Interface

- ➔ A24D16 Slave
- ➔ AM = (0x39, 0x3A, ox3B, 0x3D, 0x3E, 0x3F)
- ➔ Near 64 Mbytes of addressable space

Internal Bus for Write/Read operations:

- ➔ D16 Bi-directional Data Lines
- ➔ Up to A10 Address Lines
- ➔ WR*/RD Control
- ➔ 8 x CE* Controls

Address space Considerations:

- ➔ GA address space [GA4:GA0] = 5 bits => [A23:A19] => Address space is limited to 512 Kbytes
- ➔ Address space for each chip is determined by a chip code, 8 bits for 8 chips => [A18:A11]
- ➔ Address space for registers inside each chip = 10 bits => [A10:A1]
- ➔ Addressing scheme allows board-wide and chip-wide broadcast writes to save time on LUT downloading

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	
GA #					Chip #								Register #										

CCB Interface

Signal	Lines	Direction	Type	Logic	Duration
Clock Bus					
CCB_CLOCK40	2	IN	Point-to-point	LVDS	40MHz
CCB_CLOCK40_ENABLE	1	IN	Bussed	GTLP	Pulse, n counts
Subtotal	**3**				
Fast Control Bus					
CCB_CMD [5..0]	6	IN	Bussed	GTLP	Level
CCB_EVCNTRES	1	IN	Bussed	GTLP	25ns
CCB_BCNTRES	1	IN	Bussed	GTLP	25ns
CCB_CMD_STROBE	1	IN	Bussed	GTLP	25ns
CCB_BC0	1	IN	Bussed	GTLP	25ns+ECL FP
CCB_L1ACCEPT	1	IN	Bussed	GTLP	25ns+ECL FP
CCB_DATA [7..0]	8	IN	Bussed	GTLP	Level
CCB_DATA_STROBE	1	IN	Bussed	GTLP	25ns
CCB_RESERVED [3..0]	4	IN	Bussed	GTLP	
CCB_READY	1	IN	Bussed	GTLP	Static level
Subtotal	**25**				
Reload Bus					
SP_HARD_RESET	1	IN	Bussed	GTLP	300ns
SP_CFG_DONE	1	OUT	Point-to-Point	GTLP	Level
Subtotal	**2**				
Reserved Lines					
SP_RESERVED [3..0]	4	OUT	Bussed	GTLP	**Local Trigger**
Subtotal	**4**				
Total	**34**				

Provisions to run in Local mode:

- **If a valid track found, SP generates a 25 ns signal (SP trigger) on the backplane bussed line;**
- **SP Triggers from different cards are wire ORed;**
- **CCB receives an OR of SP Triggers and, considering it as an L1A Local (L1AL), distributes it to other SPs and Peripheral crates.**
  (care should be taken in CCB to protect system from L1AL flood)

MPC Interface

		15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Frame	1	VP	Quality				CLCT Pattern #				Wire Group ID						
	2	CSC ID				BC0	BX0	SE	L/R	CLCT Pattern ID							

CLCT Pattern ID	**For high p_T patterns, the 8-bit half-strip ID is between 0 and 159. For low p_T patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or "key" layer of the chamber**
CLCT Pattern #	**The 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit.**
L/R	**The Left/Right bend bit indicates whether the track is heading towards lower or higher strip number.**
Quality	**The more hits the higher track Quality**
Wire Group ID	**The 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111.**
CSC ID	**The 4-bit CSC ID indicates the chamber # and runs from 1 to 9.**
VP	**The Valid Pattern flag indicates a valid LCT pattern has been found and information is being sent on the current clock cycle.**
SE	**Synchronization Error bit.**
BC0	**The Bunch Crossing Zero flag marks bunch zero data.**
BX0	**The least significant bit of Bunch Crossing Number (BXN ranges from 0 to 3563)**

MPC Data Validation

- Every turn Front FPGA compares BC0s coming along the data stream and BC0 coming from the CCB against FPGA's internal counter
  - If a mismatch is found all subsequent events are marked with SE=1 bit
- Every bunch crossing Front FPGA compares BX0 bit against the corresponding bits of its internal counter;
  - If a mismatch is found, Front FPGA sets SE=1
- Every bunch crossing Front FPGA checks an SE bit
  - If SE=1 found, then Front FPGA sets VP=0 (if not set already)
    - A VME control bit enables/disables the above option
- Front FPGA feeds Main FPGA with the modified data
  - For ME1, Front FPGA informs DT about the invalid pattern by setting Q=0
- Front FPGA stores modified data in the pipeline delay for readout upon L1A

Front FPGA counts every synch error. The counter content is available over VME Interface

DDU Interface

- **The DDU Interface mostly retains its status as of the December 2001 Trigger Meeting at UCLA , see http://www.phys.ufl.edu/~uvarov/tf_crate/interfaces.htm**
- **Provisions have been made to follow the 1(control)+15(data) bit convention used in the DMB-DDU interface to minimize DDU adjustments for the SP readout.**
- **DDU Payload at 100 kHz L1A rate is shown below**

	Units	Full Event	Zero-Suppressed Inputs		Header Only	Fast Monitoring Only
			Event	No Event		
Start-of-Frame	Words	2	2	2	2	2
Header	Words	8	8	8	8	
Output Block	Words	8	8	8		
Input Block 1	Words	40	8	4		
Input Block 2	Words	40	8	4		
End-of-Frame	Words	2	2	2	2	2
Total	Words	100	(36*2+28*10)/12 =29		12	4
Payload per SP	Words/sec	$10*10^6$	$2.9*10^6$		$1.2*10^6$	$0.4*10^6$
Payload per SP	Bytes/sec	$20*10^6$	$5.8*10^6$		$2.4*10^6$	$0.8*10^6$
Payload per DDU	Words/sec	$120*10^6$	$35*10^6$		$14*10^6$	$4.8*10^6$
Payload per DDU	Bytes/sec	$240*10^6$	$70*10^6$		$29*10^6$	$9.6*10^6$

FM Interface

SP02 uses the latest approach for collecting FM (Fast Monitoring) information:

- **Number of FM signals is reduce from 5 to 4 (ERR coded by RDY=BSY=1) combination**
- **FM signals are routed to RJ45 front panel jack**
- **Electrical standard – LVDS differential**

Fast Monitoring Signals - 1

- **RDY**
  - **There three cases to consider:**
    1. **Power-on condition**
    2. **Hard Reset condition**
    3. **L1 Reset condition**
    - **All FPGA configuration processes get completed (corresponding FPGA DONE signals became HIGH) (1,2)**
    - **All FPGA registers (1,2) and LUTs (1) have been loaded with the proper data and a VME-controlled READY trigger has been set to HIGH**
    - **MPC-SP synchronization procedure has been accomplished (Front FPGA has issued the /Alignment_FIFO_Read signal and data started flowing from the Front FPGAs) (1,2,3)**
    - **Input data has reached the output of the L1 Pipeline FIFO (may be redundant, since there is a "natural delay" in the RDY-L1A loop that the Data Delay FIFO is intended to compensate anyway) (1,2,3)**
  - **The SP02 RDY signal is a logical AND of the above conditions**

Fast Monitoring Signals - 2

- **BSY**
  - **SP is BUSY, when it is not READY**
- **WOF**
  - **The DDU Interface is responsible for L1A processing; so only it is capable to issue the WOF signal based on knowledge of the number of L1A received and the number of events transmitted to DDU.**
- **ERR**
  - **Input link failure – when optical receiver SD (signal detect) has gone**
- **OSY**
  - **Each Front FPGA issues an OSY signal if number of input stubs with SE bit set exceeds a preset threshold from a given opto-link. There are several reasons why input stub could be marked as an out of synch stub:**
    - **either input stub has been received with the SE bit already set,**
    - **or the BX0 bit does not match the expected values and the SE bit has been set by the Front FPGA logic.**
  - **The SP02 OSY signal is a logical OR of all Front FPGA and Main FPGA OSY signals.**

MS Interface

Two 32-bit Frames at 80 MHz each bunch crossing

Signal	Bits / μ	Bits / 3 μ (1 SP)	Description
Phi	5	15	Azimuth coordinate
Eta	5	15	Pseudorapidity
Rank *	7	21	5 bits p_T + 2 bits quality
Valid Charge	1	3	Charge assignment OK? (8^{th} bit from Rank LUT)
Halo Muon	1	3	Halo muon trigger
Charge	1	3	Muon sign
BX0	–	1	LSB of BXN
BC0	-	1	Bunch Crossing Zero flag
SE	–	1	Synch Error
Spare	–	1	
Total:	20	64	

Need to assign bits to frames, keeping in mind that Rank comes from the PT LUT later than the rest of the bits (up to MM preferences)

DT Interface

To be Presented by Darin Acosta