SP02 to MS Data Format

Revision 1.1

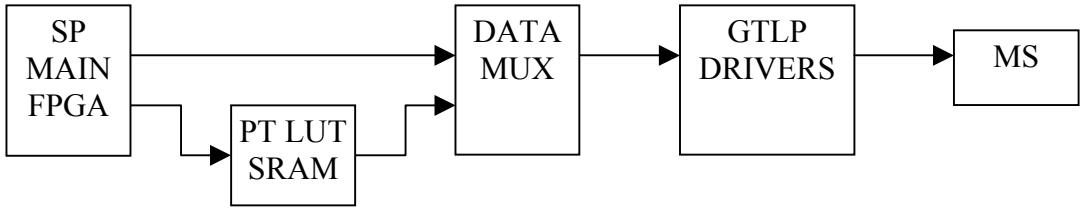

Figure 1 Dataflow inside the SP02

As Figure 1 and Table 1 show, the SP Main FPGA is a single source of all MS data, except RANK and VALID CHARGE bits coming from the PT LUT SRAM. For a timesaving reason PT LUT outputs are put in the second data frame.

Table 1 SP02 to MS Data Frames

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Frame	1	SE	BC0	ETA					PHI					ETA					PHI					ETA					PHI				
	2	SP	BX0	HL	C	VC	RANK							HL	C	VC	RANK							HL	C	VC	RANK						
Comment		Synch		MUON_3										MUON_2										MUON_1									

Here:

RANK ..... PT LUT output, 5 bits PT and 2 bits Quality
ETA ..... Pseudorapidity
PHI ..... Azimuth coordinates
VC ..... Valid Charge - 8th bit of PT LUT output
HL ..... Halo muon trigger
C ..... Charge or muon sign
BX0 ..... The least significant bit of Bunch Crossing Number (BXN ranges from 0 to 3563).
BC0 ..... The Bunch Crossing Zero flag marks bunch zero data.
Synch ..... Synchronization and spare bits
SE ..... Synchronization error (data out of synch)
SP ..... Spare bit