SP04 Production

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Muon Trigger Meeting
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SP02 Design & Test Summary

SP02 Status:

✓ **Three SP02 cards have been fabricated and tested**

✓ **All performed tests, including 2 Beam Tests at CERN were successful, although there were problems before**

✓ **Firmware supports all features implemented in hardware**

✓ **Firmware revisions are documented**

✓ **All three cards demonstrate identical behavior under the same test or/and work conditions -> robust design without marginal effects**

✓ **All major improvements for the SP04 production version were implemented in patches and tested with the SP02**

SP02 Presentations, Specifications, Interfaces, Data Formats, Firmware descriptions can be found at http://www.phys.ufl.edu/~uvarov/SP_design.htm

For the SP02 Design Files go to: http://www.phys.ufl.edu/~uvarov/SP02

SP02_SCH.pdf – complete SP02 schematic (without patches)

SP02_AST.pdf – SP02 board, assembly top

SP02_ASB.pdf – SP02 board, assembly bottom

1. New clocking solution based on the QPLL Daughter Board.

History: The Virtex II DCM clock, due to its digital nature, experiences discrete phase shifts of the order of 50 ps and can NOT be used as a TLK2501 reference clock. A QPLL substitute has been developed and the SP02 clocking solution has evolved from a single 40 MHz to a pair of 40/80 MHz clocks on-board. The SP04 version features a QPLL Daughter Board (QPLL DB), which can be driven by a 40/80 MHz backplane clock and outputs both 40 and 80 MHz clocks for the main board. The QPLL DB works under the VME_FPGA control.

2. New DDU Clocking.

History: The DDU link requires a separate clock of exactly 40.0000 MHz to match that of the DDU.

3. Flash Memory.

The SP04 features about 9 Million 16-bit words of downloadable SRAMs, as well as many other configurable registers. Keeping all SRAM and register data in a non-volatile 256 Mbit Flash Memory allows faster readiness for data-taking on power-up.

4. Unique Chip IDs.

Each FPGA on the SP04 boards has a 3-bit unique hardwired identifier.

5. Unique Board ID.

Each SP04 board has a unique 5-bit hardwired identifier.

6. Unique SP04 Mezzanine Card ID

Each SP04 Mezzanine Card has a unique 5-bit hardwired identifier.

7. **New implementation of multicast VME commands complies with the ANSI/VITA 23-1998 VME64 Extensions for Physics and Other Applications**

   Detail: The IACK* daisy-chain is used to allow Slaves to indicate that they have successfully latched the data. When the token arrives at the LAST Slave it may respond to the Master with DTACK* (if it, too, has accepted the data).
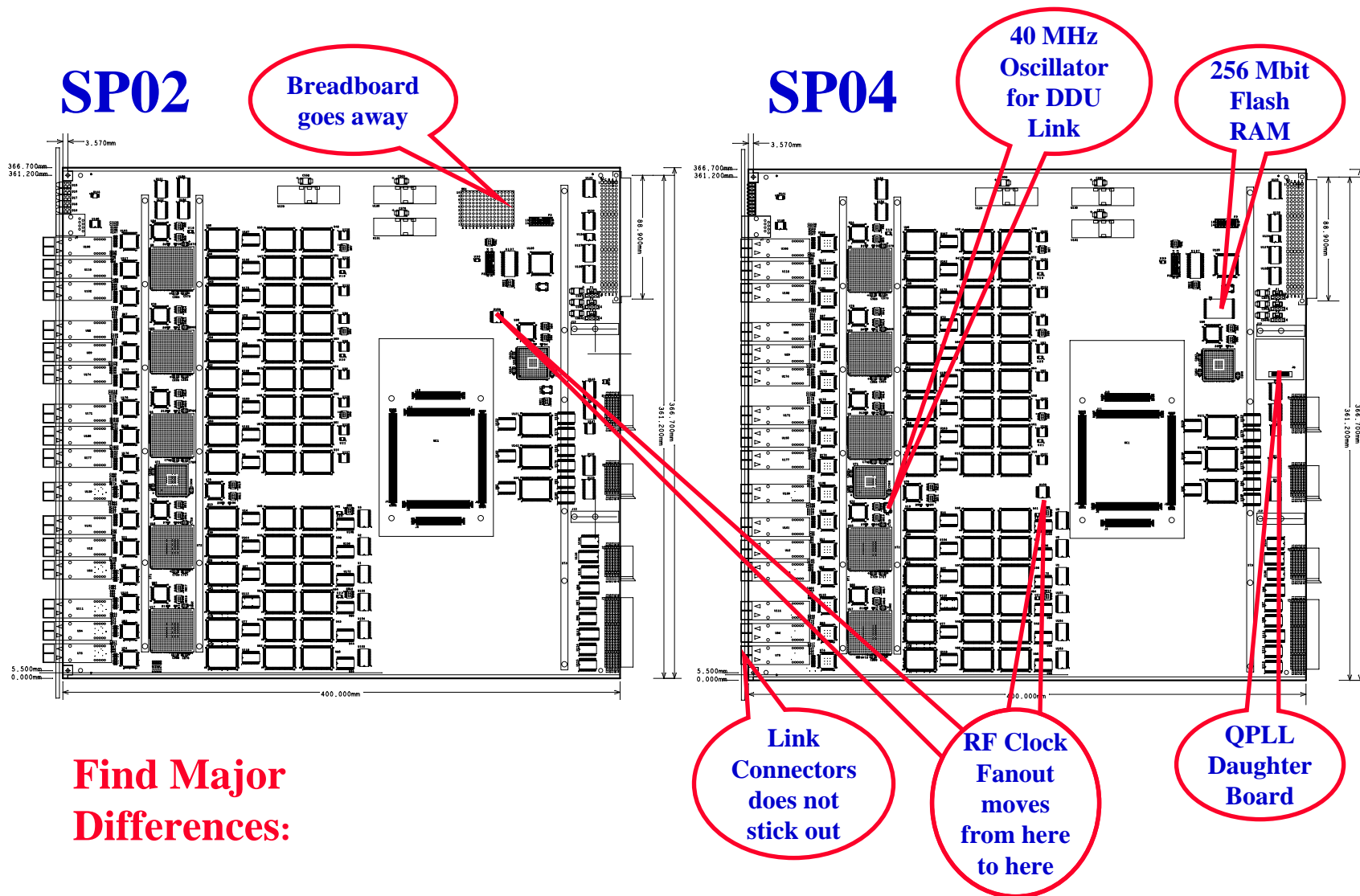
SP04 Minor Fixes & Improvements

1. **Replace Through-Hole JTAG Connectors for Xilinx Parallel Cable IV with SMT ones**

   Design improvement: Pins are short for a 93 mil board

2. **Fix signal mapping in the DT->SP interface and pin mapping for the VME connector**

   Fix typing errors: At the moment signals are remapped in the firmware or rewired in the hardware

3. **Add pull-ups to /OE (output enable) pins of the interface drivers / receivers / transceivers**

   Design improvement : Not critical, but it is useful to have controlled circuit state on power-up

4. **Terminate the winner bit lines from the MS and tie the V_{REF} pin of the GTLP transmitters to 1V**

   Design fix : oversight in the SP02 design

5. **Add ground hooks across the board**

   Design improvement : To facilitate board debugging with a scope, if needed

6. **Improve component placement**

   Design improvement : Put a Clock fanout chip in the center of the board, fix link transceivers placement

7. **Rename schematic nets to match naming convention for the FPGA Verilog code**

SP02

SP04

Breadboard goes away

40 MHz Oscillator for DDU Link

256 Mbit Flash RAM

Link Connectors does not stick out

RF Clock Fanout moves from here to here

QPLL Daughter Board

Find Major Differences:

September 5, 2004   **– SP04 Schematic ready**
September 12, 2004   **– SP04 Placement ready**
September 26, 2004   **– SP04 Layout ready (Conquest)**
September 26, 2004   **– SP04 Mezzanine Card Layout ready**
October 10, 2004   **– SP04 QPLL DB Layout ready**
October 24, 2004   **– SP04, SP04_MC and SP04_DB bare boards ready**
November 14, 2004   **– pilot samples of all boards stuffed**
December 5, 2004   **– SP04 pilot boards tested, start mass production**
January 15, 2005   **– all boards ready for testing**
March 1, 2005   **– all boards tested and ready for installation in CERN**

DDU Firmware – 2 months after the OSU DDU complete set of documents is available for UF plus 1 month for tests (conservative estimate)