SP-to-DDU Event Record Structure

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The SP readout format fully complies with the DMB-to-DDU Event Record structure, as described at http://www.physics.ohio-state.edu/~cms/ddu/ddu_pro.html, so mix of DMB and SP fibers are allowed to the same DDU module.

The format for the 16-bit SP output / DDU input is designed to easily interface with a 64-bit readout system through an S-LINK64 card. This requires that all data sent to the DDU be an integer multiple of 4 16-bit words for each event.

The highest bit of each SP 16-bit word is reserved as a special flag for DDU Code words, so only 15 bits are available for physics data. When the MSB of the 16-bit word is high, the 4 most significant bits indicate the DDU Code word. When the MSB is low, the other 15 bits are data.

The DDU Code words and the SP Data are always sent in groups of 4 to make a 64-bit word.

The Event Record has the following structure:

- Event Record Header
- Event Data
- Event Record Trailer

Both the Event Record Header and Event Record Trailer consist of two 64-bit words each. The Event Data can consist of any number of 64-bit words from 0 to 154, depending on the Event Record Configuration settings; see the DD/CSR_DFC register description for details.

Table below lists maximum Event Record sizes in 16-bit words for 1 to 8 Time Bins for different trigger boards.

Table 1: Event Record sizes for 0 to 8 TBIN values

TBIN	SP	DMB	ALCT-288	ALCT-384	ALCT-672	TMB	CFEB
0	16						
1	104		48	60	96		
2	192		84	108	180		
3	280		120	156	264		
4	368		156	204	348		
5	456		192	252	432		
6	544		228	300	516		
7	632		264	348	600		
8	-	1500	300	396	684	???	800

For SP, the maximum Event Record size is (22 + 4 = 26) 64-bit words per one TBIN plus 22 64-bit words per any additional TBIN. For TBIN=7, event size comes to 158/632 64/16-bit words in total, or 7.9 μsec readout time. The latter corresponds to a L1A rate of 126 kHz.

Event Record Header

The Event Record Header consists of 8 16-bit words, where the most significant hex digit is the DDU Code word 0x9 and 0xA. Green cells in Table 2 carry the SP-specific configuration settings; tan cells carry the SP-specific status; the content of all other cells complies with the DDU requirement.

Table 2: Event Record Header

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word
0x9				L1A [11:0]												HD1a
0x9				L1A [23:12]												HD1b
0x9				0												HD1c
0x9				L1A_BXN [11:0]												HD1d
0xA				0												HD2a
0xA				DD/CSR_BID [11:0]												HD2b
				SP_LARD [3:0]							SP_PARD [4:0]					
0xA				0				0	0	SP_OSY	FA_OSY	RDY	BSY	OSY	WOF	HD2c
0xA					DD/CSR_DFC [10:0]											HD2d
				SKIP	SPA	DTA	F5A	F4A	F3A	F2A	F1A	ZS	TBIN [2:0]			

Here:

- Spare cells are shown in yellow;
- L1A [23:0] – Event Number picked from a 24-bit Event Counter, located in the DDU_FPGA;
- L1A_BXN [11:0] – Event Bunch Crossing Number (L1A arrival time) picked from a 12-bit Bunch Counter, located in the DDU_FPGA and running at TTC timing;
- DD/CSR_BID [11:0] = DDU_FPGA / Board ID register:
  - SP_LADR [3:0] – SP Logical Address composed of:
    - SP_LADR[3] = MEZ = 0 (-Z) / 1 (+Z) – EMU side;
    - SP_LADR[2:0] = MES_ID [2:0] = 1…6 – EMU 60° Sector number;
  - SP_PADR [4:0] = 6…11, 16…21 – SP Physical Address (slot number);
- DD/CSR_DFC [11:0] = DDU_FPGA / DAQ FIFO (i.e. DDU Event Record) Configuration register:
  - F1A = 0 / 1 (default) – FRONT_FPGA Active bit. If the bit is set to 1, then the F1 is considered to be ACTIVE and is queried for CSC muon LCT(s) ME1a, ME1b, ME1c;
  - F2A = 0 / 1 (default) – FRONT_FPGA Active bit. If the bit is set to 1, then the F2 is considered to be ACTIVE and is queried for CSC muon LCT(s) ME1d, ME1e, ME1f;
  - F3A = 0 / 1 (default) – FRONT_FPGA Active bit. If the bit is set to 1, then the F3 is considered to be ACTIVE and is queried for CSC muon LCT(s) ME2a, ME2b, ME2c;
  - F4A = 0 / 1 (default) – FRONT_FPGA Active bit. If the bit is set to 1, then the F4 is considered to be ACTIVE and is queried for CSC muon LCT(s) ME3a, ME3b, ME3c;
  - F5A = 0 / 1 (default) – FRONT_FPGA Active bit. If the bit is set to 1, then the F5 is considered to be ACTIVE and is queried for CSC muon LCT(s) ME4a, ME4b, ME4c;

- DTA = 0 / 1 (default) – Drift Tube Active. If the bit is set to 1, then the Drift Tube interface is considered to be ACTIVE and the SP_FPGA is queried for DT muon Stub(s) MB1a, MB1d;
- SPA = 0 / 1 (default) – Sector Processor Active. If the bit is set to 1, then the Sector Processor output is considered to be ACTIVE and the SP_FPGA is queried for SP muon Track(s) SP1, SP2, SP3;
- ZS = 0 / 1 (default) – Zero Suppression bit. If set to 1, then only valid LCT(s), Stub(s) and Track(s) are collected;
- TBIN [2:0] = 0…7 (default = 4) – DDU_FPGA collects data from 0…7 Time Bins (bunch crossings).SP_LADR [3:0] – SP Logical Address composed of:

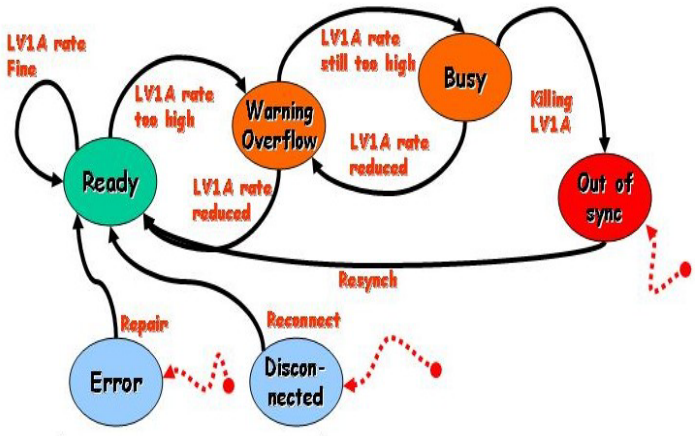
– SP_OSY – the SP_FPGA local L1A number does not match the DDU_FPGA L1A number shown in the Event Header, words {HD1b, HD1a}. This is an Out-of-Synch condition between event data fragments, which may (if it is persistent) or may not (if it is occasional) require a L1 Reset signal.

– FA_OSY – the FRONT_FPGA local L1A number from one or more FRONT_FPGA chips does not match the DDU_FPGA L1A number shown in the Event Header, words {HD1b, HD1a}. This is an Out-of-Synch condition between data fragments, which may (if it is persistent) or may not (if it is occasional) require a L1 Reset signal.

– RDY, BSY, OSY, WOF – FMM signals Ready, Busy, Out-of-SYnch, Warning OverFlow.

– SKIP – if the SKIP bit is set to 1, then the Event Data is skipped for the current event, and the event shrinks to the Event Record Header and Event Record Trailer only, as if the TBIN equals 0 (although actually not), see details on the L1A Finite State Machine (FSM) below.

All FMM signals carry signal values at the time the DDU_FPGA composes the current Event Record Header, and NOT at the time L1A has been received. This is a copy of signals the DDU_FPGA sends over to the VME_FPGA. The VME_FPGA collects same signals from all the FRONT_FPGAs and the SP_FPGA and finally generates the SP FMM output. According to http://cmsdoc.cern.ch/cms/TRIDAS/horizontal/RUWG/DAQ_IF_guide/DAQ_IF_guide.html the L1A FSM may be in one of the following states:



LF Levels	
UP	DOWN
LF_FULL	LF_FULL
---	---
LF_OSY_HI	---
---	---
LF_BSY_HI	---
---	---
---	LF_BSY_LO
---	---
LF_WOF_HI	---
---	---
---	LF_WOF_LO
---	---
---	---
---	---
LF_EMPTY	LF_EMPTY

- 1000 = RDY – Ready => L1A rate is fine.
  The Event Record Structure is per DD/CSR_DFC.
- 0001 = WOF – Warning OverFlow
  => L1A rate is too high.
  Event queue in the LF has reached the LF_WOF_HI level.
  If, despite the WOF condition reported, the event queue keeps growing and reaches the LF_BSY_LO level, then for every event above the LF_BSY_LO level the SKIP bit will be set. The SKIP bit acts as a local backup for trigger throttling system. It can not actually throttle down the L1A rate; instead it shortens the readout time in order to prevent the FSM from getting into the BSY state.
- 0100 = BSY – Busy => L1A rate is still very high.
  Event queue in the LF has reached the LF_BSY_HI level. To prevent the LF from overflow, some of the following events will be flushed, until the event queue drops to the LF_BSY_LO level and the FSM switches back to WOF state.
- 0010 = OSY – Out-of-Synch.
  May be caused by:
  - L1A very high rate persists and LF overflow is imminent, despite all efforts to throttle it down via FMM and locally. Given the above measures for preventing the LF overflow this should never happen.
  - FA_OSY and SP_OSY bits are set for a number of consecutive Event Records. Apparently, something goes wrong and a L1 Reset is required.

Event Data

The Event Data consists of the data blocks repeated TBIN times (0 to 7):

– Data Block
– ----------
– ----------
– Data Block

Data Block

The Data Block content is determined by the Event Configuration Word (DD/CSR_DFC) and the proper data and consists of 1 to 88 16-bit words, going in the following order:

– 8 16-bit words for a Data Block Header;
– 4 16-bit ME Data words per each CSC EMU MEx LCT;
– 4 16-bit MB Data words per each DT Barrel MBy Stub;
– 4 16-bit SP Data words per SPz Track.

Here:

- MEx is one of the following muon LCTs:
  ME1a | ME1b | ME1c => set Active for readout with F1A;
  ME1d | ME1e | ME1f => set Active for readout with F2A;
  ME2a | ME2b | ME2c => set Active for readout with F3A;
  ME3a | ME3b | ME3c => set Active for readout with F4A;
  ME4a | ME4b | ME4c => set Active for readout with F5A.
  Muon order always goes from ME1a to ME4c.
- MBy is one of the following muon Stubs:
  MB1a | MB1d => set Active for readout with DTA.
  Muon order always goes from MB1a to MB1d.
- SPz is one of the 3 output Tracks:
  SP1, SP2, SP3 => set Active for readout with SPA.
  Track order always goes from SP1 to SP3.

Data Block Header

The Data Block Header consists of 8 16-bit words BH1a thru BH1d and BH2a thru BH2d and is present for every time bin.

Words BH1a and BH1b provide the contents of a Data Block followed:

MEx Data is present, if:

1. **The corresponding FnA bit is set to 1 (ACTIVE)**
   AND
2. **Either (ZS = 0) OR (ZS = 1 AND VPx = 1).**

MBy Data is present, if:

1. **The DTA bit is set to 1 (ACTIVE)**
   AND
2. **Either (ZS = 0) OR (ZS = 1 AND QBy = 1).**

SPz Data is present if:

1. **The SPA bit is set to 1 (ACTIVE)**
   AND
2. **Either (ZS = 0) OR (ZS = 1 AND MODEz > 0).**

Table 3: Data Block Header

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word
	F5			F4				F3				F2				F1		
0	VP4c	VP4b	VP4a	VP3c	VP3b	VP3a	VP2c	VP2b	VP2a	VP1f	VP1e	VP1d	VP1c	VP1b	VP1a	BH1a
0	0	VQd	VQa	MODE3				MODE2				MODE1				BH1b
0	SE4c	SE4b	SE4a	SE3c	SE3b	SE3a	SE2c	SE2b	SE2a	SE1f	SE1e	SE1d	SE1c	SE1b	SE1a	BH1c
0	SM4c	SM4b	SM4a	SM3c	SM3b	SM3a	SM2c	SM2b	SM2a	SM1f	SM1e	SM1d	SM1c	SM1b	SM1a	BH1d
0	AF4c	AF4b	AF4a	AF3c	AF3b	AF3a	AF2c	AF2b	AF2a	AF1f	AF1e	AF1d	AF1c	AF1b	AF1a	BH2a
0	BX4c	BX4b	BX4a	BX3c	BX3b	BX3a	BX2c	BX2b	BX2a	BX1f	BX1e	BX1d	BX1c	BX1b	BX1a	BH2b
0	0	AFBd	AFBa	0	0	PT_LUT [1:0]		SP/M[PT_LUT]/DAT_PT [7:0]								BH2c
0	0	BXBd	BXBa	0	0	0	0	SP/M[PT_LUT]/DAT_PT [15:8]								BH2d

Here:

– Spare cells are shown in yellow;
– VPx – Valid Pattern bits for 15 MEx LCTs, as they have been received;
– VQy – Valid Quality (Q > 0) bits for 2 MBy Stubs;

- MODEz – Mode values for 3 SP output Tracks ;
- SEx – Synch Error bits for 15 MEx LCTs, as they have been received;
- SMx – Modified Synch Error bits for 15 MEx LCTs; modification performed into the FRONT_FPGA and based on the Optical Link status, Alignment FIFO status and Bunch Crossing Counter status;
- AFx – Alignment FIFO status bits for 15 MEx Links. AFx bit is reset to 0 on L1RES and is set to 1, if the Alignment FIFO word count slips any time after L1RES. So, this word monitors link's "locked to the received data stream" status;
- BXx – Bunch Crossing Counter status bits for 15 MEx links; BXx bit is set to 1, when link's BC0 timing mark arrives early or late, and it is reset back to 0, if any next BC0 timing mark arrives in time. So, this bit monitors the ALCT/TMB/MPC timing and post-marks irregular orbits;
- AFBy – Alignment FIFO status bits for 2 MBy data streams; AFBy bit is reset to 0 on L1RES and is set to 1, if the Alignment FIFO word count slips any time after L1RES. So, these bits monitor the data stream clocking status;
- BXy – Bunch Crossing Counter status bits 2 MBy data streams; BXy bit is set to 1, when link's BC0 timing mark arrives early or late, and it is reset back to 0, if any next BC0 timing mark arrives in time. So, this bit monitors the DT timing and post-marks irregular orbits;
- PT_LUT[1:0] – PT LUT number is a copy of the SP/CSR_SFC[13:12], and is used to monitor the PT LUT outputs:
  - PT_LUT = 0 => no PT_LUT is monitored;
  - PT_LUT = 1 => PT_LUT1 is monitored;
  - PT_LUT = 2 => PT_LUT2 is monitored;
  - PT_LUT = 3 => PT_LUT3 is monitored.
- SP/M[PT_LUT]/DAT_PT[15:0] – PT LUT data, if PT_LUT > 0.

ME Data Record

The Data Record for each MEx consists of 4 16-bit words: MEa, MEb, MEc, MEd.

The MEa word carries Frame1 of LCT data, as it has been received from MPC with rearranged frame fields for better readability in hex and VPx bit omitted, since it has already been extracted to the Data Block Header BH1a.

The MEb word carries Frame2 of LCT data, as it has been received from MPC with rearranged frame fields for better readability in hex and SEx bit omitted, since it has already been extracted to the Data Block Header BH1c.

Table 4: MEx Data Record

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word
0	Wire Group ID [6:0]							Quality [3:0]				CLCT Pattern # [3:0]				MEa
0	BC0	BXN0	L/R	CSC ID [3:0]				CLCT Pattern ID [7:0]								MEb
0	AFFF	RDV1	RER1	ME_BXN [11:0]												MEc
0	AFEF	RDV2	RER2	EPC [3:0]				MPC_LINK_ID [7:0]								MEd
								MPC # [5:0]						LINK # [1:0]		

Here:

- CLCT Pattern # [3:0] – 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit;
- Quality [3:0] – the more hits the higher LCT Quality;
- Wire Group ID [6:0] – 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111;
- CLCT Pattern ID [7:0] – For high pT patterns, the 8-bit half-strip ID is between 0 and 159. For low pT patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or "key" layer of the chamber;
- CSC ID [3:0] – 4-bit CSC ID indicates the chamber # and runs from 1 to 9;
- L/R – Left/Right bend bit indicates whether the track is heading towards lower or higher strip number;
- BXN0 – Bunch Crossing Number least significant bit;
- BC0 – Bunch Crossing Zero flag marks that next BXN = 0;
- ME_BXN [11:0] – LCT Bunch Crossing Number (LCT arrival time) picked from a local 12-bit Bunch Counter and running at link timing;
- MPC_LINK_ID [7:0] - MPC Link Identifier consists of:
  - LINK # [1:0] = 0 (default), 1, 2, 3 – MPC Link number;
  - MPC # [5:0] = 0 (default)…63 – MPC Crate number.

  The MPC_LINK_ID is reported by MPC on every L1 Reset.
- { RDV, RER} [1:2] = {Receive Data Valid, Receive Error} – Receive Status Signals; Receive Normal Data Character combination validates frame1 and frame2 of the LCT data:
  - {RDV, RER} = {0,0} – Receive Idle Character;
  - {RDV, RER} = {0,1} – Receive Carrier Extend;
  - {RDV, RER} = {1,0} – Receive Normal Data Character;
  - {RDV, RER} = {1,1} – Receive Error Propagation;
- AFFF – Alignment FIFO Full Flag, should be 0, if AF has been initialized successfully by L1RES;
- AFEF – Alignment FIFO Empty Flag, should be 0, if AF has been initialized successfully by L1RES;
- EPC [3:0] – the Error Propagation counter at the Alignment FIFO output accumulates the "Receive Error Propagation" occurrences since last L1RES.

MB Data Record

The Data Record for each MBy consists of 4 16-bit words: MBa, MBb, MBc, MBd.

The MBa and MBb words carry MBy Stub data, as it has been received from the DT Track Finder. The MBa / MBb data format matches the 2-frame SP/DAT_TFB and SP/DAT_SFB formats with the exception of VQ bit for the latter.

Table 5: MBy Data Record

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word
0	0	CAL	FLAG	0	0	0	PHI BEND [4:0]					0	Q [2:0]			MBa
0	BC0	BXN0	BXN1	PHI [11:0]												MBb
0	0			MB_BXN [11:0]												MBc
0	0			0				0				0				MBd

Here:

- Spare cells are shown in yellow;
- Q [2:0] = 0…7 – Muon Quality; For valid data Quality is always > 0;
- PHI BEND {4:0] – Phi Bend angle;
- PHI [11:0] – Azimuth Coordinate;
- FLAG, if 1 then it is a second muon from previous bunch crossing;
- CAL – a MBy special mode flag;
- BXN0, BXN1 – two LSBs of the MBy Bunch Crossing Number;
- BC0 – Bunch crossing zero timing mark.
- MB_BXN [11:0] – MBy Stub Bunch Crossing Number (Stub arrival time) picked from a local 12-bit Bunch Counter and running at data stream timing;

SP Data Record

The Data Record for each SPz consists of 4 16-bit words: SPa, SPb, SPc, SPd.

The SPa and SPb words carry the output track data. The data format matches the SP/DAT_TF and SP/DAT_SF formats with the following exceptions:

- The RSV bit omitted;
- The MODE bits omitted, since they have been extracted to the block header earlier;
- The BC0 and BXN0 timing bits added.

Table 6: SPz Data Record

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word
0	SE	HL	ETA [4:0]					CHRG	FR	SIGN	PHI [4:0]					SPa
0	BC0	BXN0	0	D23_PHI [3:0]				D12_PHI [7:0]								SPb
0	MS_ID [2:0]			MB_ID [2:0]			ME4_ID [1:0]		ME3_ID [1:0]		ME2_ID [1:0]		ME1_ID [2:0]			SPc
0	MB_TBIN [2:0]			ME4_TBIN [2:0]			ME3_TBIN [2:0]			ME2_TBIN [2:0]			ME1_TBIN [2:0]			SPd

Here:

- PHI [4:0] is the Azimuth Coordinate;
- ETA [4:0] is the Pseudo rapidity, the Eta [4:1] is a part of the PT LUT address;
- SIGN – Delta Phi Sign bit is a part of the PT LUT address;
- FR – Front/Rear bit;
- CHRG – Muon Charge or Sign bit;

- HL – Halo bit;
- SE – Synchronization Error bit is an OR (or some other Boolean function => to be determined) of Modified Synch Error bits for 15 MEx LCTs and similar bits for 2 MBy Stubs;
- BXN0 – an OR (or some other Boolean function => to be determined) of same signals received with ME LCTs and MB stubs, and passed to the MS;
- BC0 – an OR (or some other Boolean function => to be determined) of same signals received with ME LCTs and MB stubs and passed to the MS;
- D12_PHI [7:0] is a part of the PT LUT address;
- D23_PHI [3:0] is a part of the PT LUT address;
- MS_ID [3:1] = Muon Sorter Winner bit positional code;
- ME1_ID [2:0], ME2_ID [1:0], ME3_ID [1:0], ME4_ID [1:0], MB_ID [2:0] – track stubs used to build up the track => see Table 7 for the ID interpretation.
- ME1_TBIN [2:0], ME2_TBIN [2:0], ME3_TBIN [2:0], ME4_TBIN [2:0], MB_TBIN [2:0] – Time Bins of the above track stubs used to build up a track.

Table 7: Spy FIFO to Muon ID Correspondence

Muon ID	Muon #	Look for track stub into the Spy FIFO:
ME1_ID = 1	ME1a	SP/DAT_SF1/M1
ME1_ID = 2	ME1b	SP/DAT_SF1/M2
ME1_ID = 3	ME1c	SP/DAT_SF1/M3
ME1_ID = 4	ME1d	SP/DAT_SF2/M1
ME1_ID = 5	ME1e	SP/DAT_SF2/M2
ME1_ID = 6	ME1f	SP/DAT_SF2/M3
ME2_ID = 1	ME2a	SP/DAT_SF3/M1
ME2_ID = 2	ME2b	SP/DAT_SF3/M2
ME2_ID = 3	ME2c	SP/DAT_SF3/M3
ME3_ID = 1	ME3a	SP/DAT_SF4/M1
ME3_ID = 2	ME3b	SP/DAT_SF4/M2
ME3_ID = 3	ME3c	SP/DAT_SF4/M3
ME4_ID = 1	ME4a	SP/DAT_SF5/M1
ME4_ID = 2	ME4b	SP/DAT_SF5/M2
ME4_ID = 3	ME4c	SP/DAT_SF5/M3
MB_ID = 1	MB1a	SP/DAT_SFB/M1
MB_ID = 2	MB1a	SP/DAT_SFB/M1 – next bx
MB_ID = 3	MB1d	SP/DAT_SFB/M2
MB_ID = 4	MB1d	SP/DAT_SFB/M2 – next bx

Event Record Trailer

The Event Record Trailer consists of 8 16-bit words, where the most significant hex digit is the DDU Code word 0xF and 0xE. Green cells in Table 8 show SP-specific configuration settings, tan cells carry the SP-specific status, yellow cells are spare, and the content of all other cells is per DDU requirements.

Table 8: Event Record Trailer

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word
0xF				DD/CSR_LF [3:0]				L1A [7:0]								TR1a
0xF				DD/CSR_LF [7:4]				LFFF	0x7			0xF				TR1b
0xF				0	0	0	0	SP/CSR_SID [15:8]								TR1c
								YY [3:0]				MM [3:0]				
0xF				SP/CSR_SCC [11:0]												TR1d
0xE				0							SP/CSR_SID [4:0]					TR2a
											DD [4:0]					
0xE				DD/CSR_BID [11:0]												TR2b
0xE				LP	CRC-22 [10:0]											TR2c
0xE				HP	CRC-22 [21:11]											TR2d

Here:

- L1A [7:0] – Event Number, lower byte, same as HD1a [7:0];
- DD/CSR_LF [7:0] = 0…255 – DDU_FPGA L1A FIFO word count. Shows the L1A queue size at the moment of transmitting TR1a;
- LFFF = DD/CSR_LF[15] – L1A FIFO Full Flag (LF word count = 256) at the moment of transmitting TR1a;
- SP/CSR_SID [15:8] = {YY [3:0], MM [3:0]} – SP Core Identifier Register: Year and Month of the Core release date;
- SP/CSR_SID [4:0] = DD [4:0] – SP Core Identifier Register: Day of the Core release date;
- SP/CSR_SCC [11:0] – SP Core Configuration Register;
- TR2b == HD2b;
- LP – Low Parity => Even Parity bit for CRC-22 [10:0]
- HP – High Parity => Even Parity bit for CRC-22 [21:11]
- CRC-22 [21:0] – the last 4 Event Record Trailer words are not included in the CRC

History

Version DRAFT – March 20, 2006 – initial release

Version DRAFT 2.0 – April 05, 2006

1. In Table 2 references to configuration registers added
2. HD2b fields notation changed
3. HD2c changed completely, explanation of FMM state per Atilla's document added
4. AFFF and AFEF added to Table 4
5. DD/CSR_LF added to TR1a, TR1b and TR1c in Table 8

Version DRAFT 2.1 – April 10, 2006

1. TR2c and TR2d words in Table 8 shared by Parity bits and CRC-22.

Version DRAFT 2.2 – April 10, 2006

1. Swapped Quality bits and CLCT Pattern # bits in Table 4
2. Shuffled bits in Table 6 to match layout with SP/DAT_TF and SP/DAT_SF

Version DRAFT 2.3 – April 13, 2006

1. Bits BC0, BX0 in Table 6 moved bit left to match same bit positions in Table 4 and Table 5
2. Bits BX0, BX1 swapped in Table 5 to match same bit positions in Table 4 and Table 6

Version DRAFT 3.0 – April 19, 2006

1. Consolidated ME and MB/TF Data Blocks into a single Data Block.
2. Changed all tables.

Version 4.0 – April 25, 2006

1. First non-draft version

Version 4.1 – May 10, 2006

1. Style edits