SP Backplane Interfaces

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060701_SP04_ISE52_Chain1 and 060701_SP04_ISE52_Chaine0_Q34C.svf
configuration files.

CCB Interface

The CCB interface provides the SP with timing and trigger control signals distributed by the Clock and Control Board (CCB) over the backplane [i]. The backplane counts as many as 34 signal lines coming in and going out of the SP. Table 1 arranges backplane signals into four Groups. All GTLP lines are active LOW (negative bus logic).

Table 1: SP CCB Interface Signals.

Signal	Lines	Direction	Type	Logic	Duration	Usage
Clock Group						
CCB_CLK	2	IN	Point-to-point	LVDS	40MHz	Used
CCB_CLK_EN	1	IN	Bussed	GTLP	Pulse, n counts	Not used
Subtotal	**3**					
Fast Control Group						
CCB_CMD [5..0]	6	IN	Bussed	GTLP	Level	Used
CCB_ECRES	1	IN	Bussed	GTLP	25ns	Used
CCB_BCRES	1	IN	Bussed	GTLP	25ns	Used
CCB_CMD_STR	1	IN	Bussed	GTLP	25ns	Used
CCB_BX0	1	IN	Bussed	GTLP	25ns+ECL FP	Not Used
CCB_L1ACC	1	IN	Bussed	GTLP	25ns+ECL FP	Used
CCB_DAT [7..0]	8	IN	Bussed	GTLP	Level	Used
CCB_DAT_STR	1	IN	Bussed	GTLP	25ns	Used
CCB_RDY	1	IN	Bussed	GTLP	Static level	Used
Subtotal	**21**					
Reload Group						
CCB_SP_HRES	1	IN	Bussed	GTLP	400ns	Used
SP_CFG_DONE	1	OUT	Point-to-Point	GTLP	Level	Used
Subtotal	**2**					
Reserved Group						
CCB_RSVD [3..0][1]	4	IN	Bussed	GTLP	25ns	Used
SP_RSVD [3..0][2]	4	OUT	Bussed	GTLP	25ns	Used
Subtotal	**8**					
Total	**34**					

The Clock Group includes differential clock and clock enable lines. The SP uses the CCB_CLK signal as a reference for its on-board QPLL. The 40 MHz QPLL output after de-skewing drives each of the SP FPGA. The 80 MHz QPLL output delivers a reference clock to

[1] CCB_RSVD3 is assigned for CCB_L1RES – L1 Reset signal resets L1 buffers and resynchronizes optical links.
[2] SP_RSVD3 is assigned for SP_L1REQ – L1 request, local trigger generated by the SP_FPGA logic.

GTX_CLK pins of the TLK2501 serializers / deserializers. The SP never uses the CCB_CLK_EN signal.

The Fast Control Group includes a CCB_RDY status line, TTCrx command and data busses with strobes, and a few TTCrx signals, decoded by the CCB. The Fast Control Group signals are valid when and only when the CCB_RDY is LOW. The SP does not use any of the decoded TTCrx signals.

The Reload Group includes a CCB_SP_HRES (Hard Reset) signal for reconfiguration of the SP FPGAs and a SP_CFG_DONE (Configuration Done) status line the SP returns to the CCB.

The Reserved Group is only partially specified at the moment, see footnotes to Table 1.

The VME_FPGA delivers fast control signals to every SP FPGA via a 6-bit Fast Control (FC) bus. Table 2 sets correspondence between the FC and CCB signals.

Table 2: Correspondence between the backplane and SP Internal Fast Control Bus Signals

CCB Command Description	CCB Backplane Signal or Command Code	TTCvi Broadcast command	Internal Condition	Fast Control Bus Command Code
Dedicated Lines				
L1 Accept	ccb_l1acc		L1A_FSM in L1A_RUN	fc_cmd[5] or FC_L1ACC
L1 Accept	ccb_l1acc		If enabled by VM/MA/CSR_TFC	fc_cmd[4] or FC_TFRUN
L1 Accept	ccb_l1acc		If enabled by VM/MA/CSR_SFC	fc_cmd[3] or FC_SFRUN
Inject Test Pattern into SP	ccb_cmd[5:0]=0x2F or CCB_TPSP	0xBC	If enabled by VM/MA/CSR_TFC	fc_cmd[4] or FC_TFRUN
Inject Test Pattern into SP	ccb_cmd[5:0]=0x2F or CCB_TPSP	0xBC	If enabled by VM/MA/CSR_SFC	fc_cmd[3] or FC_SFRUN
Bunch Crossing Zero Mark	ccb_cmd[5:0]=0x01 or CCB_BC0	0x04	If enabled by VM/MA/CSR_TFC	fc_cmd[4] or FC_TFRUN
Bunch Crossing Zero Mark	ccb_cmd[5:0]=0x01 or CCB_BC0	0x04	If enabled by VM/MA/CSR_SFC	fc_cmd[3] or FC_SFRUN
Inject Test Pattern into TMB	ccb_cmd[5:0]=0x24 or CCB_TPTMB	0x90	If enabled by VM/MA/CSR_SFC	fc_cmd[3] or FC_SFRUN
Inject Test Pattern into MPC	ccb_cmd[5:0]=0x30 or CCB_TPMPC	0xC0	If enabled by VM/MA/CSR_SFC	fc_cmd[3] or FC_SFRUN
Encoded Commands				
No command / Idle state	ccb_cmd[5:0]=0x00 or CCB_NOCMD	0x00	Unconditional	fc_cmd[2:0]=0x0 or FC_NOCMD
Bunch Counter Reset	ccb_cmd[5:0]=0x32 or CCB_BXRES	0xC8	Unconditional	fc_cmd[2:0]=0x1 or FC_BXRES
Event Counter Reset	CCB_ECRES or CCB_BERES	0x02 0x03	Unconditional	fc_cmd[2:0]=0x2 or FC_ECRES
L1 Reset – Resets L1 Buffers and Resynchronizes Optical Links	ccb_cmd[5:0]=0x03 or CCB_L1RES	0x0C	Unconditional	fc_cmd[2:0]=0x3 or FC_L1RES
Bunch Crossing Zero Mark	ccb_cmd[5:0]=0x01 or CCB_BC0	0x04	Unconditional	fc_cmd[2:0]=0x4 or FC_BC0
Start Data Taking	ccb_cmd[5:0]=0x06 or CCB_L1STT	0x18	Unconditional	fc_cmd[2:0]=0x5 or FC_L1STT
Stop Data Taking	ccb_cmd[5:0]=0x07 or CCB_L1STP	0x1C	Unconditional	fc_cmd[2:0]=0x6 or FC_L1STP
Spare				fc_cmd[2:0]=0x7

The FC bus consists of three dedicated lines and three lines for encoded fast control commands. Three dedicated lines are: L1 Accept (FC_L1ACC), one line for triggering Test

FIFO (FC_TFRUN) and one line for triggering Spy FIFO (FC_SFRUN). Signals on dedicated lines may coincide with encoded commands, while encoded commands are mutually exclusive.

Note, that data taking is stopped on power-up, so backplane CCB_L1ACC signals don't pass to the FC_L1ACC line. A sequence of CCB_L1STT and CCB_BC0 commands should be issued to let L1 Accepts pass to the internal FC bus, see Figure 1 for details on the L1Accept Finite State Machine (L1A_FSM). A CCB_L1STP command returns the L1A_FSM from L1A_RUN state into default L1A_STOP state. Besides, CCB_L1RES or CCB_BXRES commands return it into L1A_STOP state unconditionally.

Usually, a periodic CCB_BC0 command is sent automatically, if a LHC orbit signal is available.

A CCB_L1ACC signal is passed to the FC_L1ACC line, if the L1A_FSM is in L1A_RUN state. The FC_L1ACC signal is used to initiate a data readout process and to increment the event counter.

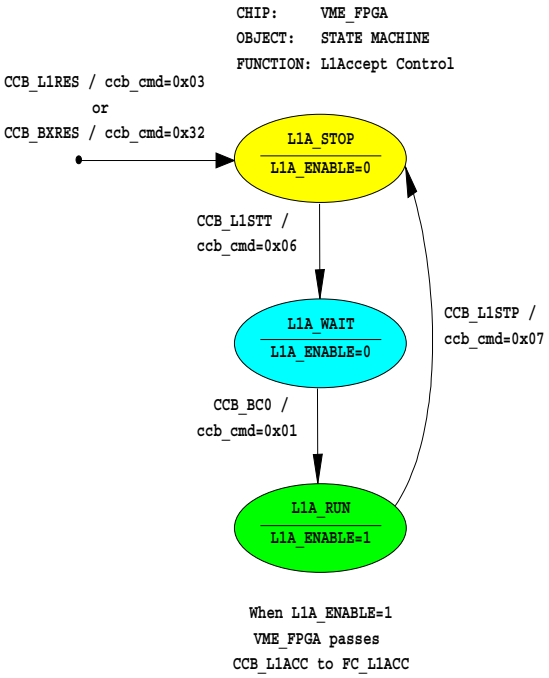


Figure 1: Finite State Machine for L1Accept Control

A FC_SFRUN internal command requests storing data into the Spy FIFO(s). For a list of events that trigger the FC_SFRUN command see the CSR_SFC register description.

A FC_TFRUN internal command requests injecting data from the Test FIFO(s) into the data path. For a list of events that trigger the FC_TFRUN command see the CSR_TFC register description.

Summary of run control fast control commands:

- CCB_ECRES and CCB_BERES – resets Event counter and Valid Pattern Counters (see the DAT_VPC register description for detail) ;

- CCB_L1RES – returns the L1A_FSM into L1A_STOP state, resets Bunch Crossing counters into 0xDEC = 3564, resynchronizes optical links, resets readout buffers, resets Event counter and Valid Pattern Counters;
- CCB_BXRES – returns the L1A_FSM into L1A_STOP state and resets Bunch Crossing counters to 0xDEC = 3564;
- CCB_L1STT – pushes the L1A_FSM into L1_WAIT state, if it is in L1_STOP state;
- CCB_L1STP – returns the L1A_FSM into L1A_STOP state;
- CCB_BC0 – pushes the L1A_FSM into L1_RUN state, if it is in L1_WAIT state.

L1_RUN state serves as a gate signal for Valid Pattern Counters in the FRONT_FPGA and SP_FPGA, see the DAT_VPC register description for detail.

L1_STOP state serves as a gate signal for training pattern generation to facilitate timing-in the MS receive clock to SP data.

The current state of the SP logic can be monitored with four fast monitoring status signals: busy (FM_BSY), ready (FM_RDY), warning-of-overflow (FM_WOF), and out-of-synch (FM_OSY). Each FPGA reports its 4-bit status to the VME_FPGA. The VME_FPGA is capable of masking individual statuses when providing the SP overall status to the RJ45 connector and front panel indicators (LEDs). See the following registers description on fast monitoring status detail: CSR_BSY, CSR_RDY, CSR_WOF, CSR_OSY.

Table 3: SP02 Front Panel LEDs

Description	Left LED Name	Left LED Color	Right LED Color	Right LED Name	Description
Busy	BSY	Red	Green	5.0V_OK	5.0V power is OK
Ready	RDY	Green	Green	3.3V_OK	3.3V power is OK
Warning-of-OverFlow	WOF	Red	Green	2.5V_OK	2.5V power is OK
Out-of-Synch	OSY	Red	Green	1.5V_OK	1.5V power is OK
Local Charged Trigger	LCT	Yellow	Yellow	L1ACC	L1 Accept

Table 4: SP04 Front Panel LEDs

Description	Left LED Name	Left LED Color
Busy	BSY	Red
Ready	RDY	Green
Warning-of-OverFlow	WOF	Red
Out-of-Synch	OSY	Red
Local Charged Trigger	LCT	Yellow

The LED indicators are located above the F5 link transceivers. The BSY, RDY, WOF, and OSY indicators display status of the corresponding signal lines. The L1ACC LED blinks for

25 ms on every CCB_L1ACC. The LCT LED blinks for 25 ms on every LCT found by the SP_FPGA.

Former Power_OK indicators have changed their assignment and now visualize the L1A_FSM states and lock condition of the on-board QPLL.

- 5.0V_OK => FSM is in L1_RUN state;
- 3.3V_OK => FSM is in L1_WAIT state;
- 2.5V_OK => FSM is in L1_STOP state;
- 1.5V_OK => On-board QPLL locked to the backplane clock.

VME Interface

The SP card includes two A24D16 Slave interfaces [ii] implemented in the VME_FPGA and CPLD_FPGA accordingly. Table 5 shows all address modifiers, the SP responds to during the VME Data Transfer Bus (DTB) cycles.

Table 5: SP Address Modifier Codes.

AM	AM Description	Access Description	Interface Chip
39	A24 non privileged data access	Access to all locations, except the BLT Mapping Registers	VME_FPGA
3A	A24 non privileged program access	Access to the BLT Mapping Registers	
3B	A24 non privileged block transfer (BLT)	BLT access using the BLT Mapping Registers	
3D	A24 supervisory data access		VME_CPLD
3E	A24 supervisory program access		
3F	A24 supervisory block transfer (BLT)		

Auxiliary VME Interface

The auxiliary VME_CPLD interface is intended for board configuration and provides access solely for the Bus Scan Controller (BSC). The BSC drives three chains of JTAG-compatible devices, see Table 6:

- Chain 0 consists of the SP_FPGA and its EEPROMs;
- Chain 1 includes the VME_FPGA with EEPROM, the FRONT_FPGAs with EEPROMs, and the DDU_FPGA with EEPROM;
- Chain 2 connects 45 SRAMs.

Table 6: SP Configuration Chains.

Chain No	Device No	Device Name	Device Type	Device ID Code	Bypass Switch
0	1	SP_EEPROM_1	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW2
0	2	SP_EEPROM_2	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW3
0	3	SP_EEPROM_3	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW4
0	4	SP_EEPROM_4	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW5
0	5	SP_EEPROM_5	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW6
0	6	SP_FPGA	XC2V4000-5FF1152C	VVVV 0001 0000 0101 0000 0000 1001 0011	MC_SW1

Chain No	Device No	Device Name	Device Type	Device ID Code	Bypass Switch
1	1	VME_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW4
1	2	VME_FPGA	XC2V1000-5FG456C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW5
1	3	FF5_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW2
1	4	FRONT_FPGA_5	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW3
1	5	FF4_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW14
1	6	FRONT_FPGA_4	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW15
1	7	FF3_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW19
1	8	FRONT_FPGA_3	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW20
1	9	DDU_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW10
1	10	DDU_FPGA	XC2V1000-5FG456C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW11
1	11	FF2_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW12
1	12	FRONT_FPGA_2	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW13
1	13	FF1_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW17
1	14	FRONT_FPGA_1	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW18
2	1	ME4C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	2	ME4C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	3	ME4C_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	4	ME4B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	5	ME4B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW7
2	6	ME4B_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	7	ME4A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	8	ME4A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	9	ME4A_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	10	ME3C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	11	ME3C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	12	ME3C_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	13	ME3B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	14	ME3B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW9
2	15	ME3B_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	16	ME3A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	17	ME3A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	18	ME3A_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	19	ME2C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	20	ME2C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	21	ME2C_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	22	ME2B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	23	ME2B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW8
2	24	ME2B_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	25	ME2A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	26	ME2A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	27	ME2A_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	28	ME1F_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	29	ME1F_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	30	ME1F_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	31	ME1E_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	32	ME1E_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW6
2	33	ME1E_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	34	ME1D_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	35	ME1D_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	36	ME1D_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	37	ME1C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	38	ME1C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	39	ME1C_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	40	ME1B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	41	ME1B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW16
2	42	ME1B_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	43	ME1A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	44	ME1A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	45	ME1A_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	

Alex M. is to determine the VME address mapping for the auxiliary VME interface.

Main VME Interface

A24 Non Privileged Data Access

An A24 non privileged data access (AM=0x39) to the main VME_FPGA interface utilizes a 5-bit geographical addressing scheme [ii] and provides for the VME Data Transfer Bus (DTB) multicast ***write*** cycles by partitioning the address space into the following fields, see Table 7.

Table 7: Address Format for Non Privileged Data Access

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SA [4:0]					CA [6:0]							0	MA [1:0]		RA [6:0]							0	0

Here:

- 0 – Zero value address line;
- SA [4:0] – Slot Address, could be either Slot Geographical Address (GA), or Slot Multicast Address (30);
- CA [6:0] – Chip Address. Positional coding provides simultaneous write access to any combination of SP FPGAs (except VME_FPGA), see Table 8;
- MA [1:0] – Muon Address. Each FRONT_FPGA processes data for 3 muons, and the SP_FPGA services 3 PT LUTs. A 2-bit MA field provides write access either to a single muon-related register or to all three such registers simultaneously, see Table 9 for details.
- RA [6:0] – Register Address inside FPGA(s). There are 4 groups of registers in total, see Table 10 for details:
    - Action Register Group. Writing to these write-only registers causes pulses, like reset or test pulse, to be generated and/or operations, like start or stop L1ACC processing, to be performed.
    - Control/Status Register Group. These registers carry 2 groups of bits: read-only status bits to monitor, and read/write bits to control behavior of the SP logic.
    - Address Register Group. These registers provide access to SRAM and Register File address counters.
    - Data Register Group. The group provides access to SRAM, FIFO and Register File data.

Full Address (FA) of the register is defined as:
FA = (SA << 19) + (CA << 12) + (MA << 9) + (RA << 2).

Table 8: Chip Address Field Format for Non Privileged Data Access

Chip	CA, binary	Description
VM	000_0000	VME_FPGA Access
F1	000_0001	FRONT_FPGA_1 Access
F2	000_0010	FRONT_FPGA_2 Access
F3	000_0100	FRONT_FPGA_3 Access
F4	000_1000	FRONT_FPGA_4 Access
F5	001_0000	FRONT_FPGA_5 Access
DD	010_0000	DDU_FPGA Access
SP	100_0000	SP_FPGA Access

Table 9: Muon Address Field Format for Non Privileged Data Access

Label	Muon in FPGA	MA, binary	Description
MA	ALL	00	Access to all three muon-related registers
M1	A/D/1	01	Access to a First (A or D or 1) muon-related register
M2	B/F/2	10	Access to a Second (B or E or 2) muon-related register
M3	C/E/3	11	Access to a Third (C or F or 3) muon-related register

Note, that only ***write*** access is defined for a group of registers, while ***read*** access may only be executed to a single register.

Table 10: Register Address Field Format for Non Privileged Data Access

RA, hex	Register Label	Description	Valid CA / Valid MA				Page
			SP	DD	Fx	VM	
Action Register Group							
0x00	ACT_HR	Hard Reset	-	-	-	MA	14
0x01	ACT_CMR	Clock Manager Reset	MA	MA	MA	MA	15
0x02	ACT_LCR	Link Counter Reset	-	MA	MA/M1/M2/M3	-	15
0x03	ACT_XFR	FIFO Reset	MA	MA	MA	-	17
0x04	ACT_ACR	Address Counter Reset	MA	-	MA	-	14
0x05	ACT_FCC	Fast Control Command	-	-	-	MA	16
Status Register Group (Expert Only)							
0x0A	STS_VAL	VME Low Address Status	-	-	-	MA	20
0x0B	STS_VAH	VME High Address Status	-	-	-	MA	68
0x0C	STS_VAM	VME Medium Address Status	-	-	-	MA	70
0x0E	STS_CD	Chip Data Status	-	-	-	MA	20
0x0F	STS_CA	Chip Acknowledge Status	-	-	-	MA	68
0x10	STS_CCB	Fast Control Status	MA	-	MA	-	20
0x11	STS_ANA	CCB Logic Analyzer	-	-	-	MA	64
0x12	STS_MWA	MS Winners Analyzer	MA	-	-	-	68
0x13	STS_BC0	Orbit Analyzer	-	-	-	MA	64
0x14	STS_AF	AF FSU Status	-	-	M1/M2/M3	-	20
Control/Status Register Group							
0x1E	CSR_BID	Board Identifier	MA	MA	M1/M2/M3	MA	20
0x1F	CSR_SID	SP Core Identifier	MA	-	-	-	20
0x20	CSR_CID	Chip Identifier	MA	MA	MA	MA	20
0x21	CSR_QDB	QPLL Daughter Board Control/Status	-	-	-	MA	33
0x22	CSR_CM1	Clock Manager_1 Control/Status	MA	MA	MA	MA	33
0x23	CSR_CM2	Clock Manager_2 Control/Status	MA	MA	MA	MA	25
0x24	CSR_HR	Hard Reset Mask	-	-	-	MA	27
0x25	CSR_CFG	Configuration Done Status	-	-	-	MA	27

RA, hex	Register Label	Description	Valid CA / Valid MA				Page
			SP	DD	Fx	VM	
0x26	CSR_INI	Init Status	-	-	-	MA	27
0x28	CSR_BSY	Busy Mask/Status	-	-	-	MA	23
0x29	CSR_RDY	Ready Mask/Status	-	-	-	MA	28
0x2A	CSR_WOF	Warning-of-OverFlow Mask/Status	-	-	-	MA	47
0x2B	CSR_OSY	Out-of-SYnch Mask/Status	-	MA	MA	MA	31
0x2C	CSR_MWC	MS Winners Configuration	MA	-	-	-	30
0x2D	CSR_FCC	Fast Control Configuration/Status	MA	MA	MA	MA	27
0x2E	CSR_REQ	L1 Request Configuration	MA	-	-	-	32
0x30	CSR_LEC	Link Error Counters	-	MA	M1/M2/M3	-	32
0x31	CSR_AF	Alignment FIFO Status	M1/M2	MA	M1/M2/M3	-	20
0x32	CSR_TF	Test FIFO Status	M1/M2/M3	MA	M1/M2/M3	-	42
0x33	CSR_SF	Spy FIFO Status	M1/M2/M3	MA	M1/M2/M3	-	35
0x34	CSR_PF	Pipeline FIFO Status	MA	-	MA	-	33
0x35	CSR_DF	DAQ FIFO Status	-	MA	-	-	25
0x36	CSR_TBC	Transition Board Configuration	-	-	MA	-	41
0x37	CSR_LF	L1 FIFO Status	MA	MA	MA	-	33
0x38	CSR_RBW	Ring Buffer Write Pointer	MA	-	MA	-	34
0x39	CSR_RBR	Ring Buffer Read Pointer	MA	-	MA	-	34
0x3A	CSR_SF1	F1 Spy FIFO Status	M1/M2/M3	-	-	-	34
0x3B	CSR_SF2	F2 Spy FIFO Status	M1/M2/M3	-	-	-	36
0x3C	CSR_SF3	F3 Spy FIFO Status	M1/M2/M3	-	-	-	36
0x3D	CSR_SF4	F4 Spy FIFO Status	M1/M2/M3	-	-	-	36
0x3E	CSR_SF5	F5 Spy FIFO Status	M1/M2/M3	-	-	-	37
0x3F	CSR_SFE	EMU Spy FIFO Status	MA	-	-	-	37
0x40	CSR_LNK	Link Control/Status	-	MA	MA/M1/M2/M3	-	28
0x41	CSR_AFD	Alignment FIFO Delay	MA	MA	MA	-	21
0x42	CSR_TFC	Test FIFO Configuration	MA	MA	MA	-	44
0x43	CSR_SFC	Spy FIFO Configuration	MA	MA	MA	MA	37
0x44	CSR_PFD	Pipeline FIFO Read Delay	MA	-	MA	-	39
0x45	CSR_DFC	DAQ FIFO Configuration	-	MA	-	-	25
0x46	CSR_SCC[3]	SP Core Configuration	MA	-	-	-	40
0X47	CSR_TFB	Barrel Test FIFO Status	M1/M2	-	-	-	41
0x48	CSR_SFB	Barrel Spy FIFO Status	M1/M2	-	-	-	40
0x49	CSR_SFM	Muon Sorter Spy FIFO Status	M1/M2/M3	-	-	-	40
0x4A	CSR_TF1	F1 Test FIFO Status	M1/M2/M3	-	-	-	41
0x4B	CSR_TF2	F2 Test FIFO Status	M1/M2/M3	-	-	-	43
0x4C	CSR_TF3	F3 Test FIFO Status	M1/M2/M3	-	-	-	43
0x4D	CSR_TF4	F4 Test FIFO Status	M1/M2/M3	-	-	-	43
0x4E	CSR_TF5	F5 Test FIFO Status	M1/M2/M3	-	-	-	44
0x4F	CSR_TFE	EMU Test FIFO Status	MA	-	-	-	44
Address Counter Group							
0x50	CNT_LPL	Local Phi LUT Address Low	-	-	MA	-	18
0x51	CNT_LPH	Local Phi LUT Address High	-	-	MA	-	19
0x52	CNT_GLL	Global_Eta/Phi/DT LUT Address Low	-	-	MA	-	19
0x53	CNT_GLH	Global_Eta/Phi/DT LUT Address High	-	-	MA	-	19
0x56	CNT_PTL	PT LUT Address Low	MA	-	-	-	19
0x57	CNT_PTH	PT LUT Address High	MA	-	-	-	19
0x58	CNT_ETA	Eta Address	MA	-	-	-	18

[3] Access to this register is available only when SP04 is under VME control (see VM/MA/CSR_FCC) and the L1A_FSM is in L1_STOP state.

RA, hex	Register Label	Description	Valid CA / Valid MA				Page
			SP	DD	Fx	VM	
Data Register Group							
0x5A	DAT_TF1	F1 Test FIFO Data	M1/M2/M3	-	-	-	48
0x5B	DAT_TF2	F2 Test FIFO Data	M1/M2/M3	-	-	-	61
0x5C	DAT_TF3	F3 Test FIFO Data	M1/M2/M3	-	-	-	61
0x5D	DAT_TF4	F4 Test FIFO Data	M1/M2/M3	-	-	-	61
0x5E	DAT_TF5	F5 Test FIFO Data	M1/M2/M3	-	-	-	62
0x5F	DAT_TFE	EMU Test FIFO Data	MA	-	-	-	62
0x60	DAT_LP[3]	Local Phi LUT Data	-	-	MA/M1/M2/M3	-	51
0x62	DAT_GP[3]	Global Phi LUT Data	-	-	MA/M1/M2/M3	-	50
0x63	DAT_DT[3]	DT LUT Data	-	-	MA/M1/M2/M3	-	48
0x64	DAT_GE[3]	Global Eta LUT Data	-	-	MA/M1/M2/M3	-	50
0x66	DAT_PT[3]	PT LUT Data	MA/M1/M2/M3	-	-	-	51
0x68	DAT_ETA[3]	Eta Data	MA	-	-	-	48
0x69	DAT_VPC	Valid Pattern Counter Data	M1/M2/M3	-	M1/M2/M3	-	63
0x6A	DAT_SF1	F1 Spy FIFO Data	M1/M2/M3	-	-	-	63
0x6B	DAT_SF2	F2 Spy FIFO Data	M1/M2/M3	-	-	-	54
0x6C	DAT_SF3	F3 Spy FIFO Data	M1/M2/M3	-	-	-	55
0x6D	DAT_SF4	F4 Spy FIFO Data	M1/M2/M3	-	-	-	55
0x6E	DAT_SF5	F5 Spy FIFO Data	M1/M2/M3	-	-	-	55
0x6F	DAT_SFE	EMU Spy FIFO Data	MA	-	-	-	56
0x72	DAT_TF	Test FIFO Data	MA/M1/M2/M3	MA	MA/M1/M2/M3	-	56
0x73	DAT_SF	Spy FIFO Data	M1/M2/M3	MA	M1/M2/M3	-	51
0x75	DAT_DF	DAQ FIFO Data	-	MA	-	-	54
0x76	DAT_TFB	Barrel Test FIFO Data	MA/M1/M2	-	-	-	62
0x77	DAT_SFB	Barrel Spy FIFO Data	M1/M2	-	-	-	56
0x78	DAT_SFM	Muon Sorter Spy FIFO Data	M1/M2/M3	-	-	-	57
0x7F	DAT_RW	Read / Write Data	MA	MA	MA	MA	52

The main VME_FPGA interface distributes VME control all over the board via the Internal Data Transfer Bus (IDTB). IDTB is a synchronous parallel bus that is used by the VME_FPGA to transfer data to or from other SP FPGA(s): the SP_FPGA, 5 FRONT_FPGAs, and the DDU_FPGA.

The IDTB bus lines are grouped into 4 categories:

- Address Lines: A[11:2] see Table 11;
- Data Lines: D[15:0] Bi-directional;
- Control Lines: /CS[7:1] Chip Select, active LOW;
  /ACK[7:1] Acknowledge, active LOW;
  /WR Write, active LOW;
- Auxiliary Lines: VMB_WR Buffer Write;
  VMB_/OE Buffer Output Enable, active LOW.

Table 11: IDTB Address Format

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2
RV	MA		RA						
RV	IA								

- IA – Internal DTB Address, defines a storage location inside FPGA

- RV – Reserved line

To prevent data lines from being too long they are split into two segments: the SP segment and the FRONT/DDU segment, with bi-directional buffers in between. The SP segment connects directly to the VME_FPGA pins. The FRONT/DDU segment is located behind the buffers. Two auxiliary lines: Buffer Write (data direction) and Buffer Output Enable, - are used to control data flow through the buffers.

The IDTB transfer is a sequence of level states on the signal lines that results in the transfer of an address and two bytes of data between the VME_FPGA and other SP FPGA(s).

Each IDTB cycle is an inherent part of the backplane DTB cycle, when DTB addresses FPGA(s), other than the VME_FPGA. Chip Select (/CS) plays a role of the DS* strobe and Acknowledge (/ACK) plays a role of the DTACK*. The major difference between backplane DTB and IDTB is that IDTB is a synchronous bus, i.e. both /CS and /ACK handshake signals should be asserted on the rising edge of the system clock at source, and sensed with the next rising edge of the system clock at destination.

The VME_FPGA initiates two types of IDTB cycles:

- **IDTB Write cycle** transfers data from the VME_FPGA to one or more destination FPGA(s). The cycle begins when the VME_FPGA sets address, data, Write and optionally Buffer Write and Buffer Output Enable on the corresponding lines and issues one or more Chip Selects. Selected FPGA(s) capture(s) the address and check(s) to see if it is to respond to the cycle. If so, sensing Write in a LOW state, it stores the data and acknowledges the transfer. The VME_FPGA then terminates the cycle.
- **IDTB Read cycle** transfers data from the source FPGA to the VME_FPGA. The cycle begins when the VME_FPGA sets address and optionally a Buffer Output Enable and issues a Chip Select. Selected FPGA captures the address and checks to see if it is to respond to the cycle. If so, sensing Write in a HIGH state, it retrieves the data from the corresponding storage, places it on the data lines and acknowledges the transfer. The VME_FPGA then terminates the cycle.

Normally the VME_FPGA would terminate the DTB transfer with the Data Transfer Acknowledge (DTACK*) asserted low. If during the DTB cycle the addressable SP detects that the VME Master either addresses a non-existed location, or tries to write to a read-only location, the VME_FPGA terminates the cycle with a Bus Error (BERR*) asserted low. The VME_FPGA is not aware of the DTB outcome, when it passed the DTB cycle to the IDTB. If the expected IDTB Acknowledge(s) is (are) not received in time, the VME_FPGA terminates the cycle driving BERR* low.

A24 Non Privileged Program Access

An A24 non privileged program access (AM=0x3A) is used to load four mapping locations in the VME FPGA, see Table 12 for valid address fields

Table 12: Address Format for Non Privileged Program Access

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SA					X													PA				0	0

Here:

- X – Don't care bit;
- SA – Slot Address, could be either Slot Geographical Address (GA), or Slot Multicast Address (30);
- PA – Program Address, defines 16 register locations in the non privileged program space, see Table 13 for valid addresses.

Table 13: Register Address Field Format for Non Privileged Program Access

PA, hex	Register Label	Description
BLT Mapping Control/Status Register Group		
0x0		
0x1	CPA_BF1	BLT Mapping FIFO_1 Control/Status
0x2	CPA_BF2	BLT Mapping FIFO_2 Control/Status
0x3	CPA_BF3	BLT Mapping FIFO_3 Control/Status
0x4		Reserved
0x5		Reserved
0x6		Reserved
0x7		Reserved
BLT Mapping Data Register Group		
0x8	DPA_BLT	BLT Mapping Data
0x9	DPA_BF1	BLT Mapping FIFO_1 Data
0xA	DPA_BF2	BLT Mapping FIFO_2 Data
0xB	DPA_BF3	BLT Mapping FIFO_3 Data
0xC		Reserved
0xD		Reserved
0xE		Reserved
0xF		Reserved

Details on the above registers can be found in the Register Detail section under the register label. During BLT transfers, mapping registers substitute the DTB address with a 16-bit address, used to access storage location(s) in the non privileged data space. The format of the mapping data/address is shown below:

Table 14: BLT Mapping Location Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CA							MA		RA						

Here CA, MA, and RA are address fields, described in the A24 Non Privileged Data Access section above.

A24 Non Privileged Block Transfer (BLT)

Any storage location, accessible via the A24 Non Privileged Data Access, can also be accessed via an A24 non privileged block transfer (BLT), when AM=0x3B. The BLT, prior to executing, should be initialized by loading a mapping location with one or more destination addresses. The BLT mapping locations are listed in Table 13. During the BLT DTB cycle the VME_FPGA, depending on the value in the BA field, uses one of the preloaded mapping

locations to substitute the current DTB address with the address stored in the mapping location, see Table 15. Table 14 shows the BLT mapping location data format and Table 16 lists 4 128Kbyte windows for block transfers.

Table 15: Address Format for Non Privileged Block Transfers

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SA					BA		X																0

Here:

- SA – Slot Address, could be either Slot Geographical Address (GA), or Slot Multicast Address (30);
- BA – BLT Address. Defines one out of four BLT Mapping locations inside the VME_FPGA to substitute the current VMA backplane address with the preloaded one;
- X – Don't care bit.

Table 16: BLT Address Field Format for Non Privileged Block Transfers

BA, binary	Register Name	First D16 Transfer Address, hex	Last D16 Transfer Address, hex	Address Space
00	BLT Mapping Register	0x00000	0x1FFFE	64 Kwords = 128 Kbytes
01	BLT Mapping FIFO_1	0x20000	0x3FFFE	64 Kwords = 128 Kbytes
10	BLT Mapping FIFO_2	0x40000	0x5FFFE	64 Kwords = 128 Kbytes
11	BLT Mapping FIFO_3	0x60000	0x7FFFE	64 Kwords = 128 Kbytes

Register Detail

Action Register Group

ACT_ACR – Address Counters Reset

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 25 ns reset pulse to a corresponding address counter. The register address is applicable to FRONT_FPGA and SP_FPGA.

Table 17: ACT_ACR Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	GLR	LPR

Here:

- X – Don't care bit;
- LPR – Local Phi LUT Address Counter Reset;
- GLR – Global Phi/Eta/DT LUT Address Counter Reset.

Table 18: ACT_ACR Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	ETR	PTR	X	X

Here:

- X – Don't care bit;
- PTR – PT LUT Address Counter Reset;
- ETR – Eta Min/Max/Window Address Counter Reset.

ACT_CMR – Clock Manager Reset

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 50 ns reset pulse(s) to selected DCM(s) and QPLL Daughter Board (DB_QPLL). The pulse resets also the DCM and QPLL troubleshooting counters described under CSR_QDB – QPLL Daughter Board Control/Status, CSR_CM1 – System Clock Manager 1 Status and CSR_CM2 – System Clock Manager 2 Status headings. The register address is applicable to all FPGAs.

Table 19: ACT_CMR Data Format for VM_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	CMR2	CMR1	QPLL

Here:

- X – Don't care bit;
- QPLL – DB_QPLL Reset, forces a Daughter Board QPLL into frequency calibration procedure to reacquire lock; it also resets the DB_LCK and TTCrq_LCK "loss of lock" counters and sets a default QPLL mode;
- CMR1 – Clock Manager 1 Reset;
- CMR2 – Clock Manager 2 Reset.

Table 20: ACT_CMR Data Format for FRONT_FPGA, DDU_FPGA, and SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	CMR2	CMR1	X

Here:

- X – Don't care bit;
- CMR1 – Clock Manager 1 Reset;
- CMR2 – Clock Manager 2 Reset.

ACT_FCC – Fast Control Command

VME write cycle to this write-only register is equivalent to getting the same fast control command from the CCB over the backplane. The difference is that the CCB commands are available to all modules in the crate, while this command affects only the addressable SP. Note, that ACT_FCC commands are enabled only when the CSR_FCM register is configured to a local fast control mode.

Table 21: ACT_FCC Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L1A	X	X	X	L1R	X	X	X	FCC7	FCC6	FCC5	FCC4	FCC3	FCC2	FCC1	FCC0

Here:

- X – Don't care bit;
- FCC[7:0] – Fast Control Command, the data format matches the TTC $C4 register and the CCB CSR2 register formats;
- L1A – L1Accept Command;
- L1R – L1Request Command – sends local trigger to the backplane bussed line. Normally L1Request is generated by the SP_FPGA core logic.

ACT_HR – FPGA Hard Reset

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 400 ns Hard Reset pulse to the selected FPGA(s) onboard. Hard Reset is applied to the /PROG_B pin of the corresponding FPGA. A VME-generated Hard Reset is ORed with a CCB backplane hard reset. This register address is applicable to the VME_FPGA only. Bit 0 of this register has a special meaning. Instead of VME_FPGA hard reset it performs soft reset of all FPGAs onboard.

Sensing a hard reset on its input, the FPGA reloads its configuration from the associated configuration EPROM. The user may use the ACT_HR transfer cycle to verify chip presence on the board. To make sure all FPGA chips are present on the board, the CSR_CFG read transfer cycle should be executed twice after the ACT_HR: first time when chips are engaged in the configuration process and second time after a 5 sec pause, when the configuration is definitely completed. If there is a missing FPGA chip on the board (a mezzanine card is not installed, for example) then the corresponding Configuration Done line remains floating, and can be sensed by the VME_FPGA as being either in HIGH (Logic ONE) or LOW (Logic ZERO) state. But in any case, Configuration Done line for a missing chip (for example, SP_FPGA) would retain its state, while the one for a successfully configured FPGA will be LOW on the first read and HIGH on the second read. See Table 44 for chip mapping.

Table 22: ACT_HR Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	SPHR	DDHR	F5HR	F4HR	F3HR	F2HR	F1HR	VMSR

Here:

- X – Don't care bit;
- VMSR – VME_FPGA Soft Reset;
- F1HR – FRONT_FPGA_1 Hard Reset;
- F2HR – FRONT_FPGA_2 Hard Reset;
- F3HR – FRONT_FPGA_3 Hard Reset;
- F4HR – FRONT_FPGA_4 Hard Reset;
- F5HR – FRONT_FPGA_5 Hard Reset;
- DDHR – DDU_FPGA Hard Reset;
- SPHR - SP_FPGA Hard Reset.

ACT_LCR – Link Counter Reset

Writing Logic ONE to specified bit(s) of this write-only register results in sending 25 ns reset pulse(s) to selected error counter(s) described under the CSR_LNK, CSR_LEC and DAT_VPC headings. The register address is applicable to the FRONT_FPGA and to the SP_FPGA.

Table 23: ACT_LCR Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	VPR	TER	SLR	CER	EWR

Here:

- X – Don't care bit;

- EWR – TLK2501 Error Word Counter Reset in the CSR_LEC register (RXDV == HIGH, RXER == HIGH);
- CER – TLK2501 Carrier Extend Counter Reset in the CSR_LEC register (RXDV == LOW, RXER == HIGH);
- SLR – FINISAR optical receiver Signal Loss Counter Reset in the CSR_LEC register (RXSD goes LOW);
- TER – PRBS Test Error Counter Reset in the CSR_LNK register;
- VPR – Valid Pattern Counter Reset in the DAT_VPC register.

Table 24: ACT_LCR Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	VPR	X	X	X	X

Here:

- X – Don't care bit;
- VPR – Valid Pattern Counter Reset in the DAT_VPC register.

ACT_XFR – FIFO Reset

Writing Logic ONE to a specified bit of this write-only register results in sending a 25 ns reset pulse to the corresponding FIFO(s). The register address is applicable to the FRONT_FPGA, DDU_FPGA and SP_FPGA.

Table 25: ACT_XFR Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	LFR	PFR	SFR	TFR	X

Here:

- X – Don't care bit;
- TFR – All Test FIFOs Reset (Init);
- SFR – All Spy FIFOs Reset (Init);
- PFR – Pipeline FIFO Reset (Init);
- LFR – L1 Accept FIFO Reset (Init) is equivalent to FC_L1RES signal. It also resets Ring Buffer Read and Ring Buffer Write Pointers.

Table 26: ACT_XFR Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	LFR	PFR	SFR	TFR	AFR

Here:

- X – Don't care bit;
- AFR – Barrel Alignment FIFO Reset (Init);
- TFR – All Test FIFOs Reset (Init);
- SFR – All Spy FIFOs Reset (Init);
- PFR – Pipeline FIFO Reset (Init);
- LFR – L1 Accept FIFO Reset (Init) is equivalent to FC_L1RES signal. It also resets the Ring Buffer Read and Ring Buffer Write Pointers.

Table 27: ACT_XFR Data Format for DDU_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	DFR	LFR	X	SFR	TFR	X

Here:

- X – Don't care bit;
- TFR – Test FIFO Reset (Init);
- SFR –Spy FIFO Reset (Init);
- LFR – L1 Accept FIFO Reset (Init) is equivalent to FC_L1RES signal. It also resets readout and FMM state machines;
- DFR – DAQ (VME) Readout FIFO Reset (Init).

Address Counter Register Group

CNT_ETA – Eta Address Counter

This read/write register carries current value of the Eta Min/Max/Window/Offset Address Counter, as shown in the table below. The default register value on power-up is zero. The counter auto-increments on every access to the DAT_ETA register. The counter can be reset with the ACT_ACR command.

Table 28: CNT_ETA Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	ETA4	ETA3	ETA2	ETA1	ETA0
											ETA Address Counter				

Here:

- X – Don't care bit for writes and zero for reads;
- ETA [4:0] = 0…25 – Eta Min/Max/Window/Offset Address Counter.

CNT_GLH – Global LUTs Address Counter High

This read/write register carries current value of the global LUTs address counter 3 Most Significant Bits (MSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all global LUTs serviced by the FRONT_FPGA and auto-increments on every access to any DAT_GP/DAT_DT/DAT_GE register in a chip. The counter can be reset with the ACT_ACR command.

Table 29: CNT_GLH Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	GA18	GA17	GA16
													GL LUTs AC MSB		

Here:

- X – Don't care bit for writes and zero for reads;
- GA [18:16] – Global LUTs Address Counter, 3 MSB.

CNT_GLL – Global LUTs Address Counter Low

This read/write register carries current value of the global LUTs address counter 16 Least Significant Bits (LSB), as shown in the table below. The default register value on power-up is

zero. The counter is common for all global LUTs serviced by the FRONT_FPGA and auto-increments on every access to any DAT_GP/DAT_DT/DAT_GE register in a chip. The counter can be reset with the ACT_ACR command.

Table 30: CNT_GLL Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GA15	GA14	GA13	GA12	GA11	GA10	GA9	GA8	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0
Global LUTs Address Counter LSB															

Here:

- X – Don't care bit for writes and zero for reads;
- GA [15:0] – Global LUTs Address Counter, 16 LSB.

CNT_LPH – Local Phi LUT Address Counter High

This read/write register carries current value of the local phi LUT address counter 3 Most Significant Bits (MSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all local LUTs serviced by the FRONT_FPGA and auto-increments on every access to any DAT_LP register in a chip. The counter can be reset with the ACT_ACR command.

Table 31: CNT_LPH Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	LA18	LA17	LA16
													LP LUT AC MSB		

Here:

- X – Don't care bit;
- LA [18:16] – Local Phi LUT Address Counter, 3 MSB.

CNT_LPL – Local Phi LUT Address Counter Low

This read/write register carries current value of the local phi LUT address counter 16 Least Significant Bits (LSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all local LUTs serviced by the FRONT_FPGA and auto-increments on every access to any DAT_LP register in a chip. The counter can be reset with the ACT_ACR command.

Table 32: CNT_LPL Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LA15	LA14	LA13	LA12	LA11	LA10	LA9	LA8	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0
Local Phi LUT Address Counter LSB															

Here:

- X – Don't care bit;
- LA [15:0] – Local Phi LUT Address Counter, 16 LSB.

CNT_PTH – PT LUTs Address Counter High

This read/write register carries current value of the global LUTs address counter 3 Most Significant Bits (MSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all PT LUTs serviced by the SP_FPGA and auto-increments on

every access to any DAT_PT register in a chip. The counter can be reset with the ACT_ACR command.

Table 33: CNT_PTH Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	PTA20	PTA19	PTA18	PTA17	PTA16
											PT LUTs AC MSB				

Here:

- X – Don't care bit for writes and zero for reads;
- PTA [20:16] – Global LUTs Address Counter, 5 MSB.

CNT_PTL – PT LUTs Address Counter Low

This read/write register carries current value of the PT LUTs address counter 16 Least Significant Bits (LSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all PT LUTs serviced by the SP_FPGA and auto-increments on every access to any DAT_PT register in a chip. The counter can be reset with the ACT_ACR command.

Table 34: CNT_PTL Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PTA15	PTA14	PTA13	PTA12	PTA11	PTA10	PTA9	PTA8	PTA7	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
PT LUTs Address Counter LSB															

Here:

- X – Don't care bit for writes and zero for reads;
- PTA [15:0] – PT LUTs Address Counter, 16 LSB.

Control/Status Register Group

CSR_AF – Alignment FIFO Status

This read-only register shows the Alignment FIFO (AF) word count.

Front FPGA

In the FRONT_FPGA Alignment FIFOs are used to switch from the receiver clock domain to the system clock domain and to compensate for different optical link latencies. Different links may show different AF word counts after link synchronization procedure has been performed. Dispersion of word count values corresponds to the dispersion of link latencies. To time-in all active links and minimize the overall AF latency one has to adjust the CSR_AFD register value and perform L1 Resets until the minimal AF value amongst all active links becomes equal to 2 or 3. The FRONT_FPGA AF runs at 80 MHz clock, so the AF latency in bunch crossings is twice less the AFC value.

Table 35: CSR_AF Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AFFF	AFEF	0	0	0	0	0	AFC8	AFC7	AFC6	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0
Flags							Alignment FIFO Word Count								

Here:

- AFC [8:0] = 0...511 – Alignment FIFO Read Word Count;

- AFFF – Alignment FIFO Full Flag or AFC = 511;
- AFEF – Alignment FIFO Empty Flag.

SP FPGA

In the SP_FPGA Alignment FIFO performs the same function for barrel muon data as it does in the FRONT_FPGA for the EMU muon data. The difference is that to time-in the barrel data the user has to adjust only the CSR_AFD value, no L1 Reset is required. The SP_FPGA AF runs at 40 MHz clock, so the AF latency in bunch crossings equals to the AFC value.

Table 36: CSR_AF Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AFFF	AFEF	0	0	0	0	0	0	0	0	0	0	AFC3	AFC2	AFC1	AFC0
Flags												Alignment FIFO Word Count			

Here:

- AFC [3:0] = 0...15– Alignment FIFO Read Word Count;
- AFFF – Alignment FIFO Full Flag or AFC = 15;
- AFEF – Alignment FIFO Empty Flag.

DDU FPGA

In the DDU_FPGA there are two Alignment FIFOs: one at the TLK2501 output and the other at the TLK2501 input. The Alignment FIFOs perform function of the elastic output and input buffers to compensate for differences between the doubled RF clock of 80.1574 MHz and the DDU link reference clock of 80.0000 MHz.

Table 37: CSR_AF Data Format for DDU_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AFFF	AFEF	0	AFRC4	AFRC3	AFRC2	AFRC1	AFRC0	AFFF	AFEF		AFWC4	AFWC3	AFWC2	AFWC1	AFWC0
Flags			Alignment FIFO Read Word Count					Flags			Alignment FIFO Write Word Count				
Input Elastic Buffer								Output Elastic Buffer							

Here:

- AFRC [4:0] = 0...31 – Input Alignment FIFO Read Word Count;
- AFWC [4:0] = 0...31 – Output Alignment FIFO Write Word Count;
- AFFF – Alignment FIFO Full Flag: AFWC = 31 or AFRC = 31;
- AFEF – Alignment FIFO Empty Flag.

CSR_AFD - Alignment FIFO Delay

Front FPGA

In the FRONT_FPGA this read/write register controls delaying of the AF read enable signal after an L1 Reset occurs. In fact, the total delay calculates as (96 + CSR_AFD Value) bunch crossings after an L1 Reset. The register is adjusted to minimize the overall MPC-to-SP data-path latency budget or during the SP link loop back tests.

Table 38: CSR_AFD Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	AFD6	AFD5	AFD4	AFD3	AFD2	AFD1	AFD0
									Alignment FIFO Delay						

Here:

- X – don't care bit for writes and zero for reads
- AFD [6:0] = 0…127 – AF resumes reads on the (96+1... 96+127) bunch crossing after an L1 Reset has been received. The register default value on power-up is 112, which gives the default delay of 208 bunch crossings.

SP FPGA

In the SP_FPGA this read/write register controls the DT-to-SP data-path latency with MBAF settings for DT muons and Front_FPGA-to-SP_FPGA data-path latency with MEAF settings for CSC muons. The latencies are updated on either an AF reset command, see the ACT_XFR register description for detail, or on any write command to this register.

Table 39: CSR_AFD Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	MEAF2	MEAF1	MEAF0	X	X	X	X	MBAF3	MBAF2	MBAF1	MBAF0
					ME Alignment FIFO							MB Alignment FIFO			

Here:

- X – don't care bit for writes and zero for reads;
- MBAF [3:0] = 0…15 – additional delay for DT muons in bunch crossings. The register default value on power-up is 0;
- MEAF [2:0] = 0…7 – additional delay for CSC muons in bunch crossings. The register default value on power-up is 0.

CSR_BID – Board Identifier Register

VME FPGA and SP FPGA

This read-only register in the VME_FPGA and SP_FPGA keeps a SP02/SP04/SP05 or SP02_MC/SP04_MC board ID. For SP02 and SP02_MC boards the BRD_ID is always zero.

Table 40: CSR_BID Data Format for VME_FPGA and SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	BRD_VER[2:0]			0	0	BRD_ID[5:0]					

Here:

- BRD_VER [2:0] = {2, 4} Boards Version: SP02 or SP04/SP05
- BRD_ID [5:0] = 1…31 Board number.

Front FPGA

This read-only register in the FRONT_FPGA keeps a MPC Link Identifier. On power-up the register defaults to all zeros. After an MPC-to-SP optical link has been successfully initialized by the TTC_L1RES command, the register keeps the MPC/Link number. Note, that the Link Number is hardware coded, while the MPC number is a value downloaded in the MPC CSR0 register. During TLK2501 loop back tests bit[15] = 1, Mx [1:0] (x=1,2,3) is a muon number, and Fy [2:0] (y=1,2,3,4,5) is a FRONT_FPGA number.

Table 41: CSR_BID Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	MPC_LINK_ID [7:0]							
								MPC # [5:0]						LINK # [1:0]	
During SP Loop Back Tests															
1	0	0	0	0	0	0	0	0	Fy			0	0	Mx[1:0]	

Here for MPC-to-SP links:

- MPC_LINK_ID [7:0] - MPC Link Identifier consists of:
  - LINK # [1:0] = 0 (default), 1,2,3 – MPC Link number;
  - MPC # [5:0] = 0 (default)…63 – MPC Crate number.

DDU FPGA

In the DDU_FPGA this downloadable register keeps information on the CSC side and sector number serviced by the SP and the SP current slot number. This data is passed to the DDU in the SP Event Record Header for unique identification of the readout stream.

Table 42: CSR_BID Data Format for DDU_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	SP_LADR [3:0]				X	X	X	SP_PADR [4:0]				
				MEZ	MES _ID [2:0]										

Here:

- X – Don't care bit, reads back as zero;
- SP_LADR [3:0] – SP Logical Address consists of:
  - MEZ = 0 (-Z) / 1 (+Z) – EMU Side;
  - MES_ID [2:0] – EMU 60° Sector number;
- SP_PADR [4:0] = 6…11, 16…21 – SP Physical Address.

CSR_BSY – Busy Control / Status

In the VME_FPGA the CSR_BSY register displays status of seven input and one output BSY lines. Besides, it carries eight mask bits, so each input or/and the VME_FPGA output can be either disabled or enabled:

BSY0 = (BSY1*BSC1 + BSY2*BSC2 + BSY3*BSC3 + BSY4*BSC4 + BSY5*BSC5 + BSY6*BSC6 + BSY7 *BSC7 + BSY0_INT) * BSC0

Indexes 0…7 stand for chip numbers; see Table 8 and/or Table 45 for chip numbering scheme, and BSY0_INT is an internal busy status o the VME_FPGA, which is "1" when counting of CCB_L1ACCs is stopped (disabled).

The FRONT_FPGA sets BSY to "1", when either the BXN carries 0xDEC=4095 value, or link resynch on CCB_L1RES failed (the AF word count remains zero).

Table 43: CSR_BSY Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
BSM7	BSM6	BSM5	BSM4	BSM3	BSM2	BSM1	BSM0	BSY7	BSY6	BSY5	BSY4	BSY3	BSY2	BSY1	BSY0	R
BSM7	BSM6	BSM5	BSM4	BSM3	BSM2	BSM1	BSM0	X	X	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- BSM [7:0] – Busy Chip mask for SP, DD, F5…F1, and VM chips;
- BSY [7:0] – Busy status for SP, DD, F5…F1, and VM chips.

CSR_CFG – FPGA Configuration Done Status

Addressing to this read-only register allows verifying the Configuration Done status of the FRONT_FPGAs, DDU_FPGA, and SP_FPGA after hard resets. The register address is applicable to the VME_FPGA only. Register's default value is 0xFE, when all chips, including the mezzanine card's chip, are in place. Being Low during configuration, Configuration Done High indicates completion of the configuration.

To make sure all FPGA chips are present on board, the CSR_CFG command should be executed twice: first, when chips are engaged in the configuration process, i.e. immediately after the ACT_HR command, and second, after a 5 sec pause, when the configuration is definitely completed. If there is a missing FPGA chip on board (a mezzanine card not installed, for example), then the corresponding Configuration Done line remains floating, and could be sensed by the VME_FPGA either as a logic ONE or logic ZERO. But in any case, Configuration Done line for a missing chip would retain its state, while the one for a successfully configured FPGA will be LOW on the first read and HIGH on the second read.

Table 44: CSR_CFG Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	CFG7	CFG6	CFG5	CFG4	CFG3	CFG2	CFG1	0
								Configuration Done Status							

Here:

- CFG [7:1] = 0xFE (default) – Configuration Done Status bits for the SP, DD, F5, F4, F3, F2, and F1 FPGAs accordingly.

CSR_CID – Chip Identifier Register

This read-only register keeps a firmware release date in the format shown in the table below. Register address is applicable to all FPGAs.

Table 45: CSR_CID Data Format for all FPGAs

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
YY				MM				NN				DD			

Here:

- DD – Day Code (01…31);
- NN – FPGA Number (0...7), which corresponds to 8 FPGA chips, numbered in the following order: VM, F1, F2, F3, F4, F5, DD, SP;
- MM – Month Code (01…12);
- YY – Year Code (00…15) = Year - 2000.

CSR_CM1 – System Clock Manager 1 Status

This read-only register keeps history of Digital Clock Manager 1 behavior after the last ACT_CMR command. Its default value is 0x0004, which means that all enabled DCM1 features locked and there were no errors since last reset. DCM1 is a DCM with internal feedback, distributing the 40.078 MHz system clock in the chip.

Table 46: CSR_CM1 Data Format for all FPGAs

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LCK1 Counter				CST1 Counter				0	0	0	0	0	LCK1	CST1	PSO1

Here:

- PSO1 – Phase Shift Overflow, should be LOW for normal operation;
- CST1 – Input Clock Stopped Toggling;
- CST1 Counter is a "loss of input clock" counter. It counts "CST1 goes HIGH" occurrences after the last DCM1 reset. The counter stops when it reaches its maximum value of 15;
- LCK1 – All enabled DCM features locked;
- LCK1 Counter is a "loss of lock" counter. It counts "LCK1 goes LOW" occurrences after the last DCM1 reset. The counter stops when it reaches its maximum value of 15.

CSR_CM2 – System Clock Manager 2 Status

This read-only register keeps history of Digital Clock Manager 2 behavior after the last ACT_CMR command. Its default value is 0x0004, which means that all enabled DCM2 features locked and there were no errors since last reset. For the VME_FPGA, DCM2 is a DCM with external feedback, distributing system clock all over the board. For the FRONT_FPGA, DDU_FPGA and SP_FPGA, the DCM2 distributes the 80.156 MHz clock in the chip.

Table 47: CSR_CM2 Data Format for all FPGAs

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LCK2 Counter				CST2 Counter				0	0	0	0	0	LCK2	CST2	PSO2

Here:

- PSO2 – Phase Shift Overflow, should be LOW for normal operation;
- CST2 – Input Clock Stopped Toggling;
- CST2 Counter is a "loss of input clock" counter. It counts "CST2 goes HIGH" occurrences after the last DCM2 reset. The counter stops when it reaches its maximum value of 15;
- LCK2 – All enabled DCM features locked;
- LCK2 Counter is a "lost of lock" counter. It counts "LCK2 go LOW" occurrences after the last DCM2 reset. The counter stops when it reaches its maximum value of 15.

CSR_DF – DAQ FIFO Status

This read-only register shows the number of words currently loaded to the DAQ FIFO (DF) and link error status for muon data words. The maximum available DF capacity is 8192 18-bit words. Register address is applicable to DDU_FPGA.

Table 48: CSR_DF Data Format for DDU_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DFFF	DFEF	DFC13	DFC12	DFC11	DFC10	DFC9	DFC8	DFC7	DFC6	DFC5	DFC4	DFC3	DFC2	DFC1	DFC0
Flags			DAQ FIFO Word Count												

Here:

- DFC [13:0] = 0…8192 – DAQ FIFO Word Count;
- DFFF – Pipeline FIFO Full Flag or DFC = 8192;
- DFEF – Pipeline FIFO Empty Flag;

CSR_DFC – DAQ FIFO Configuration

This read/write register keeps the DDU Event Configuration word that includes: a number of time bins to readout, a zero suppression option, and mask bits for FRONT_FPGA LCTs, drift tube stubs and sector processor outputs. The register default value on power-up is 0x7FC.

The DDU_FPGA provides for two readout modes: via the fiber and DDU and via the DAQ FIFO and VME interface. By default the readout mode is set to DDU. Readout via the VME interface is still available, but the DAQ FIFO behaves as a spy on the readout path: it gets next event only if is has enough room to store it without truncation. The WOF and BSY signals are solely determined by the L1A FIFO word count.

If the readout mode is set to VME, then the WOF and BSY signals become determined by the DAQ FIFO word count as well. So, the trigger throttling is still available.

Note, that the register setting neither enables/disables the actual input/output data streams, nor affects the SP core functionality in any way. What it does – it only instructs the DDU_FPGA on how it should collect information and build the Event Record.

Table 49: CSR_DEC Data Format for DDU_FPGA.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DDM	X	X	X	X	SPA	DTA	F5A	F4A	F3A	F2A	F1A	ZS	TBIN2	TBIN1	TBIN0
Readout Mode	Spare				SP Active	DT Active	FRONT_FPGA Active bits					ZS	TBIN [2:0]		

Here:

- X – Don't care bit for writes and zero for reads;
- DDM = 0 (default) / 1 – DDU (default) / VME readout mode; The difference between the two modes is that by default the DD_FPGA FMM state machine monitors occupancy of either the L1A FIFO only or both L1A FIFO and DAQ FIFO. In the latter case the FMM outputs can throttle down the L1A rate, so it gets adjusted to the throughput of the VME readout interface, which is much slower, than the DDU one.
- F5A… F1A = 0 / 1 (default) – FRONT_FPGA Active bits. If the bit is set to 1, then the corresponding FRONT_FPGA is considered to be ACTIVE and is queried for CSC muon LCT(s);
- DTA = 0 / 1 (default) – Drift Tube Active. If the bit is set to 1, then the Drift Tube interface is considered to be ACTIVE and the SP_FPGA is queried for DT muon Stub(s);
- SPA = 0 / 1 (default) – Sector Processor Active. If the bit is set to 1, then the Sector Processor output is considered to be ACTIVE and the SP_FPGA is queried for SP muon Track(s);
- ZS = 0 / 1 (default) – Zero Suppression bit. If set to 1, then only valid LCT(s), Stub(s) and Track(s) are collected;

– TBIN [2:0] = 0…7 (default = 4) – DDU_FPGA collects data from 0…7 Time Bins (bunch crossings).

CSR_INI – FPGA Init Status

Addressing to this read-only register allows verifying the INIT_B pin status of the FRONT_FPGAs, DDU_FPGA, and SP_FPGA after hard resets. The register address is applicable to the VME_FPGA only. The default register value is 0xFE. INIT_B Low indicates memory is being cleared. The INIT_B pin transitions HIGH when the clearing of configuration memory is complete. INIT_B LOW during configuration indicates an error.

Table 50: CSR_INI Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	INI7	INI6	INI5	INI4	INI3	INI2	INI1	0
								Init_B Status							

Here:

– INI [7:1] = 0xFE (default) – Init_B Status bits for the SP, DD, F5, F4, F3, F2, and F1 FPGAs accordingly.

CSR_FCC – Fast Control Configuration / Status

VME FPGA

This read/write register sets the SP fast control modes and shows the status of the L1Accept control state machine. The FCM bit switches the source of fast control commands, which could be either from the local VME interface (default on power-up), or from the CCB over the TF crate backplane. The FCL bit controls the source for the internal FC_L1ACC signal. The source can be either a backplane CCB_L1ACC signal (default), or a fake signal, generated on every FC_SFRUN to facilitate debugging of the readout logic. The feature is used for validation of the readout process in the SP. The SP should be in a L1_RUN state to let a fake L1 Accept pass through the l1 accept enable/disable logic. The FCLCT bit controls if Local Charged Triggers (LCT) from the SP_FPGA are being sent to the backplane. The LCT is defines as Mode > 0 for the SP core output. The L1Accept state machine is one-hot coded, so only one state bit could be equal to logical 1 at any time. For further details on the L1Accept state machine see Figure 1. There is also a copy of the L1Accept state machine in every other FPGAs, which is used for gating the Valid Pattern Counters.

Table 51: CSR_FCC Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
RDY	BSY	OSY	WOF	0	0	0	FCM	0	0	FCL	FCLCT	0	L1R	L1W	L1S	R
X	X	X	X	X	X	X	FCM	X	X	FCL	FCLCT	X	X	X	X	W

Here:

– X – Don’t care bit;
– RDY = 1 – FMM state machine is in Ready state;
– BSY = 1 – FMM state machine is in Busy state;
– OSY = 1 – FMM state machine is in Out-of-Synch state;
– WOF = 1 – FMM state machine is in Warning-OverFlow state;
– FCM = 0 / 1 (default) – Fast Control Mode set to CCB / VME (default);

- FCL = 0 (default) / 1 – CCB/VME_L1ACC (default) / FC_SFRUN is a source for the FC_L1ACC signal, see the CSR_SFC register description for details on FC_SFRUN.
- FCLCT = 0 (default) /1 – disable (default) / enable Local Charge Trigger;
- L1S = 1 – L1Accept state machine is in the L1A_STOP state;
- L1W = 1 – L1Accept state machine is in the L1A_WAIT state;
- L1R = 1 – L1Accept state machine is in the L1A_RUN state.

Front FPGA, SP FPGA and DDU FPGA

In the Front FPGA, SP FPGA or DDU FPGA this read-only register returns current state of the L1Acept Finite State Machine and FMM Finite State Machine.

Table 52: CSR_FCC Data Format for FRONT_FPGA, SP_FPGA and DDU_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
RDY	BSY	OSY	WOF	0	0	0	0	0	0	0	0	0	L1R	L1W	L1S	R
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- RDY = 1 – FMM state machine is in Ready state;
- BSY = 1 – FMM state machine is in Busy state;
- OSY = 1 – FMM state machine is in Out-of-Synch state;
- WOF = 1 – FMM state machine is in Warning-OverFlow state;
- L1S = 1 – L1A_STOP state of the L1Accept state machine;
- L1W = 1 – L1A_WAIT state of the L1Accept state machine;
- L1R = 1 – L1A_RUN state of the L1Accept state machine.

CSR_HR – Hard Reset Mask

In the VME_FPGA the CSR_HR register masks the CCB Hard Reset signal. By default the CCB hard reset (soft reset for VM) is disabled for all SP chips.

Table 53: CSR_HR Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	HRM7	HRM6	HRM5	HRM4	HRM3	HRM2	HRM1	SRM0

Here:

- X – Don't care bit, reads back as zero;
- HRM [7:1] = 0x00 (default) / 0x7F – Hard Reset mask for SP, DD, F5…F1 chips;
- SRM [0] = 0 (default) / 1 – Soft Reset mask for VM chip.

CSR_LF – L1 Accept FIFO Status

This read-only register shows the number of words currently loaded to the L1 Accept FIFO (LF) and FIFO Flags. The maximum available LF capacity is 512 words. Register address is applicable to FRONT_FPGA, SP_FPGA and DDU_FPGA.

Table 54: CSR_LF Data Format for FRONT_FPGA, SP_FPGA and DDU_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LFFF	LFEF	0	0	0	0	0	LFC8	LFC7	LFC6	LFC5	LFC4	LFC3	LFC2	LFC1	LFC0
Flags				L1 Accept FIFO Word Count											

Here:

- LFC [8:0] = 0…256 – L1 Accept FIFO Word Count;
- LFFF – L1 Accept FIFO Full Flag or LFC = 256;
- LFEF – L1 Accept FIFO Empty Flag.

CSR_LNK – Link Control/Status

This register provides static link control and status directly to and from both Finisar and TLK2501 transceivers' pins. Read-only upper byte shows receiver status, while lower byte provides access to control pins. Under the normal operational conditions register value equals to 0x0511 for a receiving link and equals to 0x0014 for a transmitting link. When TSEN is asserted High, results of pseudorandom bit stream tests can be monitored on the RXER output. A High on this terminal indicates that valid PRBS is being received. The PRBS test counter counts (RXER goes Low) events, when TSEN is High. It stops, when reaches its maximum value of 31. Counter reset is provided through addressing to the ACT_LER register.

When the TLK2501 device is disabled (DVEN is set to "0") the corresponding ready/busy link status is masked off and does not contribute to the overall FRONT_FPGA fast monitoring status.

Table 55: CSR_LNK Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
TEC4	TEC3	TEC2	TEC1	TEC0	RXDV	RXER	RXSD	0	TSEN	LPEN	DVEN	0	TXEN	TXER	TXDI	R
X	X	X	X	X	X	X	X	X	TSEN	LPEN	DVEN	X	TXEN	TXER	TXDI	W

Here:

- X – Don't care bit for writes;
- TXDI = 0 /1 (default) – enable / disable (default) the FINISAR optical Transmitter;
- {TXEN, TXER} = {Transmit Enable, Error Coding} – Transmit Data Control:
  - {TXEN,TXER} = {0,0} – Transmit Idle Character (0xC5BC or 0x50BC);
  - {TXEN,TXER} = {0,1} – Transmit Carrier Extend (0xF7F7);
  - {TXEN,TXER} = {1,0} – Transmit Normal Data Character -> default
  - {TXEN,TXER} = {1,1} – Transmit Error Propagation (0xFEFE);
- DVEN = 0 / 1 (default) – disable / enable (default) the TLK2501 Device;
- LPEN = 0 (default) / 1 – disable (default) / enable the TLK2501 Loop mode;
- TSEN = 0 (default) / 1 – disable (default) / enable the TLK2501 Pseudorandom Bit Stream (PRBS) Test ;
- RXSD = 0 / 1 – No Signal / Signal Detect from FINISAR optical receiver;
- { RXDV, RXER} = { Receive Data Valid, Receive Error} – Receive Status Signals
  - {RXDV, RXER} = {0,0} – Receive Idle Character (0xC5BC or 0x50BC);
  - {RXDV, RXER} = {0,1} – Receive Carrier Extend (0xF7F7);
  - {RXDV, RXER} = {1,0} – Receive Normal Data Character;
  - {RXDV, RXER} = {1,1} – Receive Error Propagation (0xFEFE);

– TEC [4:0] – PRBS Test Error Counter.

For the DDU_FPGA this register carries one extra bit, which for the SP defines link reference clock to be either a doubled RF clock of 80.1574MHz or an oscillator clock of 80.0000 MHz. For the SP02 this extra bit is irrelevant, since there is no auxiliary oscillator of 80.0000 MHz on this board. Note, that Transmit Idle Character is a default mode, which is a must for proper functioning of the DDU link. All other transmit modes are for testing only.

Table 56: CSR_LNK Data Format for DDU_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
TEC4	TEC3	TEC2	TEC1	TEC0	RXDV	RXER	RXSD	0	TSEN	LPEN	DVEN	TXCK	TXEN	TXER	TXDI	R
X	X	X	X	X	X	X	X	X	TSEN	LPEN	DVEN	TXCK	TXEN	TXER	TXDI	W

Here:

– X – Don't care bit for writes;
– TXDI = 0 (default) /1 – enable (default) / disable the FINISAR optical Transmitter;
– {TXEN, TXER} = {Transmit Enable, Error Coding} – Transmit Data Control:
  - {TXEN,TXER} = {0,0} – Transmit Idle Character (0xC5BC or 0x50BC) => default;
  - {TXEN,TXER} = {0,1} – Transmit Carrier Extend (0xF7F7);
  - {TXEN,TXER} = {1,0} – Transmit Normal Data Character;
  - {TXEN,TXER} = {1,1} – Transmit Error Propagation (0xFEFE);
– TXCK = 0 (default) / 1 – select 80.0000 MHz (default) / 80.1574 MHZ clock as a TLK2501 reference clock;
– DVEN = 0 / 1 (default) – disable / enable (default) the TLK2501 Device;
– LPEN = 0 (default) / 1 – disable (default) / enable the TLK2501 Loop mode;
– TSEN = 0 (default) / 1 – disable (default) / enable the TLK2501 Pseudorandom Bit Stream (PRBS) Test ;
– RXSD = 0 / 1 – No Signal / Signal Detect from FINISAR optical receiver;
– { RXDV, RXER} = { Receive Data Valid, Receive Error} – Receive Status Signals
  - {RXDV, RXER} = {0,0} – Receive Idle Character (0xC5BC or 0x50BC);
  - {RXDV, RXER} = {0,1} – Receive Carrier Extend (0xF7F7);
  - {RXDV, RXER} = {1,0} – Receive Normal Data Character;
  - {RXDV, RXER} = {1,1} – Receive Error Propagation (0xFEFE);
– TEC [4:0] – PRBS Test Error Counter.

CSR_MWC – MS Winners Configuration

This read/write register sets the SYS_CLK sampling phase for MS Winner bits and enables/disables the MS interface outputs; see the STS_MWA register description for details.

Table 57: CSR_MWC Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
MSD	0	0	0	0	0	0	0	0	0	0	0	0	MWP2	MWP1	MWP0	R
MSD	X	X	X	X	X	X	X	X	X	X	X	X	MW Phase [2:0]			W

Here:

– X – Don't care bit;
– MWP [2:0] = 0…7, 2 – default, the SYS_CLK Sampling Phase for MS Winners;

– MSD = 0 / 1(default) – enable / disable (default) MS interface outputs.

CSR_OSY – Out-of-Synch Control / Status

In the VME_FPGA the CSR_OSY register displays status of seven input and one output OSY lines. Besides, it carries eight mask bits, so each input or/and output can be either disabled (mask bit = 0) or enabled (mask bit = 1 => default):

OSY0 = (OSY1*OSM1 + OSY2*OSM2 + OSY3*OSM3 + OSY4*OSM4 + OSY5*OSM5 + OSY6*OSM6 + OSY7 *OSM7) * OSM0

Indexes 0…7 stand for chip numbers; see Table 8 and/or Table 45 for chip numbering scheme. By default all masks are set to enable state.

Table 58: CSR_OSY Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
OSM7	OSM6	OSM5	OSM4	OSM3	OSM2	OSM1	OSM0	OSY7	OSY6	OSY5	OSY4	OSY3	OSY2	OSY1	OSY0	R
OSM7	OSM6	OSM5	OSM4	OSM3	OSM2	OSM1	OSM0	X	X	X	X	X	X	X	X	W

Here:

– X – Don't care bit;
– OSM [7:0] – Out-of-Synch Chip mask for SP, DD, F5…F1 and VM chips;
– OSY [7:0] – Out-of-Synch status for SP, DD, F5…F1 and VM chips.

In the FRONT_FPGA each link has a Bunch Crossing Counter (BXN) associated with it, which is controlled by both the L1 Accept FSM and link bc0 mark. When the FSM is in L1_STOP state the BXN is preset to a 0xDEC value. The BXN starts counting from one and up on a first bc0 mark it gets from the link after the FSM moved on from L1_STOP state. From this moment on the monitor logic continuously compares BC0 and BXN0 marks coming from the link against the BXN zero state and the BXN[0] accordingly. Any mismatch found sets an error bit: mismatch in BC0 sets a BCE bit and mismatch in BXN0 sets a BXE bit. Once set, the error bit holds ONE until fast control command puts the FSM into L1_STOP state again. On this transition, errors accumulated during L1_RUN state get stored into BCR and BXR bits, while BCE and BXE bits are reset to zero.

One more BXN monitors the CCB timing. The logic of operation is very similar to that of link counters, except that it starts counting on FC_BC0 command and monitors only FC_BC0 timing marks.

All bits are reset on power-up and FC_L1RES command.

Table 59: CSR_OSY Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
BCR3	BXR3	BCE3	BXE3	BCR2	BXR2	BCE2	BXE2	BCR1	BXR1	BCE1	BXE1	BCR0	0	BCE0	0	R
M3 Link Timing Monitor				M2 Link Timing Monitor				M1 Link Timing Monitor				CCB Timing Monitor				W

Here:

– X – Don't care bit;
– BXE [3:1] – BXN0 out-of-synch condition detected during current run;
– BCE [3:0] – BC0 / FC_BC0 out-of-synch condition detected during current run;
– BXR [3:1] – BXN0 out-of-synch condition detected during previous run;
– BCR [3:0] – BC0 / FC_BC0 out-of-synch condition detected during previous run;

In the DDU_FPGA the CSR_OSY register carries Out-of-Synch status for the SP_FPGA and FRONT_FPGAs. During readout process of each event the DDU_FPGA queries other FPGAs for their bunch counter and event counter values, compares them against templates and sets out-of-synch flags, if the comparison fails. The SP_FPGA provides a template for the bunch counter comparison, and the DDU_FPGA provides a template for the event counter comparison.

Table 60: CSR_OSY Data Format for DDU_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
OSE7	0	OSE5	OSE4	OSE3	OSE2	OSE1	0	0	0	OSB5	OSB4	OSB3	OSB2	OSB1	0	R

Here:

- OSE [7:1] – SP_FPGA and FRONT_FPGA Event Counter Out-of-Synch bits;
- OSB [5:1] – FRONT_FPGA Bunch Counter Out-of-Synch bits.

CSR_REQ – L1 Request Mask

This read/write register allows choosing the source for the L1 request signal, being sent by the SP to the backplane. Normally, the L1 Request is an OR of tracks with none-zero Mode, found by the SP core logic. The user can also chose the L1 Request to be generated on an OR of Valid Pattern bit occurrence for enabled CSC muons.

Table 61: CSR_REQ Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CORE	ME4C	ME4B	ME4A	ME3C	ME3B	ME3A	ME2C	ME2B	ME2A	ME1F	ME1E	ME1D	ME1C	ME1B	ME1A
L1 Request Enable [15:0]															

Here:

- ME1A…ME4C = 0 (default) /1 – Disable (default) / Enable VP-bit of ME1A…ME4C to be a source of L1 Request;
- CORE = 0 / 1 (default) – Disable / Enable (default) none-zero Mode output of the SP core to be a source of L1 Request.

CSR_LEC – Link Error Counters

This read-only register monitors all possible link errors. The TLK2501 synchronization procedure, when the MPC switches TLK2501 transmitters into idle mode for 128 bunch crossings, always precedes the normal operation. Normal receiving operation assumes RXSD and RXDV to be High and RXER to be Low. To facilitate monitoring of error conditions, any combination of RXSD, RXDV and RXER other than normal is detected and countered. Error conditions are accumulated over time, starting from the previous synchronization procedure. Counter stops when it reaches its maximum value. The counters are reset on L1_Reset and begin count errors after Alignment FIFO has been enabled for writing. Addressing the ACT_LER register provides an alternative reset option.

Table 62: CSR_LEC Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SLC3	SLC2	SLC1	SLC0	CEC3	CEC2	CEC1	CEC0	EWC7	EWC6	EWC5	EWC4	EWC3	EWC2	EWC1	EWC0
Signal Loss Counter				Carrier Extend Counter				Error Word Counter							

Here:

- EWC [7:0] – TLK2501 Error Word Counter (RXDV == High, RXER == High);

- CEC [3:0] – TLK2501 Carrier Extend Counter (RXDV == Low, RXER == High);
- SLC [3:0] – FINISAR optical receiver Signal Loss Counter (RXSD goes Low).

CSR_PF – Pipeline FIFO Status

This read-only register shows the number of words currently loaded to the Pipeline FIFO (PF) and FIFO Flags. The maximum available PF capacity is 512 72-bit words. Since the Pipeline FIFO runs at the doubled RF frequency, its word count equals to (PFD +1) * 2, where PFD is a CSR_PFD register setting. Register address is applicable to FRONT_FPGA. The PF content is not available for direct reads. Use Spy FIFO to grab data of interest at the SF inputs or outputs.

Table 63: CSR_PF Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PFFF	PFEF	0	0	0	0	PFC9	PFC8	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0
Flags						Pipeline FIFO Word Count									

Here:

- PFC [9:0] = 0…512 – Pipeline FIFO Word Count;
- PFFF – Pipeline FIFO Full Flag or PFC = 512;
- PFEF – Pipeline FIFO Empty Flag.

CSR_QDB – QPLL Daughter Board Control/Status

This register sets the Daughter Board QPLL (DB_QPLL) mode of operation and returns the DB_QPLL locked status and loss of lock history since the last QPLL reset signal, see ACT_CMR – Clock Manager Reset description for details. The SP02 version lacks the DB_QPLL, but has a QPLL patch installed and a “QPLL locked” detector implemented in the VME_FPGA logic; the QPLL mode control bits are not applicable to the SP02 version, but write access to the register is available for compatibility with SP04.

Table 64: CSR_QDB Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DB_LLCK Counter				TTCrq_LLCK Counter				0	0	CTL1	CTL0	0	LCKQ	LCKD	RDY

Here:

- RDY is a read-only CCB_RDY status (TTCrx/TTCrq ASIC is ready for operation);
- LCKD is a read-only CCB_LCKD status (TTCrq QPLL is locked);
- LCKQ is a read-only DB_QPLL locked status (SP Daughter Board QPLL is locked);
- CTL[1:0] is a QPLL mode control:
  CTL = 2 => QPLL as a Standalone Clock Generator;
  CTL = 1 (default) => QPLL runs a Frequency Calibration Cycle on /Reset and Loss of Lock;
  CTL = 0 => QPLL runs a Frequency Calibration Cycle on /Reset only;
- TTCrq_LLCK Counter is a “loss of lock” counter. It counts “TTCrq_LOCKED goes LOW” occurrences after the last counter reset. The counter stops when it reaches its maximum value of 15.

– DB_LLCK Counter is a “loss of lock” counter. It counts “DB_LOCKED goes LOW” occurrences after the last counter reset. The counter stops when it reaches its maximum value of 15.

CSR_RBR – Ring Buffer Read Pointer

This read-only register shows the current position of the Ring Buffer Read Pointer. Ring Buffer is a 2048 word temporary storage for muon data, before they are get reformatted and put in the DAQ FIFO for readout. The register is valid for FRONT_FPGA and SP_FPGA and used for firmware debugging.

Table 65: CSR_RBR Data Format for FRONT_FPGA and SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	RBR10	RBR9	RBR8	RBR7	RBR6	RBR5	RBR4	RBR3	RBR2	RBR1	RBR0
					Ring Buffer Read Pointer Address										

Here:

– RBR [10:0] = 0…2047 – Ring Buffer Read Pointer.

CSR_RBW – Ring Buffer Write Pointer

This read-only register shows the current address of the Ring Buffer Write Pointer. Ring Buffer is 2048-word temporary storage for muon data, before they are get reformatted and put in the DAQ FIFO for readout. The register is valid for FRONT_FPGA and SP_FPGA and used for firmware debugging.

Table 66: CSR_RBW Data Format for FRONT_FPGA and SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	RBW10	RBW9	RBW8	RBW7	RBW6	RBW5	RBW4	RBW3	RBW2	RBW1	RBW0
					Ring Buffer Write Pointer Address										

Here:

– RBW [10:0] = 0...2047– Ring Buffer Write Pointer Address.

CSR_RDY – Ready Control / Status

In the VME_FPGA the CSR_RDY register displays status of seven input and one output RDY lines. Besides, it carries eight mask bits, so each input or/and VME_FPGA output can be either disabled or enabled:

RDY0 = (RDY1*RDM1 + RDY2*RDM2 + RDY3*RDM3 + RDY4*RDM4 + RDY5*RDM5 + RDY6*RDM6 + RDY7 *RDM7) * RDY0_INT *RDM0

Indexes 0…7 stand for chip numbers; see Table 8 and/or Table 45 for chip numbering scheme, and RDY0_INT is an internal ready status of the VME_FPGA, which is “1” when passing of CCB_L1ACCs to the FC bus is enabled.

The FRONT_FPGA sets RDY to “1”, when link resynchronization initiated by CCB_L1RES completed a success (the Alignment FIFO is neither empty, nor full). Only links with enabled TLK2501 receivers contribute to the chip’s RDY status; see the CSR_LNK register for a DVEN bit description.

Table 67: CSR_RDY Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
RDM7	RDM6	RDM5	RDM4	RDM3	RDM2	RDM1	RDM0	RDY7	RDY6	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0	R
RDM7	RDM6	RDM5	RDM4	RDM3	RDM2	RDM1	RDM0	X	X	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- RDM [7:0] – Ready Chip mask for SP, DD, F5…F1, and VM chips;
- RDY [7:0] – Ready status for SP, DD, F5…F1, and VM chips.

CSR_SID – SP Core Identifier Register

This SP_FPGA read-only register keeps an SP core code release date in the following format:

Table 68: CSR_SID Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
YY				MM				1	1	1	DD				

Here:

- DD – Day Code (01…31);
- MM – Month Code (01…12);
- YY – Year Code (00…15) = Year - 2000.

CSR_SF – Spy FIFO Status

This read-only register shows the number of words currently sitting in the Spy FIFO (SF). One would probably want to know this value before setting up the BLT read cycle to read out the SF content. Maximum available SF capacity is 1024 16-bit words. Register address is applicable to FRONT_FPGA (3 each), DDU_FPGA (1 each) and SP_FPGA (11 each).

Table 69: CSR_SF Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFFF	SFEF	RXDV	RXER	0	SFC10	SFC9	SFC8	SFC7	SFC6	SFC5	SFC4	SFC3	SFC2	SFC1	SFC0
Flags		RX Status			Spy FIFO Word Count										

Here:

- SFC [10:0] = 0..1024 – Spy FIFO Word Count;
- SFFF – Spy FIFO Full Flag or 1024 Word Count;
- SFEF – Spy FIFO Empty Flag;
- RXDV, RXER – TLK2501 Receiver Status for the last data read out from the Spy FIFO.

CSR_SF1 – F1 Spy FIFO Status

This read-only registers, one register per F1 EMU muon, return the F1 Spy FIFO (SF1) Flags and the SF1 Word Count. The maximum available SF1 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA only.

Table 70: CSR_SF1 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF1FF	SF1EF	0	0	0	SF1C10	SF1C9	SF1C8	SF1C7	SF1C6	SF1C5	SF1C4	SF1C3	SF1C2	SF1C1	SF1C0
Flags					F1 Spy FIFO Word Count										

Here:

- SF1C [10:0] = 0…1024 – F1 Spy FIFO Word Count;
- SF1FF – F1 Spy FIFO Full Flag or SF1C = 1024;
- SF1EF – F1 Spy FIFO Empty Flag.

CSR_SF2 – F2 Spy FIFO Status

This read-only registers, one register per F2 EMU muon, return the F2 Spy FIFO (SF2) Flags and the SF2 Word Count. The maximum available SF2 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA only.

Table 71: CSR_SF2 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF2FF	SF2EF	0	0	0	SF2C10	SF2C9	SF2C8	SF2C7	SF2C6	SF2C5	SF2C4	SF2C3	SF2C2	SF2C1	SF2C0
Flags					F2 Spy FIFO Word Count										

Here:

- SF2C [10:0] = 0…1024 – F2 Spy FIFO Word Count;
- SF2FF – F2 Spy FIFO Full Flag or SF2C = 1024;
- SF2EF – F2 Spy FIFO Empty Flag.

CSR_SF3 – F3 Spy FIFO Status

This read-only registers, one register per F3 EMU muon, return the F3 Spy FIFO (SF3) Flags and the SF3 Word Count. The maximum available SF3 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA only.

Table 72: CSR_SF3 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF3FF	SF3EF	0	0	0	SF3C10	SF3C9	SF3C8	SF3C7	SF3C6	SF3C5	SF3C4	SF3C3	SF3C2	SF3C1	SF3C0
Flags					F3 Spy FIFO Word Count										

Here:

- SF3C [10:0] = 0…1024 – F3 Spy FIFO Word Count;
- SF3FF – F3 Spy FIFO Full Flag or SF3C = 1024;
- SF3EF – F3 Spy FIFO Empty Flag.

CSR_SF4 – F4 Spy FIFO Status

This read-only registers, one register per F4 EMU muon, return the F4 Spy FIFO (SF4) Flags and the SF4 Word Count. The maximum available SF4 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA only.

Table 73: CSR_SF4 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF4FF	SF4EF	0	0	0	SF4C10	SF4C9	SF4C8	SF4C7	SF4C6	SF4C5	SF4C4	SF4C3	SF4C2	SF4C1	SF4C0
Flags					F4 Spy FIFO Word Count										

Here:

- SF4C [10:0] = 0…1024 – F4 Spy FIFO Word Count;
- SF4FF – F4 Spy FIFO Full Flag or SF4C = 1024;
- SF4EF – F4 Spy FIFO Empty Flag.

CSR_SF5 – F5 Spy FIFO Status

This read-only registers, one register per F5 EMU muon, return the F5 Spy FIFO (SF5) Flags and the SF5 Word Count. The maximum available SF5 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA only.

Table 74: CSR_SF5 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF5FF	SF5EF	0	0	0	SF5C10	SF5C9	SF5C8	SF5C7	SF5C6	SF5C5	SF5C4	SF5C3	SF5C2	SF5C1	SF5C0
Flags					F5 Spy FIFO Word Count										

Here:

- SF5C [10:0] = 0…1024 – F5 Spy FIFO Word Count;
- SF5FF – F5 Spy FIFO Full Flag or SF5C = 1024;
- SF5EF – F5 Spy FIFO Empty Flag.

CSR_SFE – EMU Spy FIFO Status

This read-only register, common for all EMU muons, returns the FE Spy FIFO (SFE) Flags and the SFE Word Count. The maximum available SFE capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA.

Table 75: CSR_SFE Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFEFF	SFEEF	0	0	0	SFEC10	SFEC9	SFEC8	SFEC7	SFEC6	SFEC5	SFEC4	SFEC3	SFEC2	SFEC1	SFEC0
Flags					FE Spy FIFO Word Count										

Here:

- SFEC [10:0] = 0…1024 – FE Spy FIFO Word Count;
- SFEFF – FE Spy FIFO Full Flag or SFEC = 1024;
- SFEEF – FE Spy FIFO Empty Flag.

CSR_SFC – Spy FIFO Configuration

VME FPGA

In the VME_FPGA this register defines the delay inserted between the CCB test commands and the FC_SFRUN command on the internal FC bus, see Table 2. The delay is intended to compensate for the time required for the corresponding test data to reach the Spy FIFO input. The delay is not applicable to the CCB_L1ACC command. The register also

determines if the request for data is one-time or persistent. The power-up default state for this register is 0x0000.

Table 76: CSR_SFC Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFM	SFRL	SFRS	SFRM	SFRT	SFRB	SFD9	SFD8	SFD7	SFD6	SFD5	SFD4	SFD3	SFD2	SFD1	SFD0
Mode	Spy FIFO Requests					Spy FIFO Delay Setting									

Here:

- X – don't care bit for writes and zero for reads;
- SFD [9:0] = 0 (default)…1023 - Spy FIFO starts writing data, when 1…1024 bunch crossings have passed after the requested event;
- SFRB = 0 (default) /1 – don't store (default) / store data on the next CCB_BC0 timing mark and treat CCB_BC0 as a CCB_TPSP command.
- SFRT = 0 (default) /1 – don't store (default) / store data on the next CCB_TPTMB command;
- SFRM = 0 (default) /1 – don't store (default) / store data on the next CCB_TPMPC command;
- SFRS = 0 (default) /1 – don't store (default) / store data on the next CCB_TPSP command;
- SFRL = 0 (default) /1 – don't store (default) / store data on the next CCB_L1ACC command;
- SFM = 0 (default) /1 – one-time (default) / persistent request. One-time request stores data on the next event only and self-resets after that. Persistent request stores data on all events that follow.

Front FPGA

In the FRONT_FPGA this register defines the data source for the Spy FIFO input and the number of beam crossings to be stored upon receiving the FC_SFRUN command. Note that the actual number of 16-bit words, saved in the Spy FIFO is twice as big, since each beam crossing data consists of two frames.

Table 77: CSR_SFC Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFS	X	X	X	X	X	X	SFW8	SFW7	SFW6	SFW5	SFW4	SFW3	SFW2	SFW1	SFW0
Source							Spy FIFO Window								

Here:

- X – Don't care bit for writes and zero for reads;
- SFS = 0 (default) /1 – connects the Spy FIFO input to the Pipeline FIFO input (default) / output to grab data;
- SFW [8:0] = 0 (default)…511 – Spy FIFO Window: Spy FIFO grabs 2…1024 data frames from 1…512 bunch crossings on the next FC_SFRUN command. If the Spy FIFO grabs data from the Pipeline FIFO output, the Spy FIFO data format changes: the muon lct/stub data is preceded by the two header words carrying first data frame bunch crossing number and event counter, see the DAT_SF register description for details.

SP FPGA

Similar register in the SP_FPGA has two extra control bits that define data source exclusively for the DAT_SFM Spy FIFO.

Table 78: CSR_SFC Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFS	X	SFM1	SFM0	X	X	X	SFW8	SFW7	SFW6	SFW5	SFW4	SFW3	SFW2	SFW1	SFW0
Source		Data Source						Spy FIFO Window							

Here:

- X – Don't care bit for writes and zero for reads;
- SFS = 0 (default) / 1 – connects the Spy FIFO (DAT_SF), Barrel Spy FIFO (DAT_SFB) and MS Spy FIFO (DAT_SFM) inputs to the Pipeline FIFO input (default) / output to grab data.
- SFM [1:0] = 0, 1 (default), 2, 3 – MS Spy FIFO (DAT_SFM) does not spy or spies on the M1/DAT_PT (default), M2/DAT_PT or M3/DAT_PT output data;
- SFW [8:0] = 0 (default)…511 – Spy FIFO Window: Spy FIFO grabs 2 (default)…1024 data frames from 1 (default)…512 bunch crossings on the next FC_SFRUN command;

DDU FPGA

The Spy FIFO input in the DDU_FPGA can be connected either to the input of the TLK2501 Output Alignment FIFO or to the output of the TLK2501 Input Alignment FIFO. In either case the Spy FIFO grabs only the amount of data specified by SFW [9:0] value. It may happen, there has been no valid data in that time interval, and so in this case the Spy FIFO remains empty.

Table 79: CSR_SFC Data Format for DDU_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFS	X	X	X	X	X	SFW9	SFW8	SFW7	SFW6	SFW5	SFW4	SFW3	SFW2	SFW1	SFW0
Source						Spy FIFO Window									

Here:

- X – Don't care bit for writes and zero for reads;
- SFS = 0 (default) /1 – connects the Spy FIFO input to the TLK2501 transmitter input (default) / TLK2501 receiver output to grab data;
- SFW [9:0] = 0 (default)…1023 – Spy FIFO Window: Spy FIFO grabs 1 (default)…1024 data valid words on the next FC_SFRUN command.

CSR_PFD – Pipeline FIFO Data Delay

This read/write register controls data delay in the Pipeline FIFO to compensate for L1 Accept latency. Default value on power-up is 0.

Table 80: CSR_PFD Data Format for FRONT_FPGA and SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	PFD7	PFD6	PFD5	PFD4	PFD3	PFD2	PFD1	PFD0
								Pipeline FIFO Data Delay							

Here:

- X – Don't care bit for writes and zero bit for reads;
- PFD = 0…255 – PF delays data for 1... 256 bunch crossings or up to 6.4 μsec.

CSR_SCC – SP Core Configuration

This read/write register keeps the SP core configuration options.

This register is protected against accidental accesses: in order to get VME access to this register the SP should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two VME commands:

- VW/MA/CSR_FCC/W/0x0100 -> put the SP under the VME control
- VM/MA/ACT_FCC/W/0x00C8 -> issue a bx reset command

before addressing the data register.

Table 81: CSR_SCC Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	DTE	X	X	Q4EN	Q3EN	X	X	X	BXE

Here:

- X – Don't care bit for writes and zero for reads;
- BXE = 0 (default) / 1 – disable (default) / enable Bunch Crossing Analyzer;
- DTE = 0 (default) / 1 – disable (default) / enable Drift Tube data inputs to SP Core;
- Q3EN = 0 (default) / 1 – disable (default) / enable processing stubs with Quality = 3;
- Q4EN = 0 (default) / 1 – disable (default) / enable processing stubs with Quality = 4.

CSR_SFB – Barrel Spy FIFO Status

This read-only register, ne per MB input link, returns the Barrel Spy FIFO (SFB) Flags and the SFB Word Count. The maximum available SFB capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA.

Table 82: CSR_SFB Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFBFF	SFBEF	0	0	0	SFBC10	SFBC9	SFBC8	SFBC7	SFBC6	SFBC5	SFBC4	SFBC3	SFBC2	SFBC1	SFBC0
Flags					Barrel Spy FIFO Word Count										

Here:

- SFBC [10:0] = 0…1024 – MS Spy FIFO Word Count;
- SFBFF – MS Spy FIFO Full Flag or SFBC = 1024;
- SFBEF – MS Spy FIFO Empty Flag.

CSR_SFM – Muon Sorter Spy FIFO Status

This read-only register, one per SP output track, returns the MS Spy FIFO (SFM) Flags and the SFM Word Count. The maximum available SFM capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA.

Table 83: CSR_SFM Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFMFF	SFMEF	0	0	0	SFMC10	SFMC9	SFMC8	SFMC7	SFMC6	SFMC5	SFMC4	SFMC3	SFMC2	SFMC1	SFMC0
Flags					MS Spy FIFO Word Count										

Here:

- SFMC [10:0] = 0…1024 – MS Spy FIFO Word Count;
- SFMFF – MS Spy FIFO Full Flag or SFMC = 1024;
- SFMEF – MS Spy FIFO Empty Flag.

CSR_TBC – Transition Board Configuration

Front FPGA

F1 and F2 FPGAs deliver LCT data to the DT Track Finder via the Transition Board. The data format is described elsewhere. The CSR_TBC register has been added to provide with the SP05_TB configuration options in the firmware revision 051121 and later. Although all FRONT_FPGAs carry a copy of this register, only F2 actually uses the CSR_TBC control signals to configure the SP05_TB functionality.

The SP05_TB fans out F1 clock ME1ABC_DT_CLK and timing bits ME1ABC_DT_BC0, ME1ABC_DT_BX[1:0] to both TB output connectors, and uses F2 former clock and timing bits as Transition Board control signals to configure TB output and input modes of operation.

The SP05_TB output configuration options are:

- CSC-to-DT clock polarity selection; allows to register data at destination either by negative or positive going clock edge;
- Transparent or Registered CSC-to-DT data outputs.

The SP05_TB input configuration options are:

- Onboard loop-back any of the two CSC-to-DT outputs to the DT-to-CSC inputs for self-testing purposes instead of receiving barrel muons.
- DT-to-CSC clock polarity selection; selects either negative or positive going clock edge to register input DT data (this control bit is located in the SP_FPGA).

For compatibility with the old TB, a legacy bit has been added. When this bit is set to 1, the SP assumes working with an old TB.

Table 84: CSR_TBC Data Format for F2_FPGA.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	LEGS	PES	RGS	MBS	F2S
											TB Control				

Here:

- X – Don’t care bit for writes and zero for reads;
- F2S = 0 / 1 (default) – loop-back F1 / F2 (default) output data Select;
- MBS = 0 / 1 (default) – loop-back test / regular operation (default) may be chosen with a Barrel Muon Select bit;
- RGS = 0 / 1 (default) – transparent / Registered (default) data output Select;

- PES = 0 (default) / 1 – Negative (default) / Positive clock Edge Select for DT to register the CSC output data;
- LEGS = 0 (default) / 1 – SP05_TB (default) / Legacy TB Select.

SP FPGA

The SP FPGA should be configured to accept the loop-back test data from the Transition Board. The MBS bit controls switching between the regular operation and loop-back test modes.

Table 85: CSR_TBC Data Format for SP_FPGA.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	MBS	X

Here:

- X – Don't care bit for writes and zero for reads;
- MBS = 0 / 1 (default) – loop-back test / regular operation (default) with Barrel Muon Select bit.

CSR_TF – Test FIFO Status

This read-only register shows word count currently loaded into the Test FIFO (TF) and FIFO Flags. The maximum available TF capacity is 1024 16-bit words. Register address is applicable to FRONT_FPGA (3 each), DDU_FPGA (1 each) and SP_FPGA (11 each).

Table 86: CSR_TF Data Format for FRONT_FPGA, DDU_FPGA and SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFFF	TFEF	0	0	0	TFC10	TFC9	TFC8	TFC7	TFC6	TFC5	TFC4	TFC3	TFC2	TFC1	TFC0
Flags					Test FIFO Word Count										

Here:

- TFC [10:0] = 0...1024 – Test FIFO Word Count;
- TFFF – Test FIFO Full Flag or TFC = 1024;
- TFEF – Test FIFO Empty Flag.

CSR_TF1 – F1 Test FIFO Status

This read-only registers, one register per F1 EMU muon, return the F1 Test FIFO (TF1) Flags and the TF1 Word Count. The maximum available TF1 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA only.

Table 87: CSR_TF1 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF1FF	TF1EF	0	0	0	TF1C10	TF1C9	TF1C8	TF1C7	TF1C6	TF1C5	TF1C4	TF1C3	TF1C2	TF1C1	TF1C0
Flags					F1 Test FIFO Word Count										

Here:

- TF1C [10:0] = 0…1024 – F1 Test FIFO Word Count;
- TF1FF – F1 Test FIFO Full Flag or TF1C = 1024;
- TF1EF – F1 Test FIFO Empty Flag.

CSR_TF2 – F2 Test FIFO Status

This read-only registers, one register per F2 EMU muon, return the F2 Test FIFO (TF2) Flags and the TF2 Word Count. The maximum available TF2 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA only.

Table 88: CSR_TF2 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF2FF	TF2EF	0	0	0	TF2C10	TF2C9	TF2C8	TF2C7	TF2C6	TF2C5	TF2C4	TF2C3	TF2C2	TF2C1	TF2C0
Flags		F2 Test FIFO Word Count													

Here:

- TF2C [10:0] = 0…1024 – F2 Test FIFO Word Count;
- TF2FF – F2 Test FIFO Full Flag or TF2C = 1024;
- TF2EF – F2 Test FIFO Empty Flag.

CSR_TF3 – F3 Test FIFO Status

This read-only registers, one register per F3 EMU muon, return the F3 Test FIFO (TF3) Flags and the TF3 Word Count. The maximum available TF3 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA only.

Table 89: CSR_TF3 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF3FF	TF3EF	0	0	0	TF3C10	TF3C9	TF3C8	TF3C7	TF3C6	TF3C5	TF3C4	TF3C3	TF3C2	TF3C1	TF3C0
Flags		F3 Test FIFO Word Count													

Here:

- TF3C [10:0] = 0…1024 – F3 Test FIFO Word Count;
- TF3FF – F3 Test FIFO Full Flag or TF3C = 1024;
- TF3EF – F3 Test FIFO Empty Flag.

CSR_TF4 – F4 Test FIFO Status

This read-only registers, one register per F4 EMU muon, return the F4 Test FIFO (TF4) Flags and the TF4 Word Count. The maximum available TF4 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA only.

Table 90: CSR_TF4 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF4FF	TF4EF	0	0	0	TF4C10	TF4C9	TF4C8	TF4C7	TF4C6	TF4C5	TF4C4	TF4C3	TF4C2	TF4C1	TF4C0
Flags		F4 Test FIFO Word Count													

Here:

- TF4C [10:0] = 0…1024 – F4 Test FIFO Word Count;
- TF4FF – F4 Test FIFO Full Flag or TF4C = 1024;
- TF4EF – F4 Test FIFO Empty Flag.

CSR_TF5 – F5 Test FIFO Status

This read-only registers, one register per F5 EMU muon, return the F5 Test FIFO (TF5) Flags and the TF5 Word Count. The maximum available TF5 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA only.

Table 91: CSR_TF5 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF5FF	TF5EF	0	0	0	TF5C10	TF5C9	TF5C8	TF5C7	TF5C6	TF5C5	TF5C4	TF5C3	TF5C2	TF5C1	TF5C0
Flags					F5 Test FIFO Word Count										

Here:

- TF5C [10:0] = 0…1024 – F5 Test FIFO Word Count;
- TF5FF – F5 Test FIFO Full Flag or TF5C = 1024;
- TF5EF – F5 Test FIFO Empty Flag.

CSR_TFB – Barrel Test FIFO Status

This read-only register, one per MB input link, returns the Barrel Test FIFO (TFB) Flags and the TFB Word Count. The maximum available TFB capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA.

Table 92: CSR_TFB Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFBFF	TFBEF	0	0	0	TFBC10	TFBC9	TFBC8	TFBC7	TFBC6	TFBC5	TFBC4	TFBC3	TFBC2	TFBC1	TFBC0
Flags					Barrel Test FIFO Word Count										

Here:

- TFBC [10:0] = 0…1024 – Barrel Test FIFO Word Count;
- TFBFF – Barrel Test FIFO Full Flag or TFBC = 1024;
- TFBEF – Barrel Test FIFO Empty Flag.

CSR_TFC – Test FIFO Configuration

VME FPGA

For the VME_FPGA this read/write register defines requests and delay setting for a FC_TFRUN command.

Table 93: CSR_TFC Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFM	TFRL	TFRS	X	X	TFRB	X	X	X	X	X	TFD4	TFD3	TFD2	TFD1	TFD0
Mode	Test FIFO Requests														

Here:

- X – don't care bit for writes and zero for reads;
- TFD [4:0] = 0 (default)…31 - Test FIFO starts injecting data, when 1…32 bunch crossings have passed after the requested event; => not implemented yet!
- TFRB = 0 (default) /1 – don't inject (default) / inject data on the next CCB_BC0 timing mark;

- TFRS = 0 (default) /1 – don't inject (default) / inject data on the next CCB_TPSP command;
- TFRL = 0 (default) /1 – don't inject (default) / inject data on the next CCB_L1ACC command;
- TFM = 0 (default) /1 – one-time (default) / persistent request. One-time request injects data on the next event only and self-resets after that. Persistent request injects data on all events that follow.

For the FRONT_FPGA, SP_FPGA and DDU_FPGA this read/write register defines data injection points, amount of data to be injected and whether injected patterns get written back to the TF.

Front FPGA

There are two injection points in the FRONT_FPGA, one injection point in the DDU_FPGA, and three injection points in the SP_FPGA.

The default register settings are used to run a link test with data patterns, similar to the MPC-SP one. The difference is that the SP can drive 15 optical outputs to test its 15 optical inputs at once, while one MPC is capable to drive only 3 optical cables. As for the rest, the procedure is quite similar, i.e. the user should:

- connect 15 SP outputs to the 15 inputs of the same or another SP;
- configure the CSR_LNK register, if needed;
- set the CSR_FCC into a local fast control mode, in order not to interfere with other modules in the same crate, if only one SP is under tests;
- address ACT_FCC to issue L1 Reset and perform link time-in procedure;
- load the DAT_TF register with the test patterns in the same format, as he would do it for the MPC;
- compensate for the data path latency (the optical cable length, the AF word count, and the PF word count, if the SF is hooked up to its output) by configuring the CSR_SFC registers accordingly;
- run the CCB_TPSP command;
- read back the DAT_SF content and compare it with the original test patterns.

With the TFBX bit set the FRONT_FPGAs and the SP_FPGA can be configured to perform a loop back test via the Transition Board to validate the Drift Tube output and input connections. Test patterns preloaded into the Test FIFOs of F1 and F2 chips are injected into the data path, then pass via the DT output connector to the Transition Board, loop back either via the Transition Board internal multiplexer or via the Test Board to the Transition Board inputs, pass via the DT input connector, and get registered into the SP_FPGA Barrel Spy FIFOs (DAT_SFB). With the TFBX bit set there is a change in the data format for the FRONT_FPGA DAT_TF register: otherwise ignored timing bits become valid, see the DAT_TF register description for details.

Two timing bits in the DAT_TF format are treated differently from all other data bits. The TFBX bit defines if the DAT_TF timing bits BC0/BXN0/BXN1 override the data-path

timing bits during test pattern injection. By default, the data-path timing is preserved, so the OSY condition should never occur.

Table 94: CSR_TFC Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFLP	X	TFAF	TFTX	TFBX	X	X	TFW8	TFW7	TFW6	TFW5	TFW4	TFW3	TFW2	TFW1	TFW0
Loop		Injection Points		Timing			Test FIFO Window								

Here:

- X – don't care bit for writes and zero for reads;
- TFLP = 0 (default) /1 – TF Loopback option: just inject data into the injection point (default) / inject and write back data into the TF;
- TFAF = 0 (default) /1 – disable (default) / enable injecting test data at the AF output;
- TFTX = 0 (default) /1 – disable (default) / enable injecting test data into the TLK2501 transmitter;
- TFBX = 0 (default) /1 – disable (default) / enable injecting timing bits along with data patterns;
- TFW [8:0] = 0 (default)…511 – inject test patterns for 1…512 bunch crossings on the next FC_TFRUN command; the injection point is specified by the TFA/TFT bits.

SP FPGA

The SP_FPGA has three sets of Test FIFOs (DAT_TF to simulate output tracks, DAT_TF1/ DAT_TF2/ DAT_TF3/ DAT_TF4/ DAT_TF5/ DAT_TFE to simulate EMU track stubs, and DAT_TFB to simulate DT or Barrel muons) and 3 injection points accordingly.

Table 95: CSR_TFC Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFLP	TFMB	TFME	TFSP	TFBX	X	X	TFW8	TFW7	TFW6	TFW5	TFW4	TFW3	TFW2	TFW1	TFW0
Loop	Injection points			Timing			Test FIFO Window								

Here:

- X – don't care bit for writes and zero for reads;
- TFLP = 0 (default) /1 – TF Loopback option: just inject data into the injection point (default) / inject and write back data into the TF;
- TFMB = 0 (default) /1– disable (default) / enable injecting Barrel muon test data (simulates Barrel track stubs) from the Barrel Test FIFO: DAT_TFB;
- TFME = 0 (default) /1 – disable (default) / enable injecting EMU muon test data (simulates EMU track stubs) from the EMU Test FIFOs: DAT_TF1/ DAT_TF2/ DAT_TF3/ DAT_TF4/ DAT_TF5/ DAT_TFE;
- TFSP = 0 (default) /1 – disable (default) / enable injecting Track test data (simulates SP core output) from the Test FIFO: DAT_TF;
- TFBX = 0 (default) /1 – disable (default) / enable injecting timing bits along with data patterns;
- TFW [8:0] = 0 (default)…511 – if any of the TFL/TFB/TFT bits are set, then inject test patterns for 1…512 bunch crossings on the next FC_TFRUN command.

DDU FPGA

The DDU_FPGA services just one link that sends data to the DDU. The DDU data format (see DAT_DF description) does not follow a two-frame-per-bunch-crossing structure as the MPC input or SP output data formats do, so the TFW[9:0] value explicitly specifies a number of test patterns to be injected into the DDU data stream.

Table 96: CSR_TFC Data Format for DDU_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFLP	X	X	TFTX	X	X	TFW9	TFW8	TFW7	TFW6	TFW5	TFW4	TFW3	TFW2	TFW1	TFW0
Loop			Inj Point			Test FIFO Window									

Here:

- X – don't care bit for writes and zero for reads;
- TFLP = 0 (default) /1 – TF Loopback option: just inject data into the injection point (default) / inject and write back data into the TF;
- TFTX = 0 (default) /1 – disable (default) / enable injecting test data into the TLK2501 transmitter;
- TFW [9:0] = 0 (default)…1023 – inject 1…1024 test patterns on the next FC_TFRUN command; the injection point is specified by the TFT bit.

CSR_TFE – EMU Test FIFO Status

This read-only register, common for all EMU muons, returns the FE Test FIFO (TFE) Flags and the TFE Word Count. The maximum available TFE capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bunch crossing. The register address is applicable to the SP_FPGA only.

Table 97: CSR_TFE Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFEFF	TFEEF	0	0	0	TFEC10	TFEC9	TFEC8	TFEC7	TFEC6	TFEC5	TFEC4	TFEC3	TFEC2	TFEC1	TFEC0
Flags					FE Test FIFO Word Count										

Here:

- TFEC [10:0] = 0…1024 – FE Test FIFO Word Count;
- TFEFF – FE Test FIFO Full Flag or TFEC = 1024;
- TFEEF – FE Test FIFO Empty Flag.

CSR_WOF – Warning-of-OverFlow Control / Status

In the VME_FPGA the CSR_WOF register displays status of seven input and one output WOF lines. Besides, it carries eight mask bits, so each input or/and VME_FPGA output can be either disabled or enabled:

WOF0 = (WOF1*WOM1 + WOF2*WOM2 + WOF3*WOM3 + WOF4*WOM4 + WOF5*WOM5 + WOF6*WOM6 + WOF7 *WOM7) * WOM0

Indexes 0…7 stand for chip numbers; see Table 8 and/or Table 45 for a chip numbering convention.

The WOF0 signal controls the SP readout process by inhibiting the FC_L1STR signal: incoming CCB_L1ACC signals increment event counters to keep them in synch with other systems, but no events get added to the readout queue. Both the FRONT_FPGA and SP_FPGA set WOF to "1", when either the L1 Accept FIFO or Ring Buffer are almost full. Both drop WOF

to “0”, when there is a room for at least one more event. The DDU_FPGA sets its WOF to “1”, when the DAQ FIFO is almost full, and drops it to “0”, when there is a room for at least one more event.

Table 98: CSR_WOF Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
WOM7	WOM6	WOM5	WOM4	WOM3	WOM2	WOM1	WOM0	WOF7	WOF6	WOF5	WOF4	WOF3	WOF2	WOF1	WOF0	R
WOM7	WOM6	WOM5	WOM4	WOM3	WOM2	WOM1	WOM0	X	X	X	X	X	X	X	X	W

Here:

- X – Don’t care bit;
- WOM [7:0] – Warning-of-Overflow chip Mask for SP, DD, F5…F1, and VM chips;
- WOF [7:0] – Warning-of-OverFlow status for SP, DD, F5…F1, and VM chips.

Data Register Group

DAT_DF – DAQ FIFO Data

See LU-SP2DDU_Event_Record_Structure_4d0.pdf for details.

DAT_DT – Drift Tube Global Phi LUT Data

This read/write registers provides access to the Drift Tube Global Phi LUT content. The DT LUT data format is shown in the table below. Read/write transfers are performed on the DT LUT current address defined by the CNT_GLL and CNT_GLH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three muons and to the DT/GP/GE LUTs, serviced by the FRONT_FPGA. Register address is applicable to the FRONT_FPGA only.

This register is protected against accidental accesses: in order to get VME access to this register the SP should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two commands:

- VW/MA/CSR_FCC/W/0x0100 -> under VME control
- VM/MA/ACT_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

Table 99: DAT_DT Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	DT11	DT10	DT9	DT8	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
				Drift Tube Global Phi											

Here:

- X – don’t care bit, returns zero on reads;
- DT [11:0] = 0…4095 – Drift Tube Global Phi.

DAT_ETA – Eta Min/Max/Win Data

This read/write register provides access to the Eta register file content. The register file keeps data for Eta Minimum – 8 words, Eta Maximum – 8 words, Eta Window – 6 words and Eta Offset – 4 words setting, in that order, which totals to 26 data words. The CNT_ETA counter

provides indexed access to the register content; see the CNT_ETA register description for details.

There are 8 types of pair-wise extrapolations between 2 stations in the core SP logic, which listed in numerical order are:

1. ME1-ME2
2. ME1-ME3
3. ME2-ME3
4. ME2-ME4
5. ME3-ME4
6. ME1-ME2ov
7. ME2-MB1
8. ME2-MB2.

The last type is no longer implemented in hardware (the SP doesn't get the signals) but still exists in the firmware input. In the extrapolation unit the requirement is that Eta from each track segment lie in this range. There is also a cut on the difference in Eta, called Eta Window, between two stations for the first 6 CSC extrapolation units, since the DT system does not sent Eta values. This cut is very powerful against beam halo muons. Eta Offsets can be added to each CSC station (ME1-4) to compensate for chamber offsets in beam test data.

The default settings are:

- Eta Minimum: 22, 22, 14, 14, 14, 10, 10, 10
- Eta Maximum: 127, 127, 127, 127, 127, 24, 24, 24
- Eta Window: 2, 2, 2, 2, 2, 2
- Eta Offset: 0, 0, 0, 0

This register is protected against accidental accesses: in order to get VME access to this register the SP should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two VME commands:

- VW/MA/CSR_FCC/W/0x0100 -> put the SP under the VME control
- VM/MA/ACT_FCC/W/0x00C8 -> issue a bx reset command prior to addressing the data register.

Table 100: DAT_ETA Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	ETAP7	ETAP6	ETAP5	ETAP4	ETAP3	ETAP2	ETAP1	ETAP0
								Eta Parameters							

Here:

- X – don’t care bit, reads back as zero;
- ETAP [7:0] = 0…127 for Eta Minimum;
- ETAP [7:0] = 0…127 for Eta Maximum;
- ETAP [7:0] = 0…255 for Eta Window;
- ETAP [7:0] = 0…127 for Eta Offset;

DAT_GE – Global Eta LUT Data

This read/write registers provides access to the Global Eta LUT content. The GE LUT data format is shown in the table below. Read/write transfers are performed on the GE LUT current address defined by the CNT_GLL and CNT_GLH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three muons and to the DT/GP/GE LUTs, serviced by the FRONT_FPGA. Register address is applicable to the FRONT_FPGA only.

This register is protected against accidental accesses: in order to get VME access to this register the SP should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two commands:

- VW/MA/CSR_FCC/W/0x0100 -> under VME control
- VM/MA/ACT_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

Table 101: DAT_GE Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	GE11	GE10	GE9	GE8	GE7	GE6	GE5	GE4	GE3	GE2	GE1	GE0
				Global Phi Bend					Global Eta						

Here:

- X – don't care bit, returns zero on reads;
- GE [6:0] = 0…127 – Global Eta;
- GE[11:7] = 0…31 – Global Phi Bend;

DAT_GP – Global Phi LUT Data

This read/write registers provides access to the Global Phi LUT content. The GP LUT data format is shown in the table below. Read/write transfers are performed on the GP LUT current address defined by the CNT_GLL and CNT_GLH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three muons and to the DT/GP/GE LUTs, serviced by the FRONT_FPGA. Register address is applicable to the FRONT_FPGA only.

This register is protected against accidental accesses: in order to get VME access to this register the SP should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two commands:

- VW/MA/CSR_FCC/W/0x0100 -> under VME control
- VM/MA/ACT_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

Table 102: DAT_GP Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
				Global Phi											

Here:

- X – don't care bit, returns zero on reads;
- GP [11:0] = 0…4095 – Global Phi.

DAT_LP – Local Phi LUT Data

This read/write registers provides access to the Local Phi LUT content. The LP LUT data format is shown in Table 103. Read/write transfers are performed on the LP LUT current address defined by the CNT_LPL and CNT_LPH values; after that the counter auto-increments. Note, that the local phi LUT address counter is common to all three muons, serviced by the FRONT_FPGA. Register address is applicable to the FRONT_FPGA only.

This register is protected against accidental accesses: in order to get VME access to this register the SP should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two commands:

- VW/MA/CSR_FCC/W/0x0100 -> under VME control
- VM/MA/ACT_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

Table 103: DAT_LP Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LPB5	LPB4	LPB3	LPB2	LPB1	LPB0	LP9	LP8	LP7	LP6	LP5	LP4	LP3	LP2	LP1	LP0
Local Phi Bend						Local Phi									

Here:

- LP [9:0] = 0…1023 – Local Phi.
- LPB [5:0] = 0…31 – Local Phi Bend.

DAT_PT – PT LUT Data

This read/write registers provides access to the PT LUT content. The PT LUT data format is shown in the table below. Read/write transfers are performed on the PT LUT current address defined by the CNT_PTL and CNT_PTH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three PT LUTs serviced by the SP_FPGA.

This register is protected against accidental accesses: in order to get VME access to this register the SP should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two commands:

- VW/MA/CSR_FCC/W/0x0100 -> under VME control
- VM/MA/ACT_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

Table 104: DAT_PT Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RVC	RQ1	RQ0	RR4	RR3	RR2	RR1	RR0	FVC	FQ1	FQ0	FR4	FR3	FR2	FR1	FR0
Rear Muon Data								Front Muon Data							

Here:

- RVC – Rear muon Valig Charge;
- RQ[1:0] – Rear muon Quality;
- RR[4:0] – Rear muon Rank;
- FVC – Front muon Valig Charge;
- FQ[1:0] – Front muon Quality;

– FR[4:0] – Front muon Rank.

DAT_RW – Data Transfer Bus Read/Write Register

This register is used for backplane and internal data bus validation. It allows write/read cycles to be performed to/from each FPGA chip without affecting SP functionality in any way.

Table 105: DAT_RW Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Validation Data Word															

DAT_SF – Spy FIFO Data

VME cycles addressed to this read-only register return data from the Spy FIFO (SF). Preferred method of reading the SF content is setting up the BLT read. Before reading the SF content it is useful to check the SF status, by addressing to the CSR_SF register, which would return the current SF word count. Address is valid for FRONT_FPGA (3 each) and SP_FPGA (3 each).

Front FPGA

The FRONT_FPGA SF input could be connected to either Pipeline FIFO Input or Pipeline FIFO output, as defined by the CSR_SFC register. Data format for both sources is shown in tables below. Two header words with Bunch Crossing Counter (BXN) and Event Counter (EC) values are available only when the FRONT_FPGA input is connected to the Pipeline FIFO output. The process of collecting data into the SF is regulated by fast control commands.

Every muon input link has a BXN associated with it and synchronized by the BC0 timing mark coming along with the data. On power-up and after CCB_BXRES, or CCB_L1RES commands the BXN gets preloaded with a 0xDEC=3564 value. Every time the link BC0 mark arrives it resets its BXN to zero and the BXN starts counting up. If the BC0 does not arrive in time, the BXN reaches its maximum value of 0xDEC=3564 and stops.

In a properly timed-in setup, all link BXNs should be in synch. This ensures that at any given moment the SP gets data tagged by the same bunch crossing number. The SP can only diagnose if the data on different links is timed-in or not, using its Spy FIFO triggered by the CCB_L1ACC signal, see the CSR_SFC and DAT_SF register descriptions for detail. It is the ALCT and Peripheral Crate electronics that actually performs the data tagging procedure, while the SP gets link data with already embedded timing marks.

Table 106: DAT_SF Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
0	0	0	0	Bunch Crossing Counter BXN [11:0]												HD1
0	0	0	0	Event Counter EC [11:0]												HD2
VP	Quality [3:0]			CLCT Pattern # [3:0]				Wire Group ID [6:0]								FR1
CSC ID [3:0]				BC0	BXN0	SE	L/R	CLCT Pattern ID [7:0]								FR2

Here:

– HD1 and HD2 – Header words, available only when the SF input is connected to the PF output; It is used to monitor relative timing of different links.

- VP – Valid Pattern flag;
- Quality – the more hits the higher LCT Quality;
- CLCT Pattern # – 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit;
- Wire Group ID – 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111;
- CSC ID – 4-bit CSC ID indicates the chamber # and runs from 1 to 9;
- BC0 – Bunch Crossing Zero flag marks bunch zero data**;**
- BXN0 – Bunch Crossing Number least significant bit;
- SE – Synchronization Error bit;
- L/R – Left/Right bend bit indicates whether the track is heading towards lower or higher strip number;
- CLCT Pattern ID – For high pT patterns, the 8-bit half-strip ID is between 0 and 159. For low pT patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or "key" layer of the chamber.

SP FPGA

The SP_FPGA SF input could be connected to either Pipeline FIFO Input or Pipeline FIFO output, as defined by the CSR_SFC register. Data format for both sources is shown in table below. The process of collecting data into the SF is regulated by fast control commands.

Table 107: DAT_SF Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
RSV	SE	HL	Eta [4:0]					CHRG	FR	SIGN	Phi [4:0]					FR1
Mode [3:0]				Delta23 Phi [3:0]				Delta12 Phi [7:0]								FR2

Here:

- HD1 and HD2 – Header words, available only when the SF input is connected to the PF output;
- Phi [4:0] is the Azimuth Coordinate;
- Eta [4:0] is the Pseudorapidity, the Eta [4:1] is a part of the PT LUT address;
- SIGN – the Delta Phi Sign bit is a part of the PT LUT address;
- FR – the Front/Rear bit;
- CHRG – the Muon Charge or Sign bit;
- HL – the Halo bit;
- SE – the Synchronization Error bit;
- RSV – the Reserved bit;
- Delta12 Phi [7:0] is a part of the PT LUT address;
- Delta23 Phi [3:0] is a part of the PT LUT address;
- Mode [3:0] is a part of the PT LUT address.

DDU FPGA

The DDU_FPGA SF input can be connected to either the TLK2501 Transmitter output or TLK2501 Receiver input, as defined by the CSR_SFC register. Data format for both sources is shown in table below. The process of collecting data into the SF is regulated by fast control commands.

Table 108: DAT_SF Data Format for DDU_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DF15	DF14	DF13	DF12	DF11	DF10	DF9	DF8	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0

Here:

– DF [15:0] – DAQ FIFO data bits; see DAT_DF register description for details.

DAT_SF1 – F1 Spy FIFO Data

This read-only register in the SP_FPGA, one register per F1 EMU muon, returns data from the F1 Spy FIFO (SF1). The SF1 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BXN0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR_SFC register description.

Table 109: DAT_SF1 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
CSC ID [3:0]				Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

– Global Phi [11:0] = 0…4095;
– Global Eta [6:0] = 0…127;
– Global Phi Bend [11:7] = 0…31;
– Quality [3:0] = 0…15;
– CSC ID [3:0] = 1…9.

DAT_SF2 – F2 Spy FIFO Data

This read-only register in the SP_FPGA, one register per F2 EMU muon, returns data from the F2 Spy FIFO (SF2). The SF2 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BXN0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR_SFC register description.

Table 110: DAT_SF2 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
CSC ID [3:0]				Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

– Global Phi [11:0] = 0…4095;
– Global Eta [6:0] = 0…127;
– Global Phi Bend [11:7] = 0…31;

- Quality [3:0] = 0…15;
- CSC ID [3:0] = 1…9.

DAT_SF3 – F3 Spy FIFO Data

This read-only register in the SP_FPGA, one register per F3 EMU muon, returns data from the F3 Spy FIFO (SF3). The SF3 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BXN0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR_SFC register description.

Table 111: DAT_SF3 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
0	0	0	0	Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15.

DAT_SF4 – F4 Spy FIFO Data

This read-only register in the SP_FPGA, one register per F4 EMU muon, returns data from the F4 Spy FIFO (SF4). The SF4 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BXN0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR_SFC register description.

Table 112: DAT_SF4 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
0	0	0	0	Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15.

DAT_SF5 – F5 Spy FIFO Data

This read-only register in the SP_FPGA, one register per F5 EMU muon, returns data from the F5 Spy FIFO (SF5). The SF5 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BXN0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR_SFC register description.

Table 113: DAT_SF5 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
0	0	0	0	Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15.

DAT_SFE – EMU Spy FIFO Data

This read-only register in the SP_FPGA returns data from the FE Spy FIFO, which carries VP, SE and timing marks for all fifteen EMU muons. Each FRONT_FPGA sends a pair of timing marks to the SP_FPGA, but all active muon links should be timed on L1 Reset, so that the timing is the same for all FRONT_FPGAs. What the Spy FIFO captures is a logical OR of five BC0 and five BXN0 timing signals. On how to configure the spying process refer to the CSR_SFC register description. The BC0 and BXN0 bits can also be found in the M1/DAT_SFM, M2/DAT_SFM and M3/DAT_SFM registers, where they incorporate also Barrel Muon timing marks (to be implemented !).

Table 114: DAT_SFE Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
BXN0	F5 VP Flags			F4 VP Flags			F3 VP Flags			F2 VP Flags			F1 VP flags			FR1
BC0	F5 SE Flags			F4 SE Flags			F3 SE Flags			F2 SE Flags			F1 SE flags			FR2

Here:

- Valid Pattern flags, one per EMU muon;
- Synch Error flags, one per EMU muon;
- BXN0 – an OR (or some other Boolean function => to be determined) of same signals received along with ME LCTs;
- BC0 – an OR (or some other Boolean function => to be determined) of same signals received along with ME LCTs;

DAT_SFB – Barrel Spy FIFO Data

This read-only register in the SP_FPGA, one per a barrel muon link, returns data from the Barrel Spy FIFO, which carries track stubs from the overlapping DT region. Refer to the CSR_SFC register descriptions for details on how to configure the Barrel Spy FIFO.

Table 115: DAT_SFB Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
VQ	0	Calib	Flag	0	0	0	Phi Bend [4:0]					0	Q [2:0]			FR1
0	BC0	BXN0	BXN1	Phi [11:0]												FR2

Here:

- Q [2:0] = 0…7 – Muon Quality; For valid data Quality is always > 0;
- VQ – Valid Quality flag. This is a derivative bit from Q [2:0] > 0;
- Phi Bend {4:0] – Phi Bend angle;

- Phi [11:0] – Azimuth Coordinate;
- Flag, if 1 then it is a second muon from previous bunch crossing;
- Calib – a DT special mode flag;
- BXN0, BXN1 – two LSBs of the DT bunch counter;
- BC0 – Bunch crossing zero flag.

When the CSR_FCC/FCT bit is set and a loopback test is being performed on the DT outputs/inputs, the DAT_SFB format changes. Since the Transition Board has 4 output connectors and only 2 input connectors, the user can loop back the DT output from only one FRONT_FPGA (F1 or F2) at any given time.

Table 116: DAT_SFB/M1 Data Format for SP_FPGA: DT loopback test option

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
0	0	ME1B_PHI[5:4]		0	0	0	ME1B_PHI0	ME1A_Q[2:0]			ME1A_ETA	0	ME1B_PHI[3:1]			FR1
ME1B_PHI[9:6]				ME1A_PHI[11:0]]												FR2

Table 117: DAT_SFB/M2 Data Format for SP_FPGA: DT loopback test option

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
0	0	ME1C_Q[2:1]		0	0	0	ME1C_PHI[10:6]					0	ME1C_Q0	ME1C_ETA	ME1C_PHI11	FR1
0	ME1A_BC0	ME1A_BXN0	ME1A_BXN1	ME1C_PHI[5:0]						ME1B_Q[2:0]			ME1B_ETA	ME1B_PHI[11:10]		FR2

Here:

- ME1A_PHI [11:0] – FX/M1 muon azimuth coordinate, FX = F1 or F2;
- ME1B_PHI [11:0] – FX/M2 muon azimuth coordinate, FX = F1 or F2;
- ME1C_PHI [11:0] – FX/M3 muon azimuth coordinate, FX = F1 or F2;
- ME1A_Q [2:0] – FX/M1 muon Quality, FX = F1 or F2;
- ME1B_Q [2:0] – FX/M2 muon Quality, FX = F1 or F2;
- ME1C_Q [2:0] – FX/M3 muon Quality, FX = F1 or F2;
- ME1A_ETA – FX/M1 muon region flag, FX = F1 or F2;
- ME1B_ETA – FX/M2 muon region flag, FX = F1 or F2;
- ME1C_ETA – FX/M3 muon region flag, FX = F1 or F2;
- ME1A_BXN0, ME1A_BXN1– two LSBs of the FX/M1 bunch counter, FX = F1 or F2;
- ME1A_BC0 – FX/M1 bunch crossing zero flag, FX = F1 or F2.

DAT_SFM – MS Spy FIFO Data

This read-only register in the SP_FPGA, one per output track, returns data from the MS Spy FIFO, which carries MS winner bits, muon stub IDs and muon stub Tbin numbers. If the stub ID is non-zero, then it shows the input stub number used by the SP core logic to build the output track. The Tbin value shows the track stub relative time bin number in case the Bunch crossing analyzer is enabled. The same BC0 and BXN0 bits can also be found in the DAT_TFE / DAT_SFE registers.

Table 118: DAT_SFM Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
BXN0	MS_ID [3:1]			MB_ID [2:0]			ME4_ID[1:0]		ME3_ID [1:0]		ME2_ID [1:0]		ME1_ID [2:0]			FR1
BC0	MB_TBIN [2:0]			ME4_TBIN [2:0]			ME3_TBIN [2:0]			ME2_TBIN [2:0]			ME1_TBIN [2:0]			FR2

Here:

- BXN0 – an OR (or some other Boolean function => to be determined) of same signals received along with ME LCTs and MB stubs, and passed to the MS; (barrel timing mark to be implemented !)
- BC0 – an OR (or some other Boolean function => to be determined) of same signals received along with ME LCTs and MB stubs and passed to the MS; (barrel timing mark to be implemented !)
- MS_ID [3:1] = Muon Sorter Winner bit positional code;
- ME1_ID [2:0], ME2_ID [1:0], ME3_ID [1:0], ME4_ID [1:0], MB_ID [2:0] – track stub IDs used to build up a track;
- ME1_TBIN [2:0], ME2_TBIN [2:0], ME3_TBIN [2:0], ME4_TBIN [2:0], MB_TBIN [2:0] – Time Bins of the track stubs used to build up a track;

For the track stub ID to muon correspondence see table below.

Table 119: Muon ID to Spy FIFO Correspondence

Muon ID	Look for track stub into the Spy FIFO
ME1_ID = 1	SP/DAT_SF1/M1
ME1_ID = 2	SP/DAT_SF1/M2
ME1_ID = 3	SP/DAT_SF1/M3
ME1_ID = 4	SP/DAT_SF2/M1
ME1_ID = 5	SP/DAT_SF2/M2
ME1_ID = 6	SP/DAT_SF2/M3
ME2_ID = 1	SP/DAT_SF3/M1
ME2_ID = 2	SP/DAT_SF3/M2
ME2_ID = 3	SP/DAT_SF3/M3
ME3_ID = 1	SP/DAT_SF4/M1
ME3_ID = 2	SP/DAT_SF4/M2
ME3_ID = 3	SP/DAT_SF4/M3
ME4_ID = 1	SP/DAT_SF5/M1
ME4_ID = 2	SP/DAT_SF5/M2
ME4_ID = 3	SP/DAT_SF5/M3
MB_ID = 1	SP/DAT_SFB/M1
MB_ID = 2	SP/DAT_SFB/M1 – next bx
MB_ID = 3	SP/DAT_SFB/M2
MB_ID = 4	SP/DAT_SFB/M2 – next bx

DAT_TF – Test FIFO Data

VME cycles addressed to this write-only register load data in the Test FIFO (TF). Address is valid for FRONT_FPGA (3 each), SP_FPGA (3 each) and DDU_FPGA (1 each).

Front FPGA

The output of the FRONT_FPGA Test FIFO can be connected either to the TLK2501 transmitter to provide test patterns for link tests or to the Alignment FIFO output to provide for SP logic tests. Injection points for the DAT_TF are defined by the CSR_TFC register.

Table 120 shows the DAT_TF data format, which exactly follows the MPC – SP two-frame data format. For DT interface tests, the SE bit have different meaning, as shown in Table 121. The conversion rule from a 4-bit MPC quality to a 3-bit DT quality is yet to be finalized, as well as conversion from CSC_ID into DT_ETA. In the meantime, the following mapping is valid: DT_ETA = Quality [3] and DT_Quality [2:0] = Quality [2:0].

Injection of the BCO/BXN0 timing bits is controlled with a special TFBX bit in the CSR_TFC register. By default, the data-path timing is preserved, so the OSY condition should never occur as a result of test pattern injection.

Table 120: DAT_TF Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
VP	Quality [3:0]				CLCT Pattern # [3:0]			Wire Group ID [6:0]								FR1
CSC ID [3:0]				BC0	BXN0	SE	L/R	CLCT Pattern ID [7:0]								FR2

Table 121: DAT_TF Data Format for FRONT_FPGA during the DT Interface Loop-back Test

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
VP	Quality [3:0]				CLCT Pattern # [3:0]			Wire Group ID [6:0]								FR1
CSC ID [3:0]				BC0	BXN0	BXN1	L/R	CLCT Pattern ID [7:0]								FR2

Here:

- X – Don't care bit;
- VP – Valid Pattern flag;
- Quality - the more hits the higher track Quality;
- CLCT Pattern # - the 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit;
- Wire Group ID - the 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111;
- CSC ID - the 4-bit CSC ID indicates the chamber # and runs from 1 to 9;
- SE - Synchronization Error bit;
- BC0 – Bunch crossing zero timing mark;
- BXN0, BXN1 – 2 LSBs of the Link Bunch Crossing Counter;
- L/R - the Left/Right bend bit indicates whether the track is heading towards lower or higher strip number;
- CLCT Pattern ID - For high pT patterns, the 8-bit half-strip ID is between 0 and 159. For low pT patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or "key" layer of the chamber.

SP FPGA

With the help of the SP/DAT_TF every bit of the SP => MS interface can be tested, except for the BC0/BXN0 timing bits. Use the SP/DAT_TFE register to test timing bits.

Since the FRONT_FPGA BC0/BNX0 timing bits are ORed in the SP_FPGA they will propagate to the SP => MS interface, as they were injected from the SP Test FIFO. The injected SP Test FIFO data patterns will override all other data bits in the data-path.

Table 122: DAT_TF Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
RSV	SE	HL	ETA [4:0]					CHRG	FR	SIGN	PHI [4:0]					FR1
MODE [3:0]				DELTA23 PHI [3:0]				DELTA12 PHI [7:0]								FR2

Here:

- PHI [4:0] is the Azimuth Coordinate;
- ETA [4:0] is the Pseudo rapidity, the ETA [4:1] is part of the PT LUT address;
- SIGN – the Delta Phi Sign bit is a part of the PT LUT address;
- FR – the Front/Rear bit;
- CHRG – the Muon Charge or Sign bit;
- HL – the Halo bit;
- SE – the Synchronization Error bit;
- RSV – the Reserved bit;
- DELTA12 PHI [7:0] is part of the PT LUT address;
- DELTA23 PHI [3:0] is part of the PT LUT address;
- MODE [3:0] is part of the PT LUT address.

DDU FPGA

In the DDU_FPGA the TF is used to perform loop-back tests of the TLK2501 chip to validate its proper connectivity to the FPGA.

Table 123: DAT_TF Data Format for DDU_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DF15	DF14	DF13	DF12	DF11	DF10	DF9	DF8	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0

Here:

- DF [15:0] – DAQ FIFO data bits; see DAT_DF register description for details.

DAT_TF1 – F1 Test FIFO Data

This write-only register in the SP_FPGA, one register per F1 EMU muon, keeps the F1 Test FIFO (TF1) data. The TF1 data can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR_TFC register description.

Table 124: DAT_TF1 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
CSC ID [3:0]				Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15;
- CSC ID [3:0] = 1…9.

DAT_TF2 – F2 Test FIFO Data

This write-only register in the SP_FPGA, one register per F2 EMU muon, keeps the F2 Test FIFO (TF2) data. The TF2 data can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR_TFC register description.

Table 125: DAT_TF2 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
CSC ID [3:0]				Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15;
- CSC ID [3:0] = 1…9.

DAT_TF3 – F3 Test FIFO Data

This write-only register in the SP_FPGA, one register per F3 EMU muon, keeps the F3 Test FIFO (TF3) data. The TF3 data can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR_TFC register description.

Table 126: DAT_TF3 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
X	X	X	X	Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- X – don’t care bit;
- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15.

DAT_TF4 – F4 Test FIFO Data

This write-only register in the SP_FPGA, one register per F4 EMU muon, keeps the F4 Test FIFO (TF4) data. The TF4 data can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR_TFC register description.

Table 127: DAT_TF4 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
X	X	X	X	Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- X – don't care bit;
- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15.

DAT_TF5 – F5 Test FIFO Data

This write-only register in the SP_FPGA, one register per F5 EMU muon, keeps the F5 Test FIFO (TF5) data. The TF5 data can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR_TFC register description.

Table 128: DAT_TF5 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
X	X	X	X	Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- X – don't care bit;
- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15.

DAT_TFB – Barrel Test FIFO Data

his write-only register in the SP_FPGA, one register per F1 EMU muon, keeps the F1 Test FIFO (TF1) data. The TF1 data can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR_TFC register description. This read-only register in the SP_FPGA, one per output track, returns data from the MS Spy FIFO, which carries track ID, MS winner bits, and the PT LUT output. If the ID is non-zero, it shows the input stub number used by the SP core logic to build the output track. Although there is a DAT_SFM register for each output track, only one register at a time can be selected for spying on the PT LUT output data, refer to the CSR_SFC register descriptions for details.

Table 129: DAT_TFB Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
X	X	Calib	Flag	X	X	X	Phi Bend [4:0]					X	Quality [2:0]			FR1
X	BC0	BXN0	BXN1	Phi [11:0]												FR2

Here:

- X – don't care bit
- Quality [2:0] = 0…7 – Muon Quality; For valid data Quality is always > 0;
- Phi Bend {4:0] – Phi Bend angle;
- Phi [11:0] – Azimuth Coordinate;
- Flag, if 1 then it is a second muon from previous bunch crossing;
- Calib – a DT special mode flag;
- BXN0, BXN1 and BC0 timing bits are injected, if SP/CSR_TFC/TFBX=1, see Table 95 for details.

DAT_TFE – EMU Test FIFO Data

This write-only register in the SP_FPGA keeps the FE Test FIFO data, which carries VP and SE bits for all fifteen EMU muons. The content of the TFE can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. On how to configure the testing process refer to the CSR_TFC register description.

Table 130: DAT_TFE Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
BXN0	F5 VP Flags			F4 VP Flags			F3 VP Flags			F2 VP Flags			F1 VP flags			FR1
BC0	F5 SE Flags			F4 SE Flags			F3 SE Flags			F2 SE Flags			F1 SE flags			FR2

Here:

- BXN0 and BC0 timing bits are injected if SP/CSR_FCC/FCT=1, see Table 52 for details;
- Valid Pattern flags, one per EMU muon;
- Synch Error flags, one per EMU muon.

DAT_VPC – Valid Pattern Counter Data

This read-only register is intended to monitor incoming muon stub rate for each link by counting the number of Valid Pattern bits at the Alignment FIFO output in the FRONT_FPGAs and outgoing track rate for each SP core output by counting the number of Mode>0 decisions in the SP_FPGA. The counter control follows that of the event counter: it is reset on the FC_L1RES and FC_ECRES commands and enabled when data taking state machine is in L1A_RUN state, see Figure 1 for details on L1Accept control. An internal 42-bit binary counter is read out in a floating point format as VPM * 2^{VPP}. The DAT_VPC address is applicable to FRONT_FPGAs and SP_FPGA.

Table 131: DAT_VP Data Format for FRONT_FPGA and SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VPM10	VPM9	VPM8	VPM7	VPM6	VPM5	VPM4	VPM3	VPM2	VPM1	VPM0	VPP4	VPP3	VPP2	VPP1	VPP0
Mantissa											Power of 2				

Here:

- VPM [10:0] = 0…2047 - Mantissa;
- VPP [4:0] = 0…31 – Power of 2.

Status Register Group (Expert Only)

STS_AF – AF FSU Status

This read-only register shows the status of the Finite State Machine (FSM) controlling the Alignment FIFO write enable input in the FRONT_FPGA and the Error Propagation Counter at the Alignment FIFO output. The EPC is reset either on VM/ACT_HR/WR[0] = 1 Soft Reset VME command or on FC_L1RES.

Table 132: STS_AF Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	EPC3	EPC2	EPC1	EPC0	0	0	0	0	WREN	FRM1	IDLE	INIT
				EPC [3:0]								AF_STATE [3:0]			

Here:

- AF_STATE [3:0] = AF One-Hot FSM States;
- INIT – Init State, which is the first state on power up or sysreset;
- IDLE – Idle State, the TLK2501 receives IDLE characters from the MPC after CCB_L1RES/TTC_L1RES was issued;
- FRM1 – Frame One State, the TLK2501 has received first data frame from the MPC;
- WREN – Write Enable State, the TLK2501 has received second data frame from the MPC and keeps receiving MPC data;
- EPC [3:0] – Error Propagation Counter.

STS_ANA – CCB Analyzer

The CCB analyzer allows registering timing of the CCB command strobe with respect to the SP system clock, as well as the CCB command itself. The SP system clock (SYS_CLK) is a deskewed CCB_CLK that drives every SP FPGA chip. The contents of the analyzer is reset on power-up and on any write command (data value is irrelevant) to this register. After reset, it starts recording non-zero data, if the SP is under the CCB fast control; see the CSR_FCC register description on how to set the SP under the CCB control. Any read command returns recorded data in the format shown below. The analyzer keeps up to 64 data words. If the analyzer is empty, the read command returns bus error to the VME Master. Typical position of the CCB command (data) strobe is shown below:

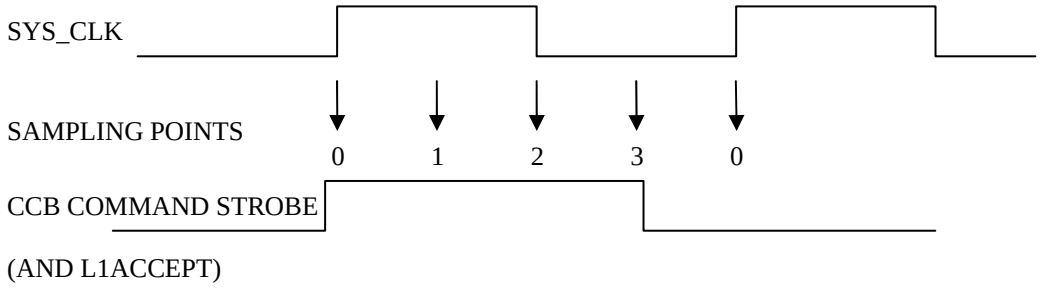


Figure 2: CCB Command Strobe (L1Accept) typical position

Typical set of values that analyzer returns after recording the CCB_L1RES, CCB_L1STT, CCB_BCO and CCB_L1ACC command sequence are:

- 1st word = 0x0F0C;
- 2nd word = 0x0F18;
- 3rd word = 0x0F04;
- 4th word = 0xF000.

Since the analyzer records only non-zero input, the above sequence means that:

- Valid samples are on all phases;
- The VME_FPGA finally samples the CCB command on phase 2, which is about the middle valid sample.

Table 133: STS_ANA Data Format for VME_FPGA

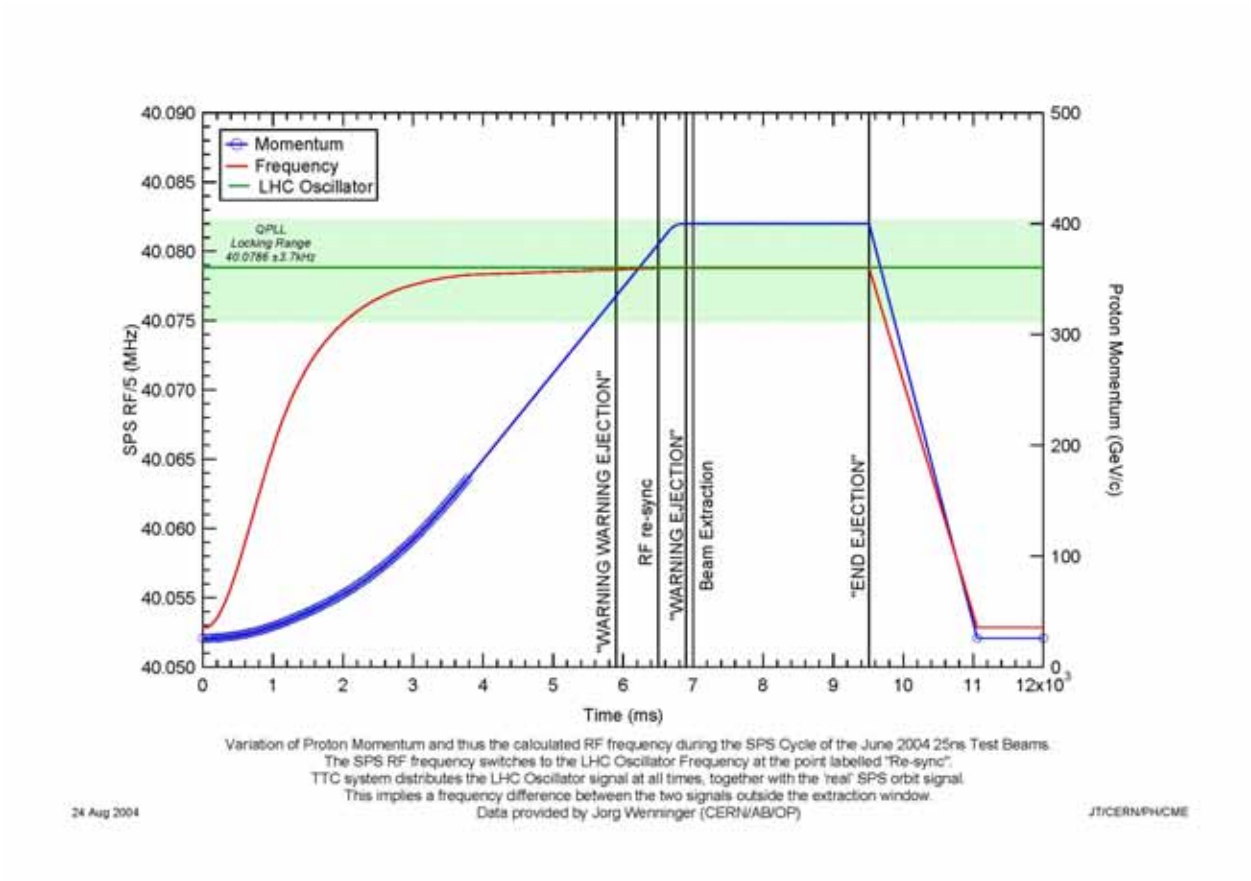
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L1AC3	L1AC2	L1AC1	L1AC0	CSTR3	CSTR2	CSTR1	CSTR0	CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	ECRES	BCRES
L1 Accept				CCB Command Strobe				CCB command							

Here:

- L1AC[3:0] – L1 Accept sampled on four different phases of the SYS_CLK clock (3/4, 2/4, 1/4, and 0/4 of the SYS_CLK period);
- CSTR[3:0] – CCB command strobe sampled on four different phases of the SYS_CLK clock (3/4, 2/4, 1/4, and 0/4 of the SYS_CLK period);
- CMD [7:2] – CCB command code;
- ECRES – Event Counter Reset;
- BCRES – Bunch Crossing Counter Reset.

STS_BC0 – Orbit Analyzer

The Orbit Analyzer (OA) keeps record of all occurrences when an SPS orbit period



counted in bunch crossings has changed. The OA is built to study the SPS spill structure during test beams.

Figure 3: SPS Spill Structure

There is an orbit rephrasing stage between “Warning Warning Ejection” (WWE) and “Warning Ejection” (WE) marks, when the SPS revolution frequency is resynchronized to the bunch frequency. As it has been shown during the test beams the OA helps to study the rephrasing process in great detail.

The OA consists of the Orbit Counter (OC), the Bunch Crossing Counter (BXN) and the FIFO. The OA is active only when the L1Accept FSM is in L1_WAIT or L1_RUN states; see Figure 1 for details on the L1Accept FSM logic. In practice it means that the OA is active only during beam gate or beam extraction phase.

When the OA is inactive, its OC is reset to zero and its BXN is reset to 3564 or 0xDEC. The OA FIFO can be reset either with a L1 Reset TTC command or by a VME write access to the STS_BC0 register.

When the OA is active, the OC increments by 1 and the BXN resets to 1 on every orbit signal (BC0), so the OC counts from 1 and up during the spill gate and the BXN counts from 1 to a maximum value determined by the arrival time of the next BC0 signal.

On the first orbit signal in beam gate the OA FIFO stores a two-frame event, consisting of the current BXN value of 4094 and the current OC value of 1. Next BC0 signal stores the BXN value of 924 and the OC value of 2, since the OA detects the change in the orbit period, which normally equals to 924 bunch crossing periods (924BX orbit). If there are no irregular orbits (925BX or 923BX orbits) in a spill the above 2 events are the only events stored in the OA FIFO per spill. This is the case, when the beam gate is triggered by the WE signal. But if the beam gate is triggered by the WWE signal the OA stores about 43-44 events per spill, recording the process of gradual approach of the orbit period to a nominal 924BX one.

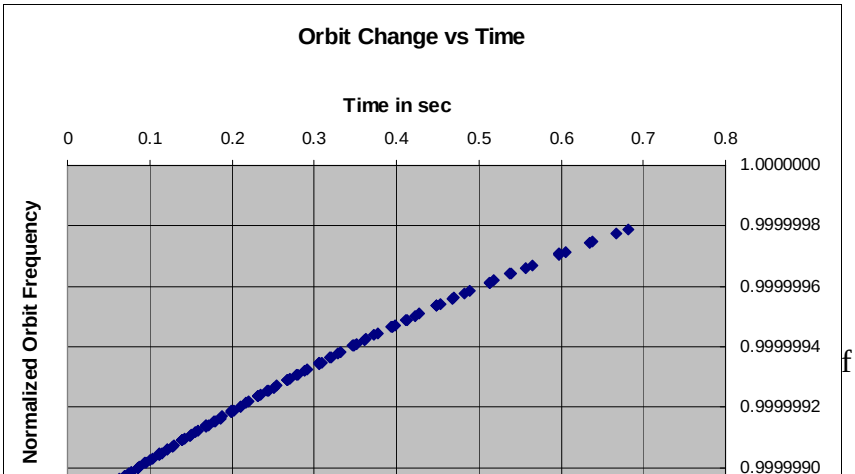
VME read access to the STS_BC0 register is acknowledged with DTACK* when there is data to read back, otherwise it is acknowledged with BERR*.

Table 134: Typical OA FIFO event dump for beam gates triggered by WE.

Frame1	Frame 2
4094	1
924	2
4094	1
924	2
…	…

Table 135 and Figure 4: Typical OA FIFO event dump for beam gates triggered by WWE and typical data recalculated into the orbit frequency change versus time.

Frame1	Frame 2
4094	1
924	2
925	177
924	178
925	1159
924	1160



925	2179
924	2180
925	3242
924	3243
925	4353
924	4354
925	5517
924	5518
925	6742
924	6743
925	8036
924	8037
925	9413
924	9414
925	10886
924	10887
925	12478
924	12479
925	14213
924	14214
925	16140
924	16141
925	18320
924	18321
925	20882
924	20883
925	24085
924	24086
925	28867
924	28868
923	28869
925	28870
924	28871
4094	1
924	2
…	…

Table 136: STS_BC0 Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
0	0	0	0	Bunch Crossing Counter – BXN [11:0]												FR1
Orbit Counter – OC [15:0]																FR2

Here:

- BXN [11:0] – Bunch Crossing counter (1…4095) ;
- OC [15:0] – Orbit Counter (1…65535).

STS_CA – Chip Acknowledge Status

This read-only register returns current state of the ACK [7:1] bus and latched state of the Acknowledges bus during last IDTB command. The register address is valid for the VME_FPGA. The current ACK [7:1] state should always be zero, if there are no shorts on the board.

Table 137: STS_CA Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ACK7	ACK6	ACK5	ACK4	ACK3	ACK2	ACK1	0	ACKL7	ACKL6	ACKL5	ACKL4	ACKL3	ACKL2	ACKL1	0
Current ACK State								Latched ACK State							

Here:

- ACK [7:1] – current state of the Acknowledge bus;
- ACKL [7:1] – latched state of the Acknowledge bus during last IDTB command.

STS_CCB – Fast Control Command bus Status

This read-only register returns current state of the SP internal Fast Control Command bus. The register address is valid for FRONT_FPGA. The current bus state should always be zero, if there are no shorts on the board. See the CCB Interface section for a list of Fast Control Commands.

Table 138: STS_CCB Data Format for FRONT_FPGA and SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	FCC5	FCC4	FCC3	FCC2	FCC1	FCC0	0	0	FCP5	FCP4	FCP3	FCP2	FCP1	FCP0
		Current FC State								Previous FC Command					

Here:

- FCC [5:0] – current state of the Fast Control Command bus;
- FCP [5:0] – previous Fast Control Bus Command;

STS_CD – Chip Data Status

This read-only register returns last data read out over the Internal Data Transfer Bus (IDTB) from F1/F2/F3/F4/F5/DD/SP chips. The register address is valid for the VME_FPGA only.

Table 139: STS_CD Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
IDTB Read Data															

Here:

- CD [15:0] – chip data from the last IDTB read command.

STS_MWA – MS Winners Analyzer

This analyzer allows determining a timing position of the Muon Sorter Winner bits, when the TF crate is in L1_STOP state and the MS provides a training pattern for the SP. A training pattern is a 40.08 MHz positive square wave. The training pattern can also be thought of as a 80Mbit/sec sequence of logical ONES (frame 1 of a 40 MHz reference clock) and ZEROS

(frame 2). The analyzer uses 4 sampling points per frame to determine position of frames' boundaries. Figure below shows typical position of winner bits for the MS2004:

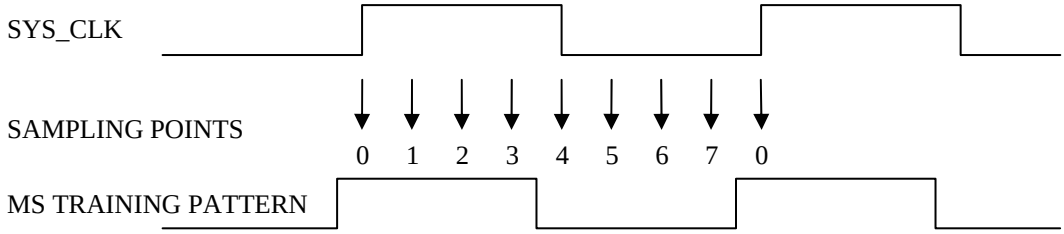


Figure 5: MS2004 Winner bit typical position

A typical value the analyzer returns is 0x0F0F, and sometimes 0x1F1F. The latter tells us that the duty factor of the training pattern is a little bit more than 50%. So, the optimal CSR_MWC setting is 2.

Table 140: STS_MWA Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MWM7	MWM6	MWM5	MWM4	MWM3	MWM2	MWM1	MWM0	MWL7	MWL6	MWL5	MWL4	MWL3	MWL2	MWL1	MWL0
MS Winner MSB								MS Winner LSB							

Here:

- MWL [7:0] – MS Winner LSB sampled at 8 phases of the SYS_CLK clock (7/8, 6/8, 5/8, 4/8, 3/8, 2/8, 1/8 and 0/8 of the SYS_CLK period);
- MWM [7:0] – MS Winner MSB sampled at 8 phases of the SYS_CLK clock (7/8, 6/8, 5/8, 4/8, 3/8, 2/8, 1/8 and 0/8 of the SYS_CLK period).

STS_VAH – VME High Address Status

This read-only register returns latched address bits of the last VME command seen on the backplane. The register address is valid for the VME_FPGA only.

Table 141: STS_VAH Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	GA4	GA3	GA2	GA1	GA0	0	0	0	SA4	SA3	SA2	SA1	SA0
			GA [4:0]								Slot Address – SA [4:0]				

Here:

- GA [4:0] – Geographical Address;
- SA [4:0] = VME_A [23:19] – Slot Address.

STS_VAL – VME Low Address Status

This read-only register returns latched address bits of the last VME command seen on the backplane. The register address is valid for the VME_FPGA only.

Table 142: STS_VAL Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	CA6	CA5	CA4	CA3	CA2	CA1	CA0	0	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	Chip Address - CA [6:0]								Register Address - RA [6:0]						

Here:

- CA [6:0] = VME_A [18:12] – Chip Address;
- RA [6:0] = VME_A [8:2] – Register Address.

STS_VAM – VME Medium Address Status

This read-only register returns latched address bits of the last VME command seen on the backplane. The register address is valid for the VME_FPGA only.

Table 143: STS_VAM Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	AM5	AM4	AM3	AM2	AM1	AM0	0	A11	MA1	MA0	RD	0	A1	A0
		Address Modifier – AM [5:0]								MA [1:0]					

Here:

- AM [5:0] – Address Modifier;
- A11 = VME_A[11] line status;
- MA [1:0] = VME_A [10:9] – Muon Address;
- RD = not VME_WRITE* line status;
- A1 = VME_A[1] line status;
- A0 = not VME_LWORD* line status.

History

Version 5.0 – Sep 01, 2003

1. Clock routing changed due to patches:
   - Eliminated the osc_clk input in the VME_FPGA;
   - Eliminated the clk_sel input in the VME_FPGA;
   - Returned two DCMs: internal and external to the VME_FPGA;
   - Eliminated the CSR_CLK register in the VME_FPGA;
   - Changed default value of the CSR_CLK register in the FRONT_FPGA from DCM to VCXO clock;
2. Changed the CCB_BC0 to DATA_BC0 adjustment scheme:
   - Eliminated the CSR_CCB register in the VME_FPGA;
   - Added the CSR_BCO register in the FRONT_FPGA (with the same access address);
   - Changed format of the CSR_OSY registers in the FRONT_FPGA, now it displays the latched bunch counter value without calculating positive/negative offsets;
3. Added data taking state diagrams in the interface description;
4. Added the STS_VPC (Valid Pattern Counter) register for each link in the FRONT_FPGA;
5. Renamed ACT_LER – Link Error Counters Resets to ACT_LCR – Link Counter Resets, added the VPR bit to reset the STS_VPC counter;
6. Fake L1Accept generated by CCB_TPxxx commands is ORed with the CCB_L1A line BEFORE the L1Accept delay, not AFTER;
7. Added intercept of the CCB_TPTMB(0x24) command;
8. Changed the CSR_SFC format in the VME_FPGA;

Version 5.1 – Nov 25, 2003

1. Changed the usage of the 39 and 3A access codes, Table 5. Previously identical data and program access is now split according to its function.
2. Changed the IDTB protocol from synchronous with a handshake to synchronous with a predetermined timing.
3. Added the CSR_BF(0x36) and DAT_BF(0x76) registers for the Barrel FIFO, Table 10;
4. Added the BF reset bit in the ACT_XFR, Table 25;
5. Added the ACT_ACR register description;
6. Changed the CSR_LF address from 0x36 to 0x37, Table 10;
7. Changed the CSR_RBW address from 0x37 to 0x38, Table 10;
8. Changed the CSR_RBR address from 0x38 to 0x39, Table 10;
9. Eliminated the CNT_GEL/CNT_GEH/CNT_GPL/CNT_GPH registers description;

10. Added the CNT_GLL/CNT_GLH registers description.

Version 5.2 – Dec 10, 2003

1. Added the DAT_GP register description;
2. Added the DAT_DT register description;
3. Added the DAT_GE register description.

Version 5.3 – Dec 25, 2003

1. Added the CNT_PTL/CNT_PTH registers description;
2. Added the DAT_PT register description;
3. Modified the ACT_ACR register description;
4. Modified the CSR_AFD register description;
5. Added the CSR_TFC register description;
6. Completely redefined CSR_OSY for FRONT_FPGA.

Version 5.6 – Mar 8, 2004

1. Added the CSR_F1/CSR_F2/CSR_F3/CSR_F4/CSR_F5 registers description;
2. Added the DAT_F1/DAT_F2/DAT_F3/DAT_F4/DAT_F5 registers description;
3. Eliminated the STS_CCB register description;
4. Changed the STS_ANA register description;
5. Added the ACT_FCC register description;
6. Eliminated the ACT_TST register description, the ACT_FCC took over this register;
7. Added the CSR_FCM register description;
8. Changed the CSR_TFC register description;
9. Eliminated the CSR_L1D register description since this the CCB function;
10. Restricted access to DAT_LP, DAT_GP, DAT_DT, DAT_GE, DAT_PT, DAT_ETA, and CSR_SCC registers

Version 5.7 – Jun 1, 2004

1. Changed the STS_ANA register description;
2. Added description of the QPLL lock LED;
3. Changed link data logic; now link data passes through SP logic unconditionally.
4. Changed the CCB_CMD to FC_CMD mapping.
5. Added STS_BCO - Bunch Crossing Analyzer

Version 6.0 – Nov 15, 2004

1. Migrated to SP04 board

Version 8.0 – April 24, 2006

1. Initial release with new DDU readout format

Version 8.1 – May 16, 2006

1. Moved timing control bit from FA/CSR_FCC into FA/CSR_TFC
2. Moved timing control bit from SP/CSR_FCC into SP/CSR_TFC
3. Moved readout control bit from DD/CSR_FCC into DD/CSR_DFC
4. Split and moved DT loopback bit from SP/CSR_FCC into SP/CSR_TBC
5. Added Q to DT_Q and CSCID to DT_ETA mapping tables

Version 8.2 – June 14, 2006

1. Added VM/STS_VAL, VM/STS_VAH, VM_STS_VAM registers
2. Changed ACT_XFR/D4 bit description
3. Added DD/ACT_XFR/D5 bit

Version 8.3 – July 1, 2006

1. Changed fc_cmd bit assignment in Table 2
2. Modified SP/CSR_AFD, added ME delay, change access to MA only
3. Added Test pattern injection on L1A option for VM/CSR_TFC

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[i] CSC Track Finder Crate Specification, created by Mike Matveev and updated by Alex Madorsky, December 12, 2002; http://www.phys.ufl.edu/~madorsky/TrackFinder/TF_backplane_v4.doc
[ii] ANSI/VITA 1.1-1997, American National Standard for VME64 Extensions.