Update on SP02 firmware design

Alex Madorsky
University of Florida

Trigger Meeting at Rice
August 2002

SP02 firmware design status

V++ model in now completely up to date.

New features added:

- **7 bit Eta input**
- **DAQ output bits – SP outputs parameters of the track stubs for the best three tracks**
- **Ghost busting**
- **Bunch Crossing Analysis (BXA)**
- **CSC ID inputs**
- **AMU and FR bits generated internally from CSC ID**

SP02 firmware design status

To be done:

- Extensive performance checking
- DAQ interface
- Firmware for the front FPGAs