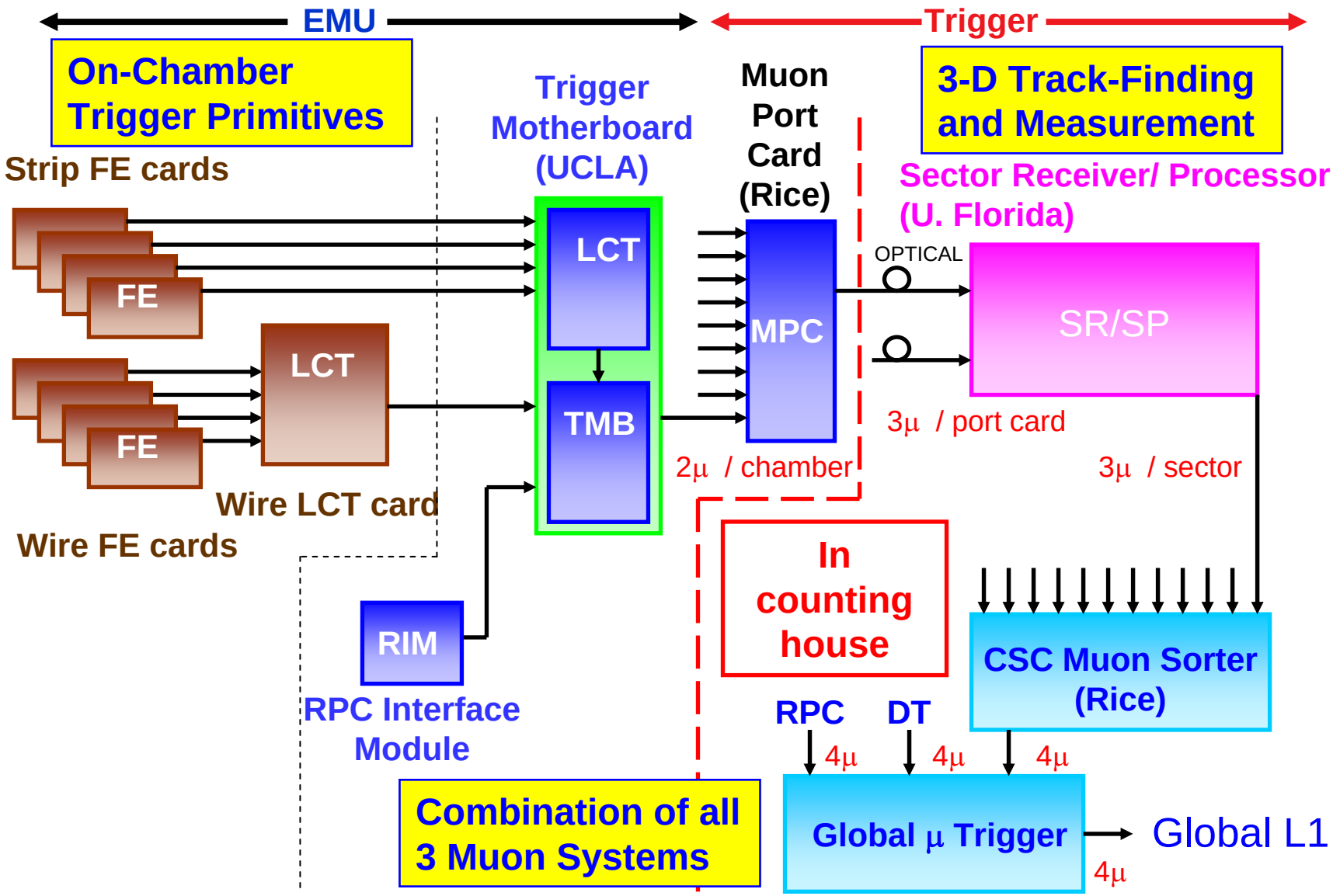
CSC Track-Finder

http://www.phys.ufl.edu/~acosta/cms/trigger.html

Darin Acosta

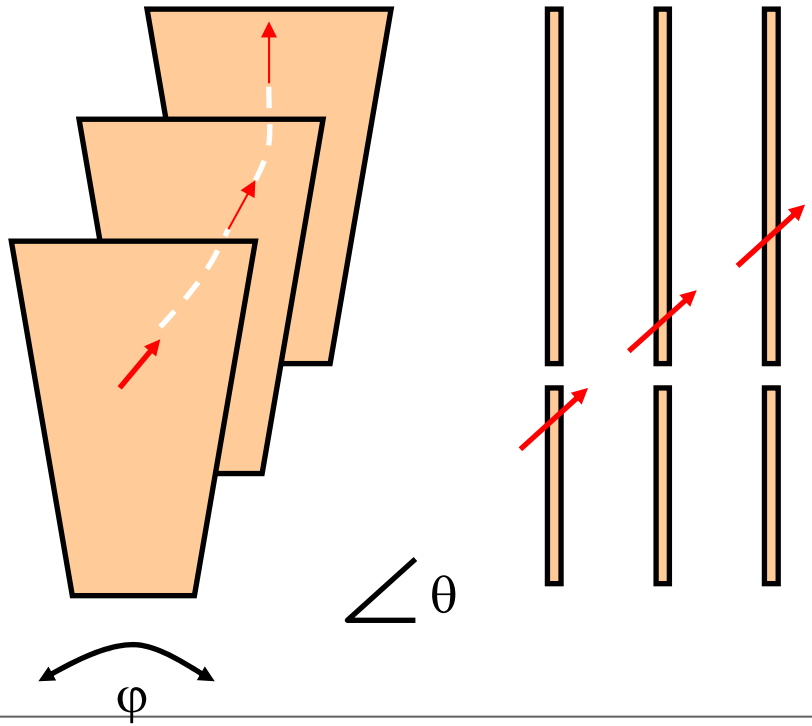
University of Florida

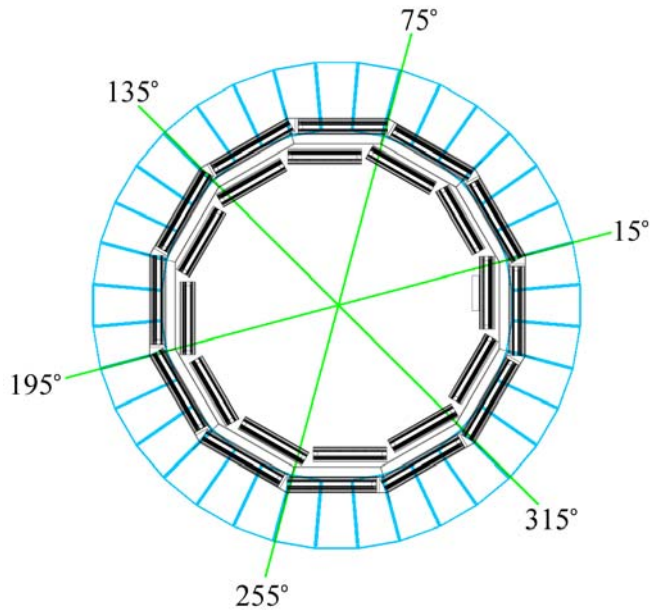
CSC Muon Trigger Scheme



CSC Track-Finding

- Link local track segments into distinct 3D tracks (FPGA logic)
  - Reconstruction in η suppresses accelerator muons
- Measure p_T, φ, and η of the muon candidates in the non-uniform fringe field in the endcap iron (SRAM LUTs)
- Send highest quality candidates to Global Muon Trigger
  - Partitioned into 60° sectors that align with DT chambers

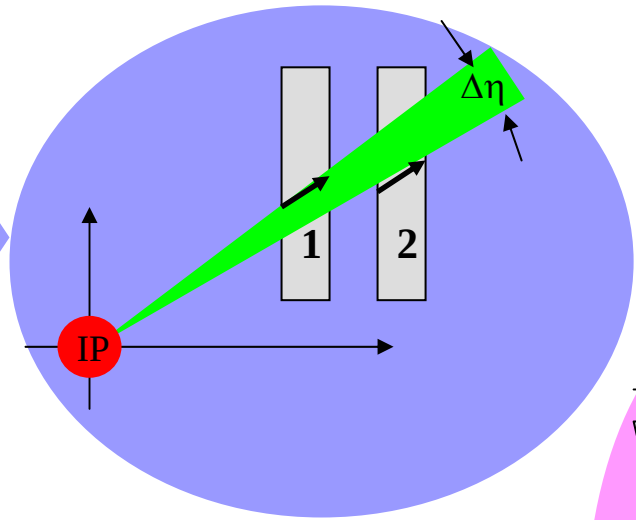




Basis of Track-Finding Logic

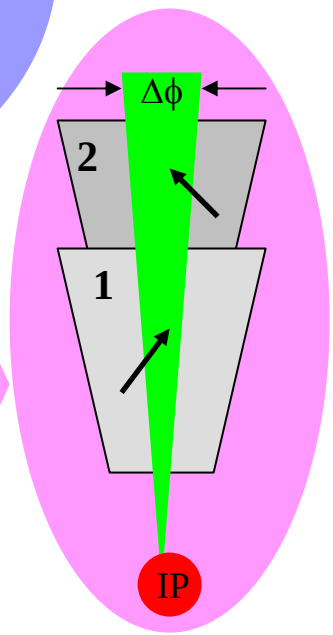
η Road Finder:

- Check if track segment is in allowed trigger region in η.
- Check if Δη and η bend angle are consistent with a track originating at the collision vertex.



ϕ Road Finder:

- Check if Δϕ is consistent with ϕ bend angle ϕ_B measured at each station.
- Check if Δϕ in allowed range for each η window.

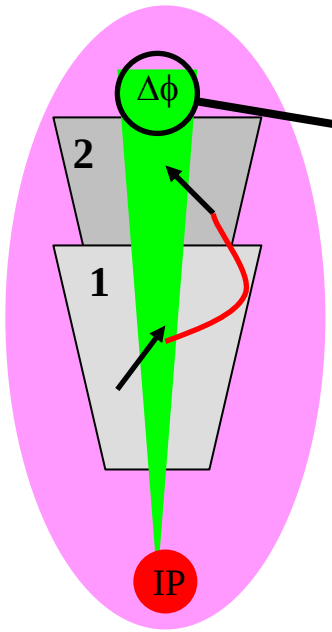


Quality Assignment Unit:

- Assigns final quality of extrapolation by looking at output from η and ϕ road finders and the track segment quality.

Extrapolation Units utilize 3-D information for track-finding.

P_T Measurement



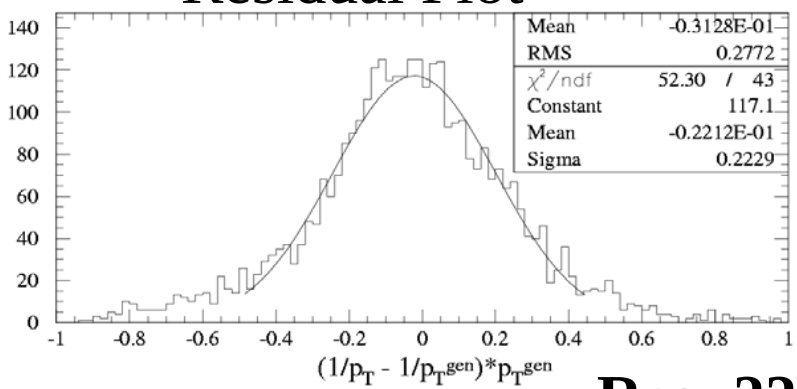
Pt LUT

4 MB

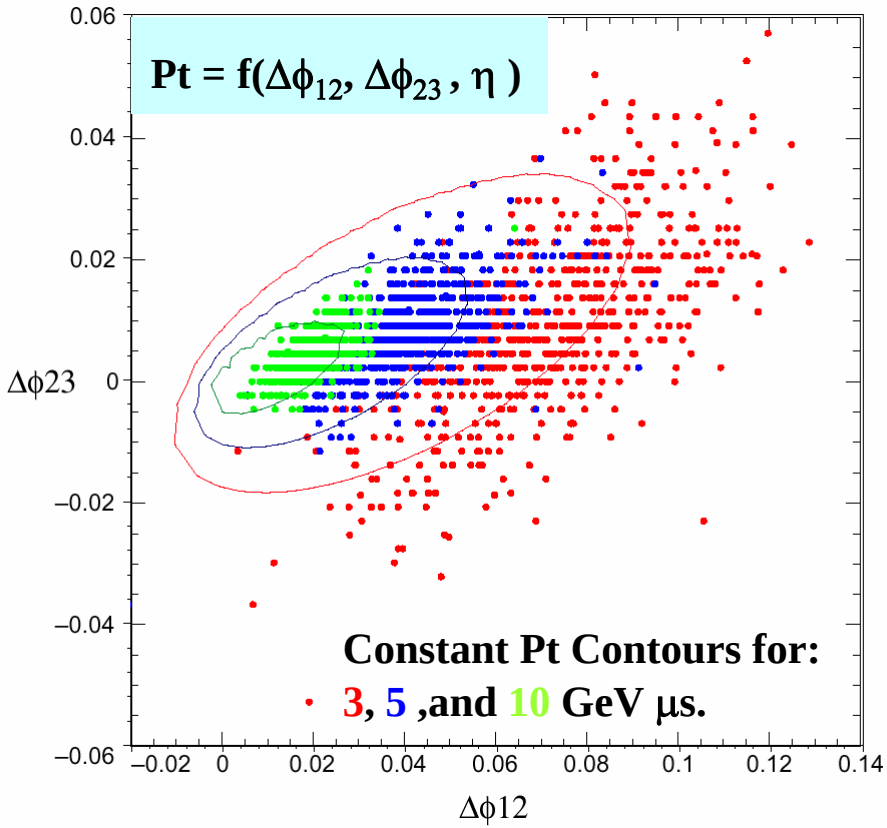
P_T

Can use information from up to 3 chambers

Residual Plot



Res=22%



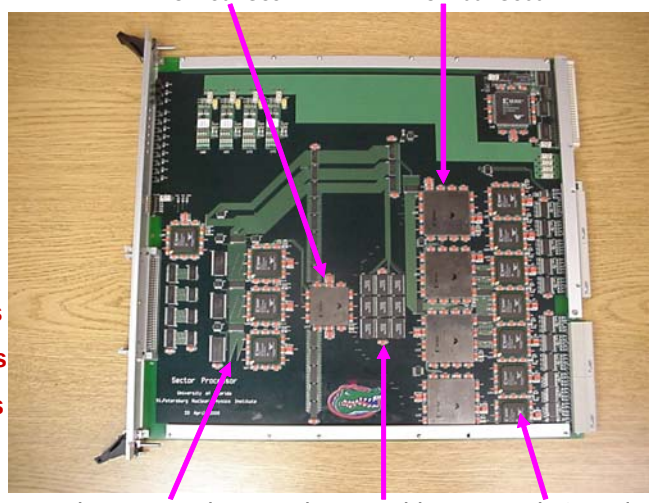
1st Track-Finder Prototypes

Sector Processor Prototype

Florida

Final Selection Unit XCV150BG352

Extrapolation Units XCV400BG560



12 layers
10K vias
17 FPGAs
12 SRAMs
25 buffers

Assignment Units XCV50BG256 & 2M x 8 SRAM

Track Assemblers 256k x 16 SRAM

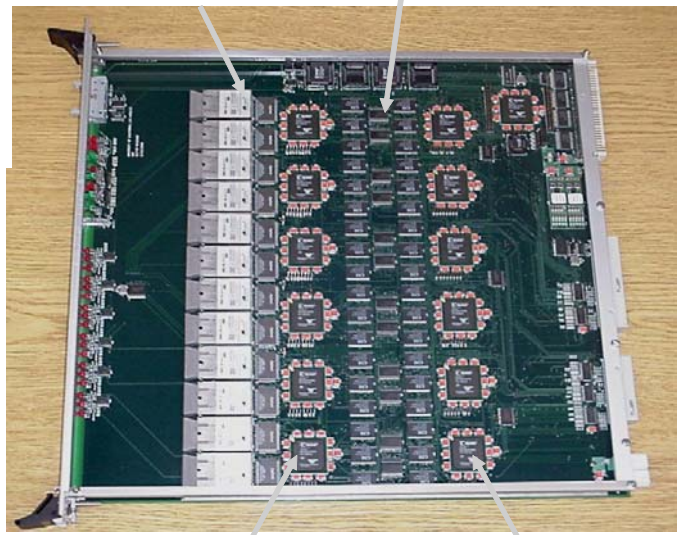
Bunch Crossing Analyzer XCV50BG256

Sector Receiver Prototype

UCLA

Optical Receivers and HP Glinks

SRAM LUTs



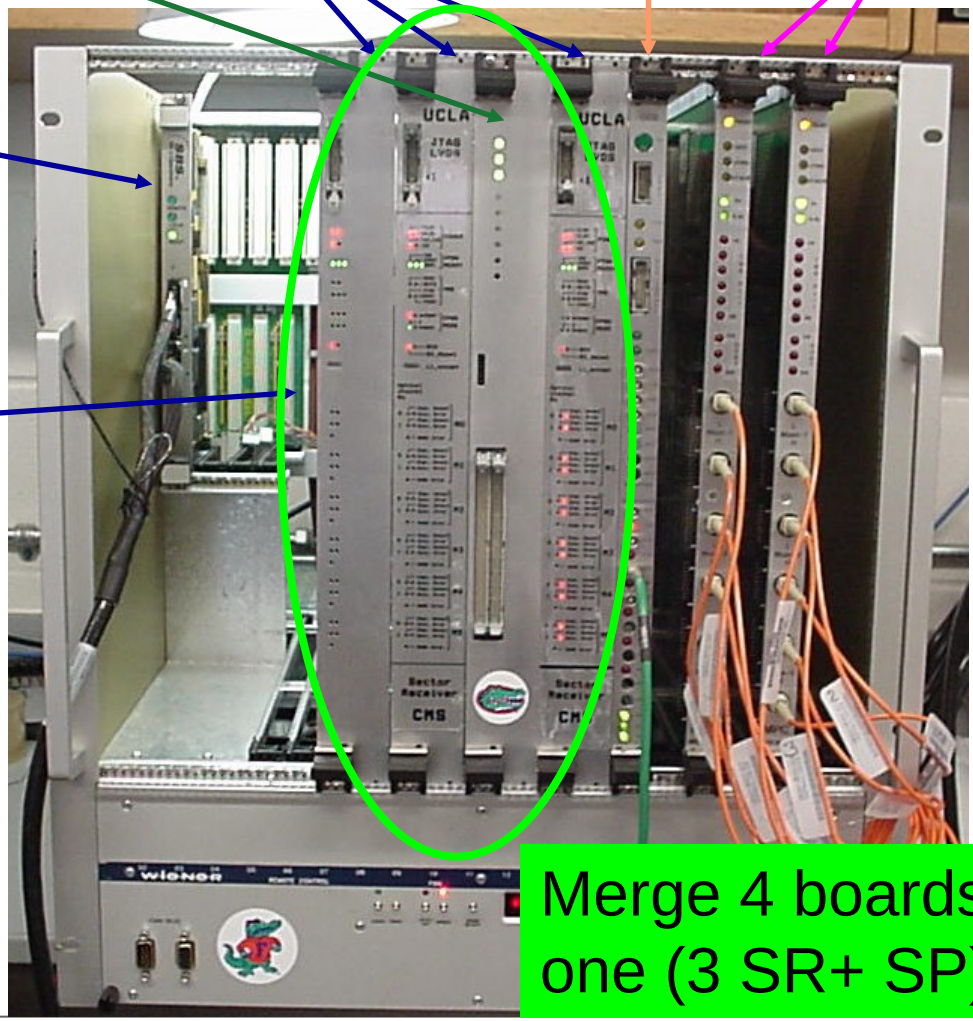
Front FPGAs

Back FPGAs

Tested in 2000

System would require 6 crates

1st Prototype Track-Finder Tests



Very successful, but overall CSC latency was too high

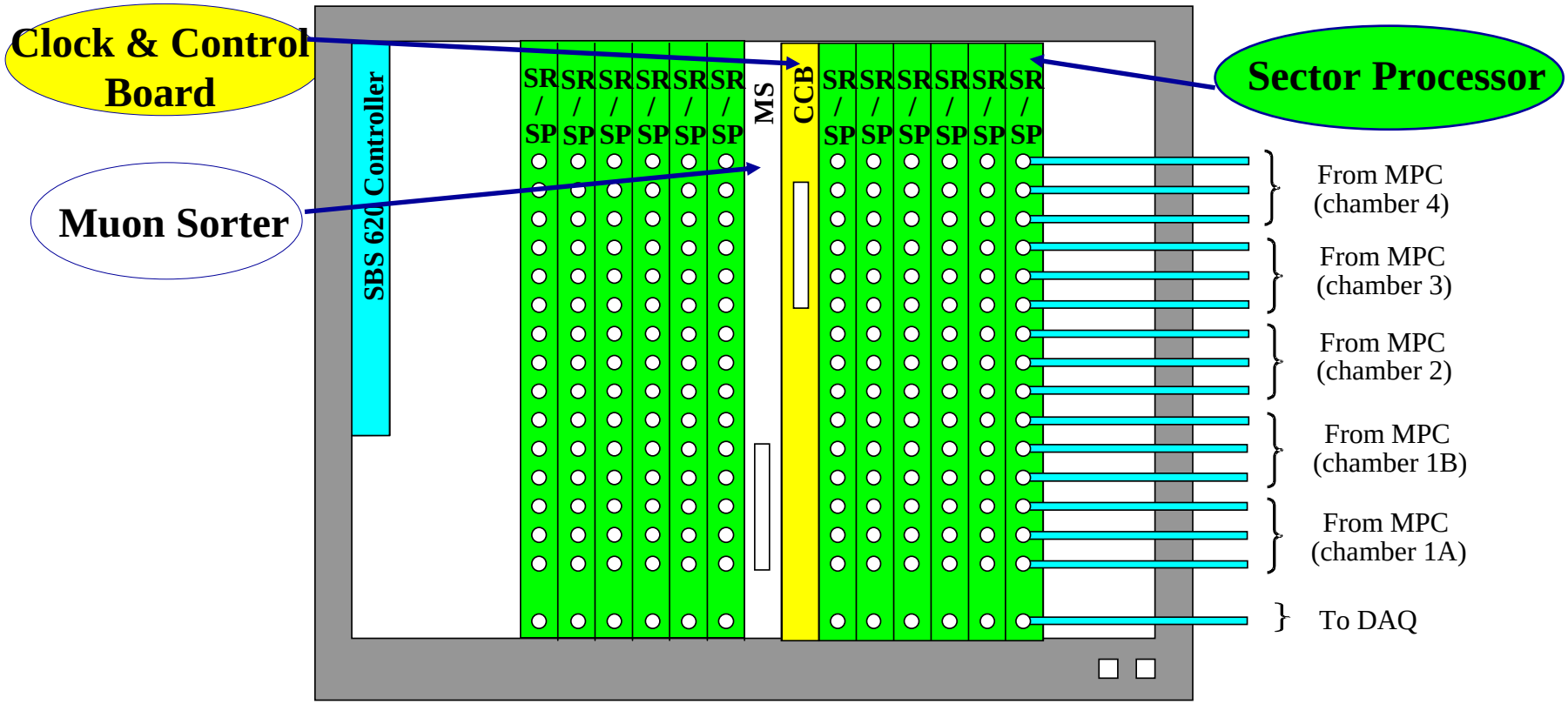
Second design improves latency

Test Results included in Trigger TDR (2000) & NIM A496 (2003) 64

Merge 4 boards into one (3 SR+ SP)

CSC Track-Finder Crate

Single crate solution, 2nd generation prototypes under test



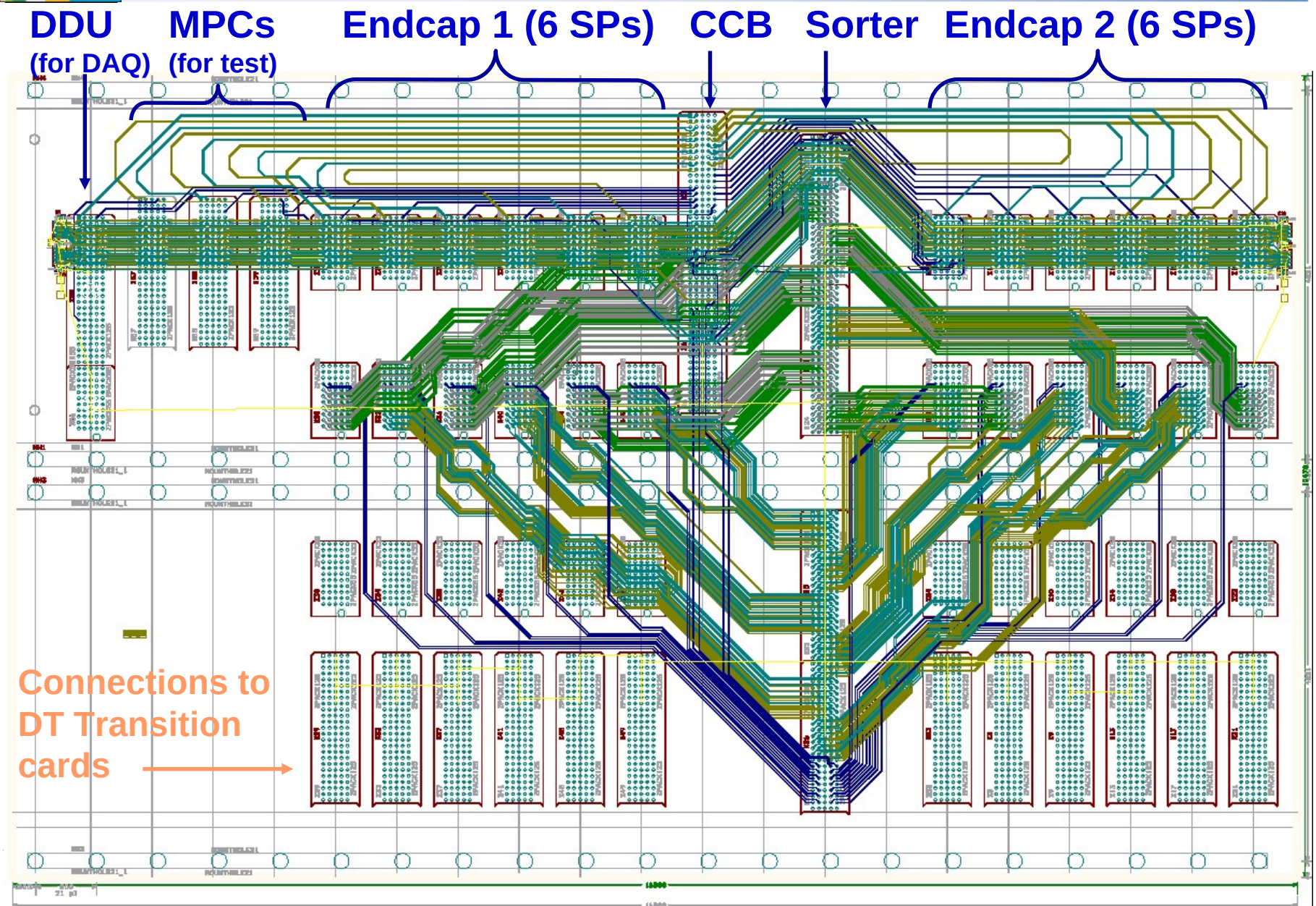
180 × 1.6 Gbit/s optical links:

Data clocked in parallel at 80 MHz in 2 frames (effective 40 MHz)

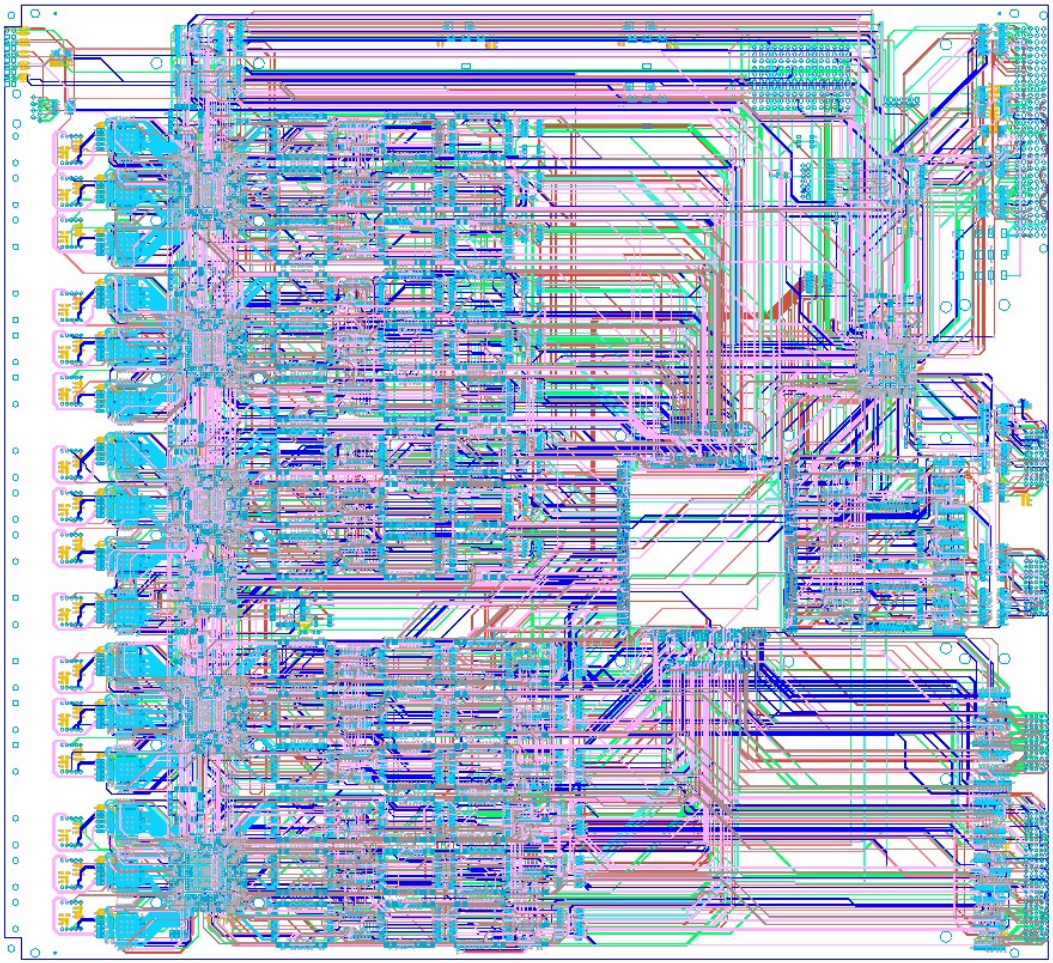
Custom 6U GTLP backplane for interconnections (mostly 80 MHz)

Rear transition cards with 40 MHz LVDS SCSI cables to/from DT

CSC Track-Finder GTLP Backplane

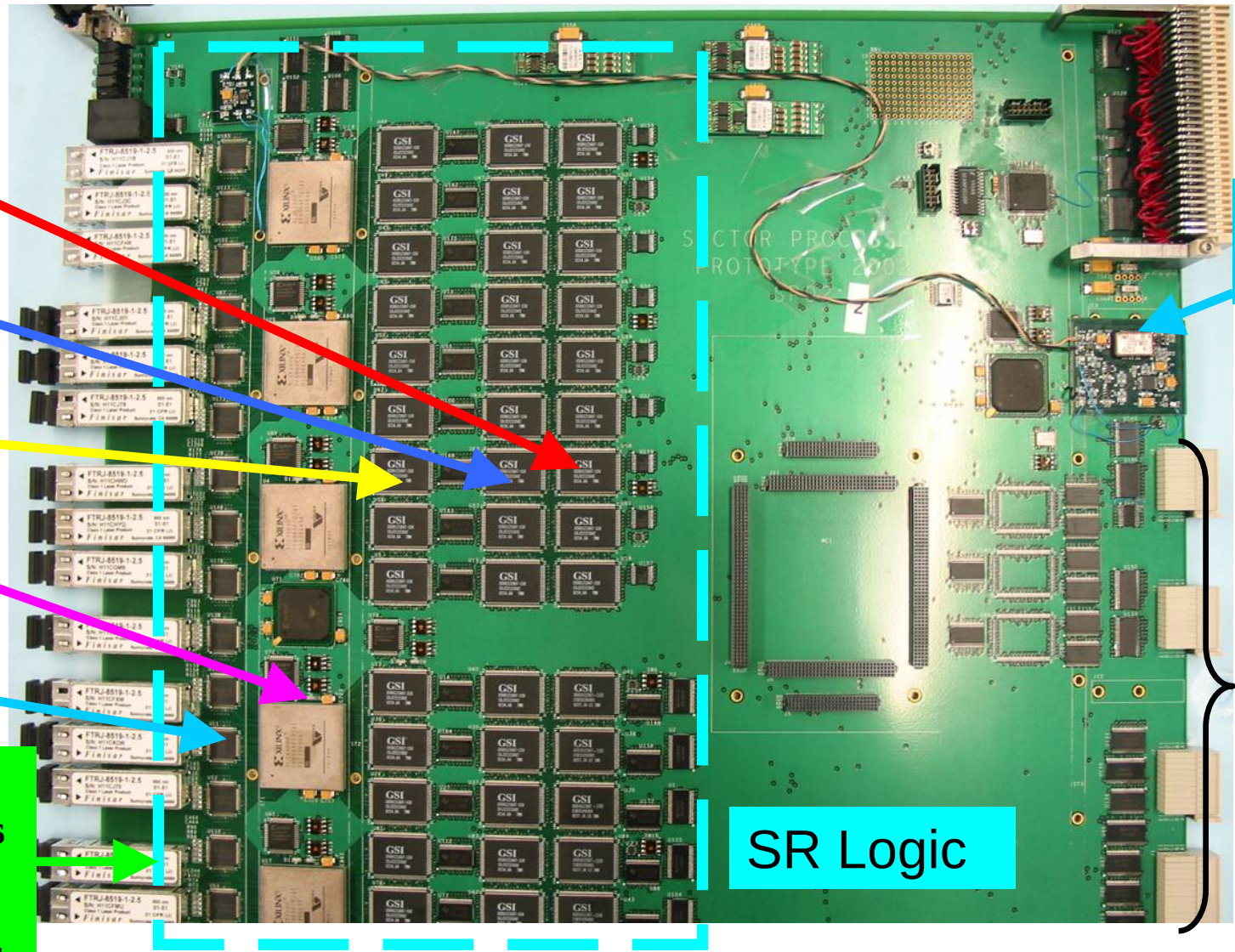


Combined SR/SP 2002

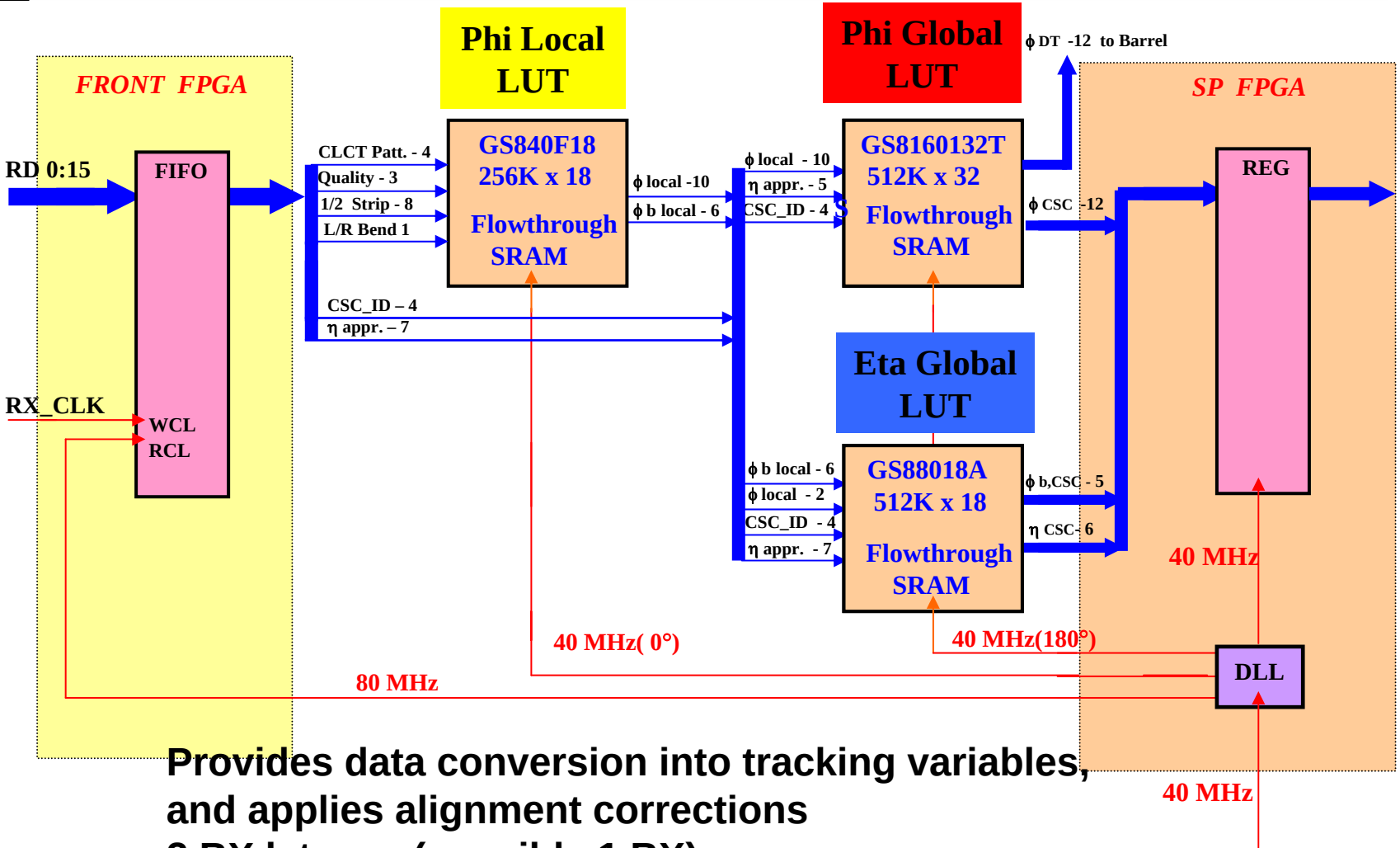


- 4 boards in 1
- Delays with complex layout using in-house tools
- Sent to industry for completion of layout using Cadence Allegro
  - Since then acquired Allegro license at UF
- Final board takes 16 layers
- 3 boards manufactured and stuffed
- Testing began Mar. ‘03

SP2002 Main Board (SR Logic)



SR Memory Scheme



Provides data conversion into tracking variables, and applies alignment corrections
2 BX latency (possibly 1 BX)
45 LUTs (only 11 distinct per SR/SP), >40MB
Can multicast when loading chips, boards

SP2002 Track-Finder Logic

SP2002 mezzanine card

- Xilinx Virtex-2 XC2V4000 ~800 user I/O
- Same mezzanine card is used for Muon Sorter
- Track-Finding logic operates at 40 MHz
  - Frequency of track stub data from optical links
- About 50% of chip resources (LUTs) used
- Easily upgradeable path

SP Firmware

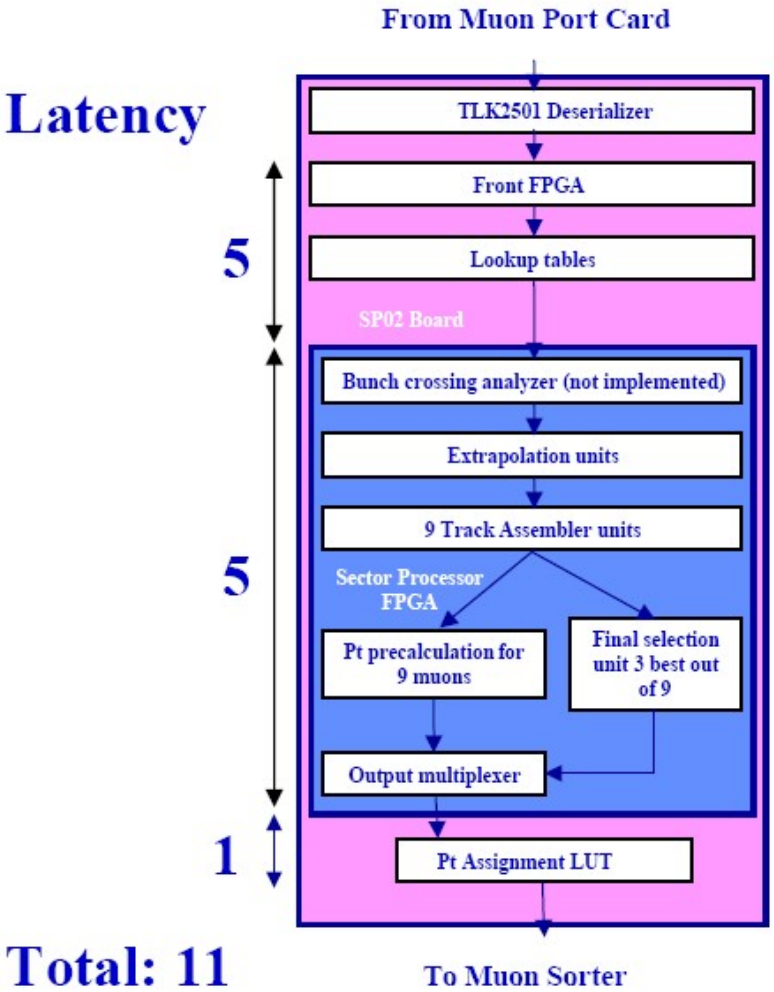
- **FPGA firmware is synthesized from Verilog**
  - **Top-level schematic connects Verilog blocks**
- **Core track-finding logic is actually written in C++ and converted to Verilog using a special C++ class library written by our engineer, A.Madorsky**
  - **Two compiler options for one piece code:**
    - **Compiled one way, the C++ program self-generates Verilog output files which are human-readable and from which can be synthesized by the FPGA vendor tools**
    - **Compiled another way, the same code exactly emulates the behavior the digital logic**
  - **Solves main obstacle to validation of the first TF prototypes**
  - **Allows use of free compiler tools on commodity PC's for debugging**
    - **Still need vendor simulation tools for other FPGAs**
  - **This SP logic is implemented in the ORCA simulation and reconstruction framework and is now the default (≥7.7.0)**

Recent Updates to Track-Finder Logic

- **Firmware improvements**
  - Multiple-BX input acceptance for track segments
    - Improves efficiency
  - Track-Finding parameters under VME control (e.g. η windows)
  - Error counters, track segment counters, track counters for monitoring
  - Ghost-busting at sector boundaries
    - Increases di-muon trigger acceptance to $|\eta|<2.4$ when low quality CSC tracks included
    - Installed into ORCA
- **Self-trigger capability**
  - A Level-1 Accept signal can be generated based on the presence of a track for beam test use
  - Goes onto bussed backplane to CCB, then out front-panel

CSC Track-Finding Logic & Latency

SP02 Simulated Timing



11 × 25 ns, or 275 ns

Big improvement over 1st prototypes (21 bx)

CSC Trigger Latency

- **Measured with scope during the beam tests:**
  - From CSC to MPC input: 32 bx (± 1 bx)
  - From the CSC to SR/SP input: 57 bx
    (includes 90 m fiber, 18 bx delay)
- **Estimated latency for output of SP:**
  - Add 11 bx for SR/SP processing: 68 bx
- **Estimated latency for output of Muon Sorter:**
  - Add 7 bx for backplane + sorting: 75 bx
- **Total compares well with 74.5 bx projected in TDR**
  - (Latter includes 1 bx TOF delay)
- **Expect to save additional ~7 bx with "Virtex-2" TMB**
- **Estimated latency to send CSC data to DT TF:**
  - 1bx TOF + 57bx + 5bx for SR + 2bx cable: 65 bx – 7 bx = 58 bx
  - Nearly aligned with DT data at DT TF: 54 bx according to TDR

Test Status

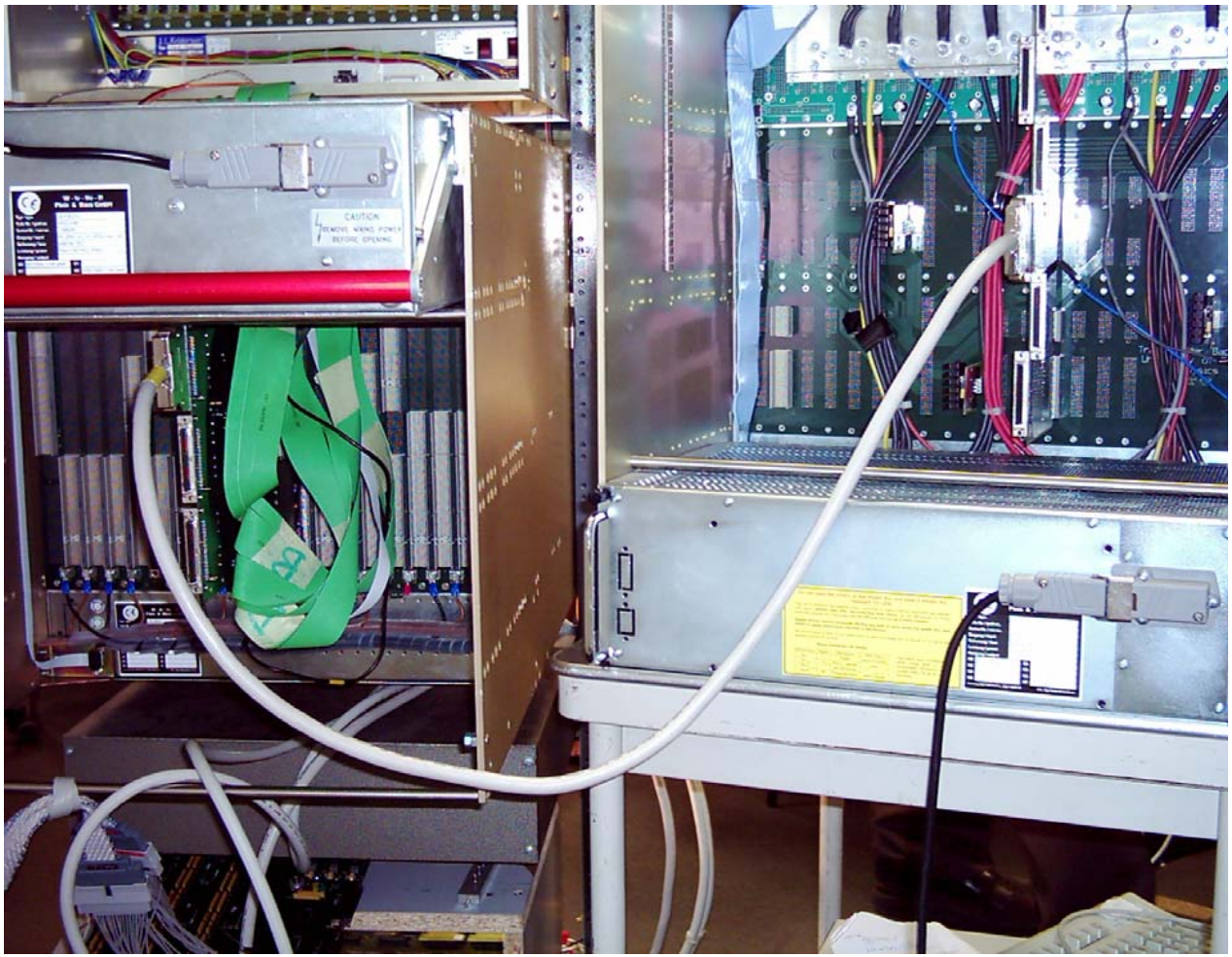
- **Basically all functionality has been successfully tested**
- **Optical links:**
  - **Demonstrated to maintain synchronization during Sept'03 beam test with home-built PLL+VCXO and with latest QPLL (TTCRq)**
- **LUT Tests:**
  - **Validated loading and read-back of all 45 SR LUTs and 3 PT LUTs using random numbers and simulated muon LUT files**
- **SP Track-Finding Logic Tests:**
  - **Downloaded random data and simulated muon data into 512 BX input FIFO, read-back and compare output FIFO**
  - **No discrepancies in 1.2M random events**
  - **No discrepancies in 13K single muon events, or 4K triple muon events (3 single muons piled up)**
  - **Verilog model also "installed" into ORCA**
- **Complete functionality test**
  - **Input FIFO → Optical loopback → Front FPGA → LUTs → Track-Finding → output FIFO (all 15 links)**

Interface Tests

- **MPC to Sector Processor**
  - Validated with optical link tests
- **SP to Muon Sorter Test**
  - Data successfully sent from SP to Muon Sorter and received properly. Read-back of winner bits also correct.
  - Tested 10/12 slots on custom GTLP backplane
- **Clock and Control Board (TTC interface)**
  - New design based on discrete logic and with TTCRq installed still needs to be tested (beginning April)
- **DT/CSC Data Exchange Test**
  - Demonstrated to work during Sept'03 in both directions, with only a few minor problems with swapped bits, connectors, and dead chips

First DT/CSC Integration Tests

DT TF transition card ↔ CSC TF transition card

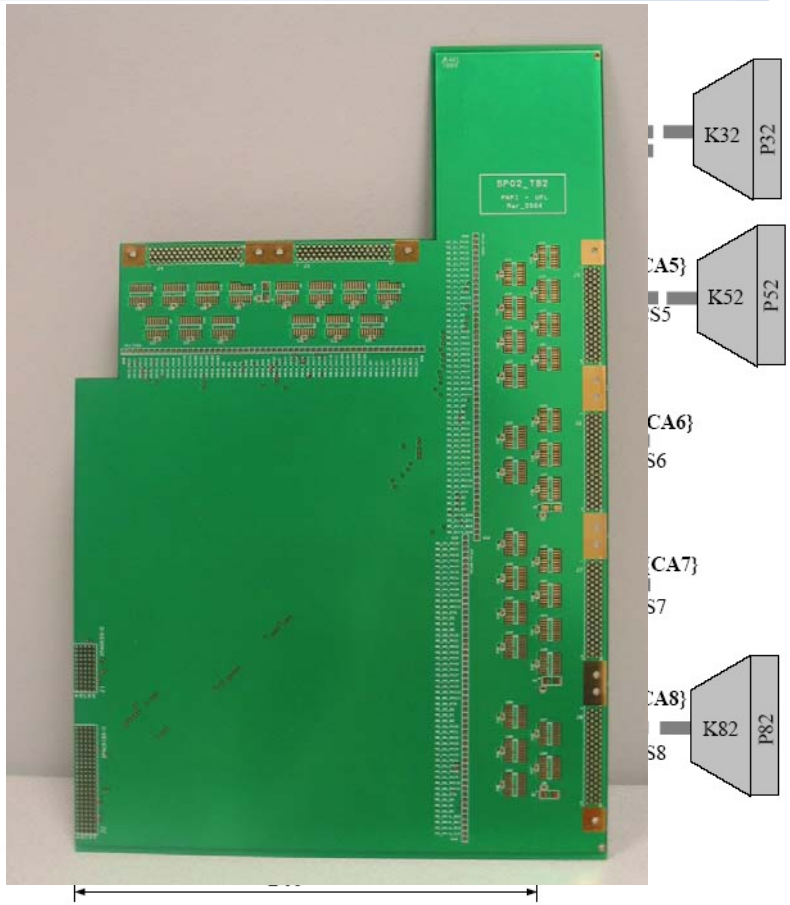


DT/CSC interface

- **Reminder: data is exchanged between the two systems for efficient coverage of the region $0.9 < |\eta| < 1.2$**
  - **Interface document: CMS IN 2002/040**
  - **CSC sends 3 LCT's/BX (52 bits) from ME1 to two 30° DT sectors**
  - **DT sends 1 segment/BX (26 bits) from each 30° sector**
  - **Signaling standard is LVDS at 40 MHz through SCSI cables and connectors**
- **Layout problem on first CSC transition card meant connectors had to be attached on opposite side of board**
  - **Cable connector had to be flipped 180° at one end so that signals are received on correct pins**
  - **Anyway, have to redesign anyway because SCSI connectors on two sides exceeds single VME slot width**

New DT/CSC Transition Board Layout

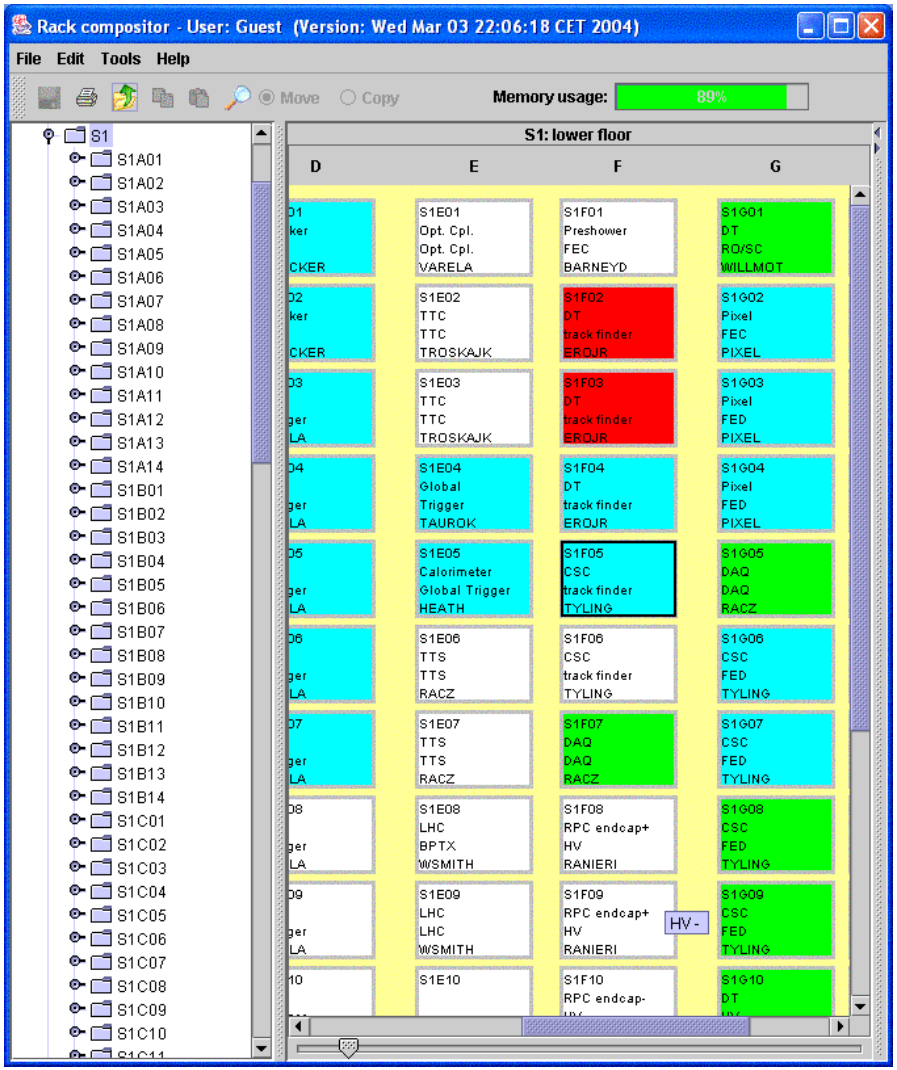
- SCSI connectors on one side of card
- Ability to perform self-test with tester card
- Fabrication completed this week
- Plan another DT/CSC interface test in Oct'04

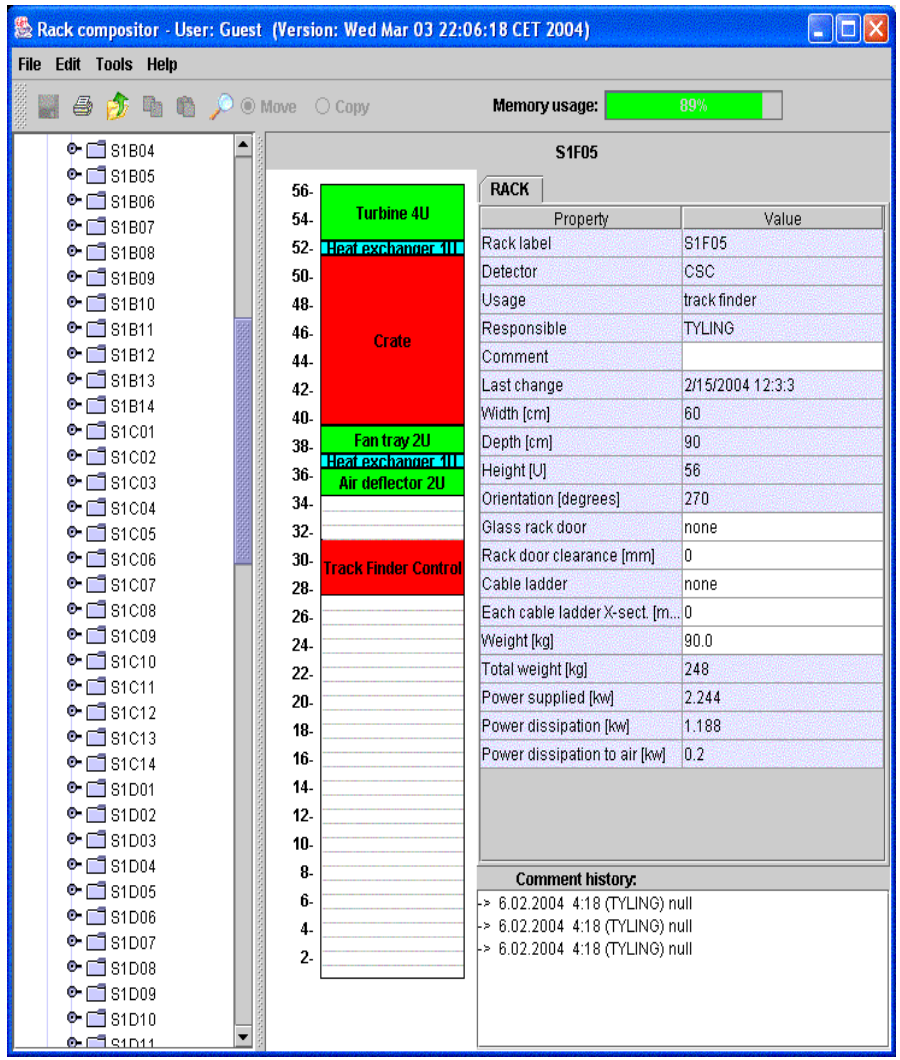


J3÷J8: AMP787190-7 – Amplimite Connector, 68 Cont
{CA3}, {CA4}: P31 ÷ P42 - P4AMP749621-7 –Amplimite Plug Assembly, 68 Pin
K31, K41 - AMP749204-2 – Amplimite Backshell Kit, 68 Pos.
K32, K42 – AMP749195-2 – Amplimite Backshell Kit, 68 Pos.
CS3, CS4 – Belden 1403A – 34 Pairs SCSI2 Cable, Non halogen
{CA5} ÷ {CA8}: P51 ÷ P82 - P4AMP749621-7 –Amplimite Plug Assembly, 68 Pin
K51 ÷ K82 - AMP749195-2 – Amplimite Backshell Kit, 68 Pos.
CS5 ÷CS8 – Belden 1403A – 34 Pairs SCSI2 Cable, Non halogen

Fig.1. CSC/DT Transition Board Connections

CSC Track-Finder Rack Layout





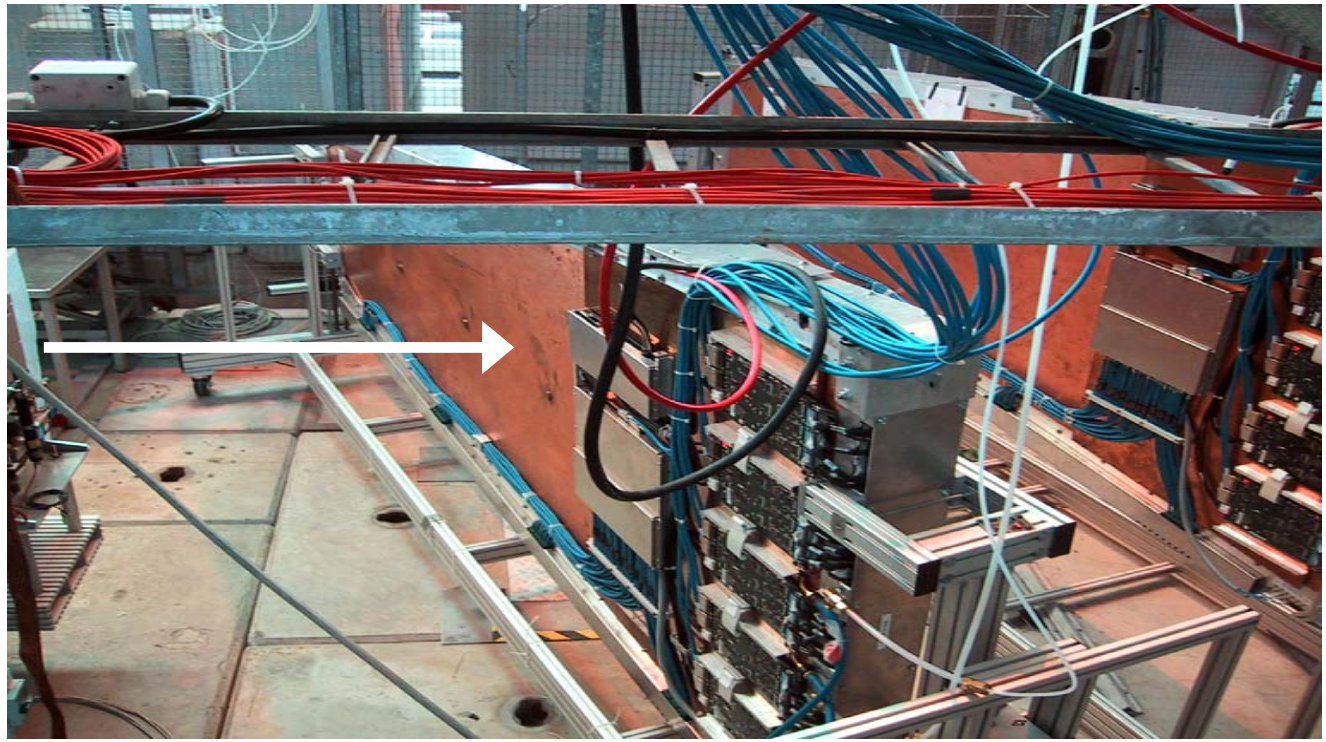
Remaining Integration Tests Required Before Production (Peripheral & Track-Finder Crate)

- Standalone test of MPC and nine production TMBs with CCB'2004 in the peripheral crate. Check data paths from TMB to MPC and winner paths from MPC to every TMB.
  - On-going
- Optical test (three links) from MPC to SP. Data check from SP's input buffers should be sufficient.
  - Possible during 2004 beam test with new CCB and TTCRq
- Multiple MPCs to SP Link test (check SP input buffers & SP logic)
  - Possible during 2004 beam test
- Multiple SP to MS data path test with at least two SP boards and winner feedback from the MS to those two SPs

Desired Tests:

- At some point we should check the MS-to-GMT data path.
- We should check the SP-to-MS data path with 12 Muon Tester (MT) boards and all 12 winner paths from MS to MT.
- TMB to MPC to SP to MS chain test with as many boards as we an manage
  - Possible during 2004 beam test
- Readout of SP through SLINK64 on EMU DDU board

2003 Beam Test of 2 CSC's at X5a



Goals:

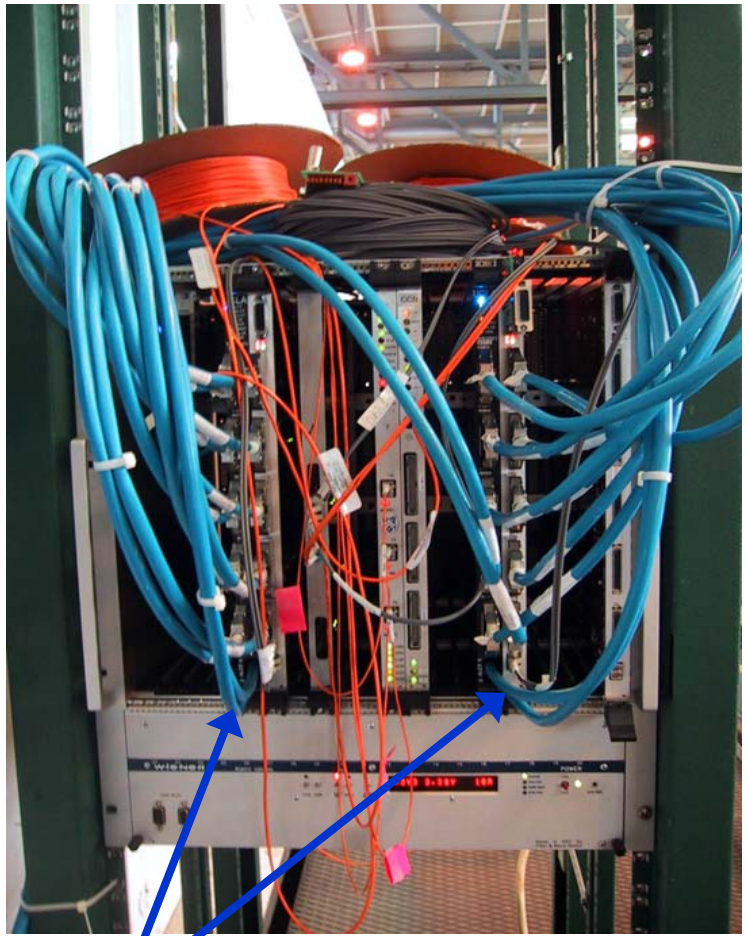
1) Verify that the peripheral crate electronics (mainly DMB/TMB) are ready for production

2) Complete an electronic chain test of data transmission from CSC front-end electronics to counting-room trigger electronics, all operating synchronously with the 40 MHz structured beam

3) Test new XDAQ-based software

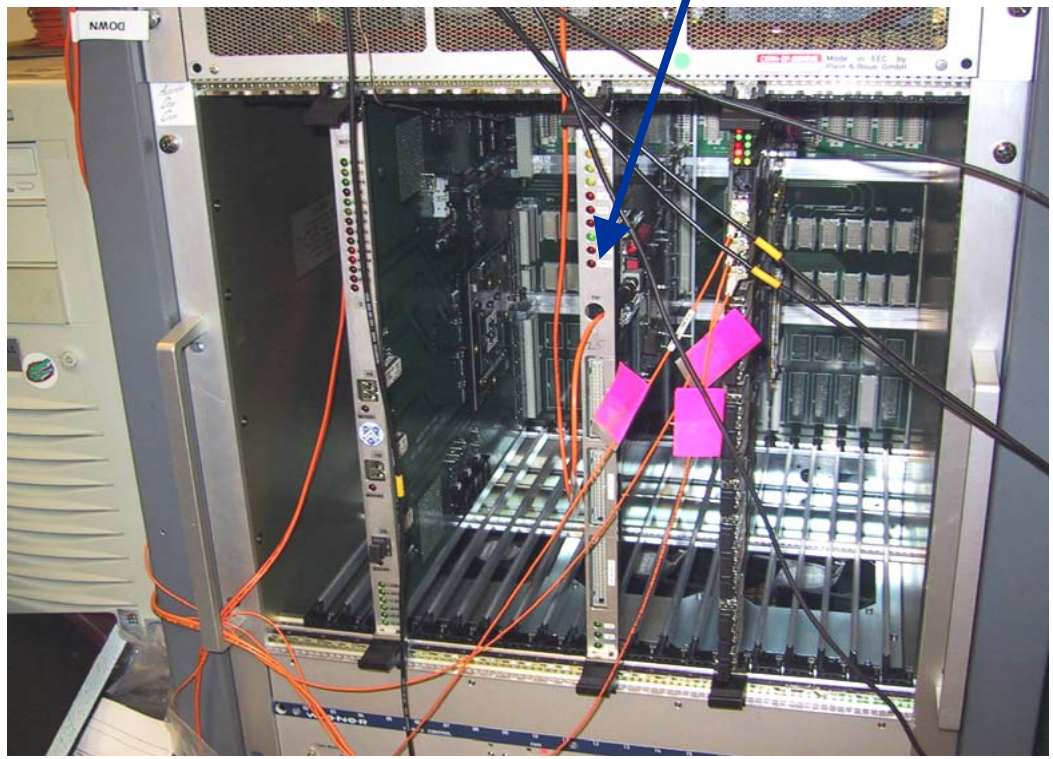
CSC Peripheral Crate

Peripheral crate



Track-Finder crate

Sector Processor, receives optical data



2 Trigger Motherboards (TMBs) for trigger primitive generation, and
2 DAQ Motherboards (DMBs) for chamber read out

TTC QPLL Mezzanine card (TTCRq)

- Three made available to CSC group for testing during Sept.03 structured beam test
- Provides stable clock signals at 40, 80, and 160 MHz at correct LHC frequency
- Installed on CCB with 40 MHz clean clock sent to backplane, 80 MHz clock sent by twisted pair to SP or MPC

TTCRq (QPLL) Test Results

1. **QPLL 80 MHz clock directly to MPC transmitters and UFL custom VCXO+PLL for SP receivers**
   - No link errors for 20 minute PRBS test
2. **QPLL 80 MHz clock directly to SP receivers MPC uses default clock multiplier**
   - No link errors for 15 minute PRBS test
   - Successfully logged data for 10K events (run 5151)
3. **QPLL 40 MHz clock on TF crate backplane SP uses DLL in FPGA for clock multiplier**
   - ***Link errors observed in PRBS test***
4. **TTCRq on CCB in peripheral crate TTCRm on CCB in TF crate**
   - Able to take data with same trigger efficiency (i.e. TTCRq works for peripheral crate as well)

Detailed TMB–SP Comparison

- **Run TMB data (correlated LCT trigger primitives) through MPC simulation to compare with SP**
  - **MPC is not directly read out**
  - **MPC sorts possible 4 LCTs to 3 in beam test data**
  - **Use BXN reported by ALCT for each LCT**
- **Preliminary comparison between SP and TMB for all 5 BX read out by SP for every L1A match:**
  - **99.7% agreement for ~70K events**
- **Mismatches between TMB and SP data are in BX assignment only, not in LCT frames**
  - **More detailed checks will continue at next beam test**

2004 CSC Beam Test Goals

- **Base goal:**
  - **Set up pre-production system and repeat prior tests using 25 ns structured beam**
    - **New CCB design**
- **Additional goals:**
  - **Test TMB2004 with RAT (new ALCT/RPC transition card)**
  - **Use fully functional XDAQ-based event builder and run control**
  - **Use fully functional Track-Finder system (self-triggering)**
  - **Use new DDU+DCC (FED) developed by OSU**
  - **Use new crate controller developed by OSU**
  - **Add an ME1/2 chamber in order to have 3-chamber test (for SP)**
  - **Swap/Add in ME1/1**
  - **Mount an endcap RPC on ME1/2, connect Link board to RAT, record RPC data in TMB**
  - **Add a small block of iron absorber between to validate OSCAR/ORCA simulation**

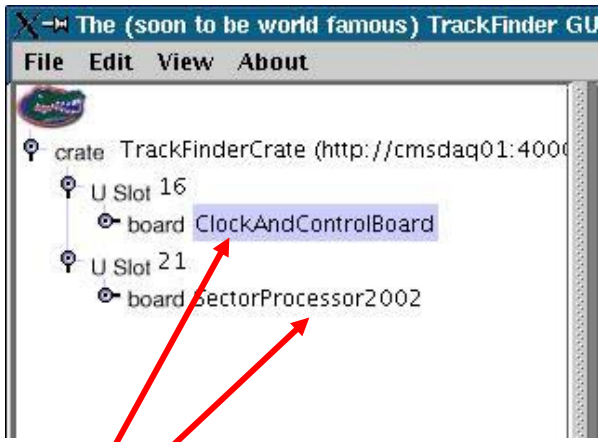
Production and Test Plans

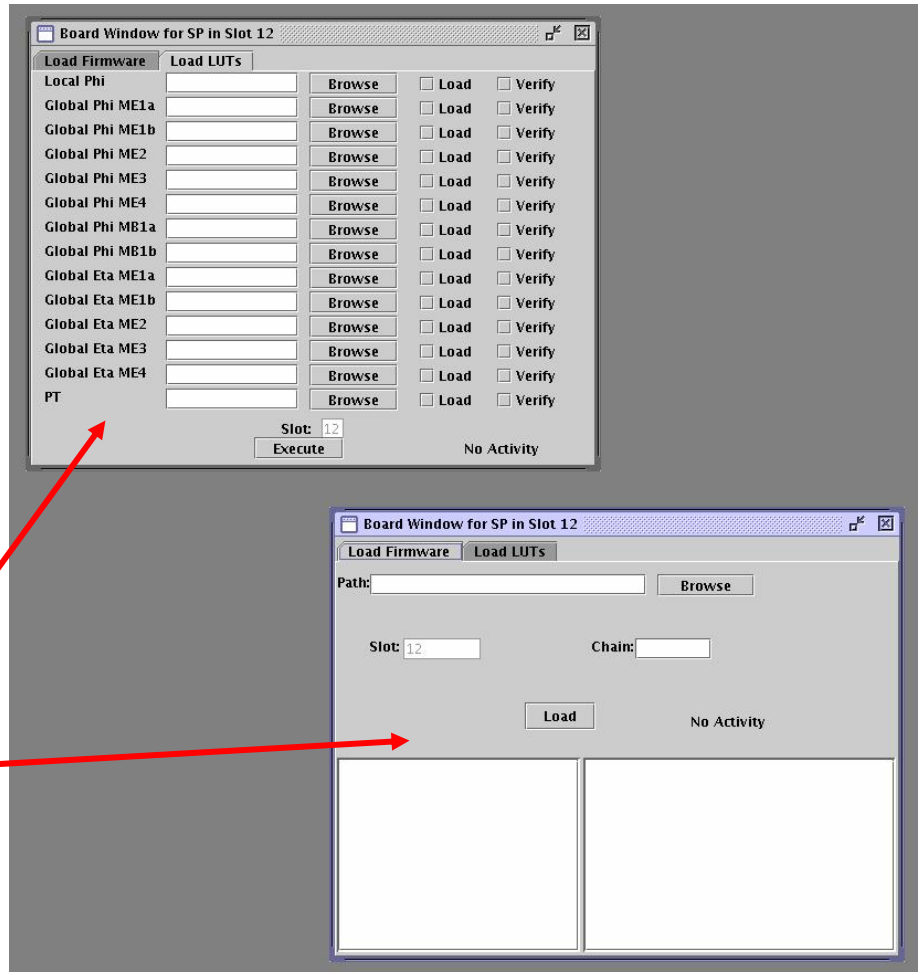
- **Will assemble 1 board first as pre-production prototype and test before launching full production (12 SR/SP + 3 spare)**
  - **To begin September 2004**
    - **May conflict with Sept/.Oct. 25 ns beam test run**
- **Each of the prototype tests (optical link PRBS tests, LUT tests, etc.) will become standard tests for the production modules**
  - **Therefore, we will have a suite of tests in our XDAQ-based software (hopefully with a JAVA interface)**
  - **Initial testing will be performed by a technician or student**
  - **Encountered problems will be addressed by our engineers**
- **Integration tests at CERN to be led by postdoc**

Known Fixes for Production Version

- Fix the DIN160 (VME connector) schematic component, initially designed with mislabeling of pin rows
- Fix mapping of five signals in the DT→SP interface
- Drive the TLK2501 reference clock from the on-board VCXO-based PLL clock (QPLL or QPLL substitute), and not from the Virtex II DCM clock (small mezzanine card)
- Make provision for the on-board QPLL reference clock to be either 40 MHz or 80 MHz backplane clock
- Visualize QPLL Lock condition with a front panel LED, and also access state in VME register
- Make a three-bit hardwired chip ID for each FPGA and make a six-bit hardwired card ID for each SP
  - On the CSR_CID VME command, each FPGA returns its ID and firmware revision date
- Several other technical fixes

Track-Finder GUI





Boards

Higher level SP02 command panel windows

Java interface to XDAQ-based software framework

CSC Track-Finder Milestones

CSC	Bckpl	Proto tested	Sep-02	Delay: Jun-04	Done
CSC	CCB	Proto tested	Sep-02	Done	New design tested Jun-04
CSC	SR/SP	Proto tested	Mar-03	Delay: Jun-04	~Done, wait for Jun-04 test
CSC	MPC	Proto tested	Mar-03	Delay: Jun-04	~Done, wait for Jun-04 test
CSC	SR/SP-MPC-CCB	Tested	Jun-03	Delay: Jun-04	~Done, wait for Jun-04 test
CSC	Sort	Proto done	Aug-03	Done	
CSC	Sort	Proto Tested	Nov-03	Delay: Jun-04	
CSC	Sort	Final Bd done	Mar-04	Delay: Oct-04	
CSC	Bckpl	Prod. done	Mar-04	Delay: Oct-04	
CSC	CCB	Prod. done	Mar-04	Delay: Oct-04	
CSC	Sort	Final Bd Test	Jun-04	Delay: Jan-05	
CSC	SR/SP	Prod. done	Jun-04	Delay: Jan-05	Delayed to Jan-05
CSC	MPC	Prod. done	Jun-04	Delay: Oct-04	
CSC	Bckpl	Prod. tested	Aug-04	Delay: Jan-05	
CSC	CCB	Prod. tested	Aug-04	Delay: Jan-05	
CSC	SR/SP	Prod. tested	Nov-04	Delay: Mar-05	Delayed to Mar-05

Personnel

- **Professors**
  - Darin Acosta (Florida), Robert Cousins (UCLA), Jay Hauser (UCLA), Paul Padley (Rice)
- **Postdocs**
  - Sang-Joon Lee (Rice), Holger Stoeck (Florida), Slava Valouev (UCLA), Martin Von der Mey (UCLA), Yangheng Zheng (UCLA)
- **Students**
  - Brian Mohr (UCLA), Jason Mumford (UCLA), Greg Pawloski (Rice), Bobby Scurlock (Florida)
    - Also Lindsey Gray and Nick Park (Florida undergraduates)
- **Engineers**
  - Alex Madorsky (Florida), Mike Matveev (Rice), Ted Nussbaum (Rice), Alex Tumanov (Rice - Software)
- **Collaborating engineers (PNPI)**
  - Victor Golovtsov, Lev Uvarov