Status of the CSC Trigger

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Outline

Status of the CSC Track-Finder

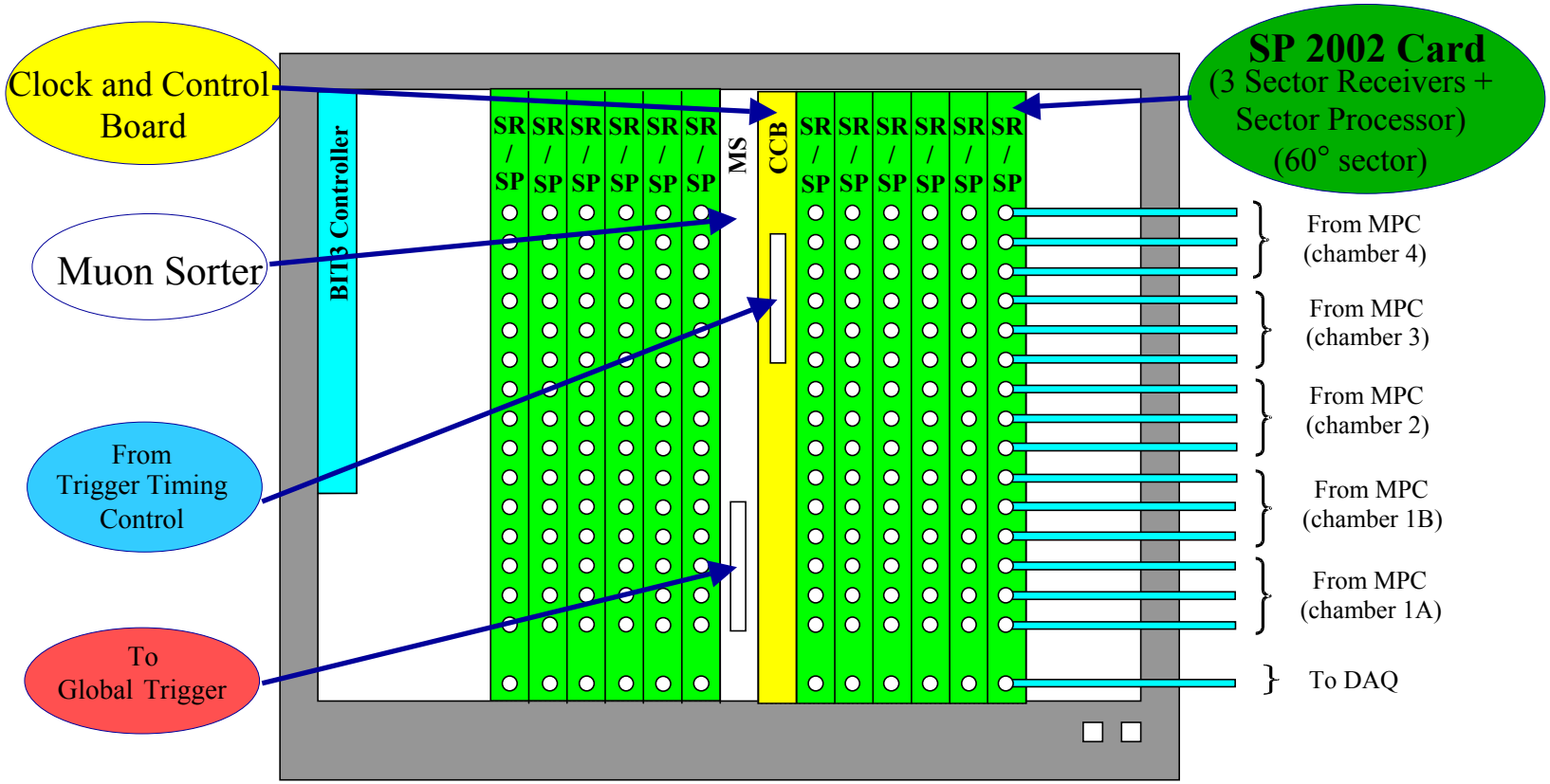
Status of the CSC Local Trigger

PHOS4 Experience

TTC Jitter Measurements

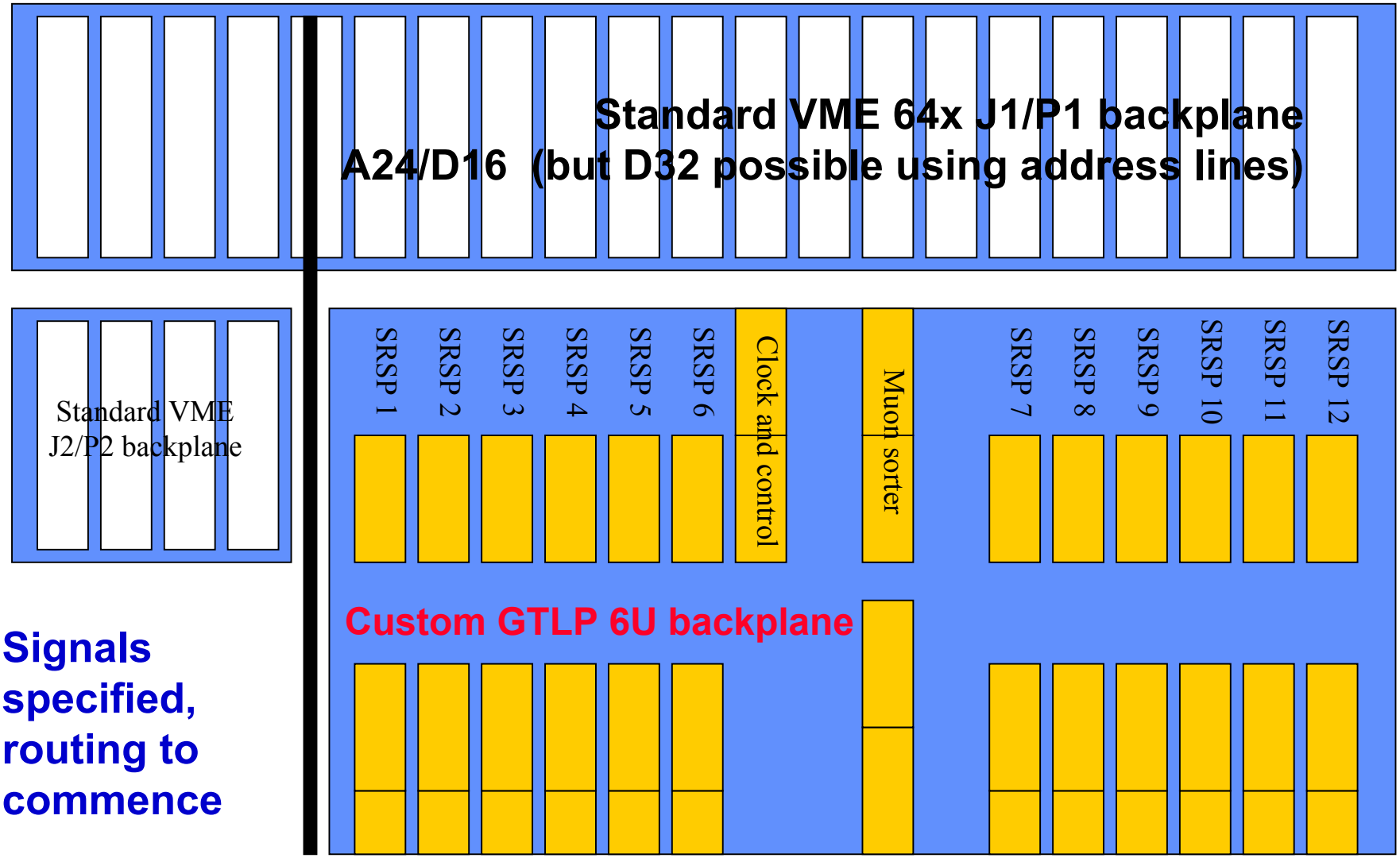
The CSC Track-Finder Crate

Track-Finder crate (1.6 Gbits/s optical links)



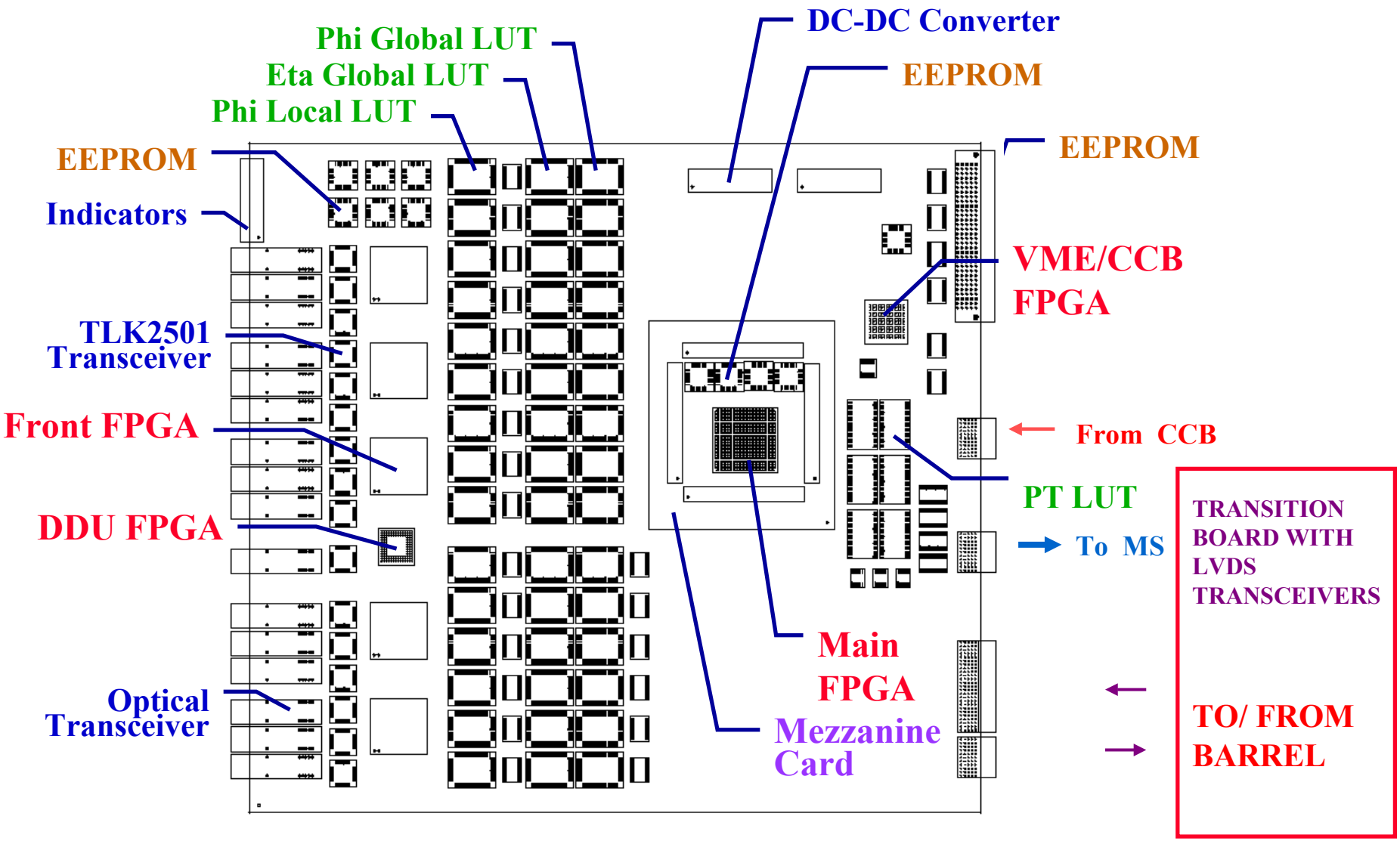
- **Power consumption : ~ 1000W per crate**
- **16 optical connections per SP**
- **Custom backplane for SP ↔ CCB and MS connections**

CSC Track Finder Backplane

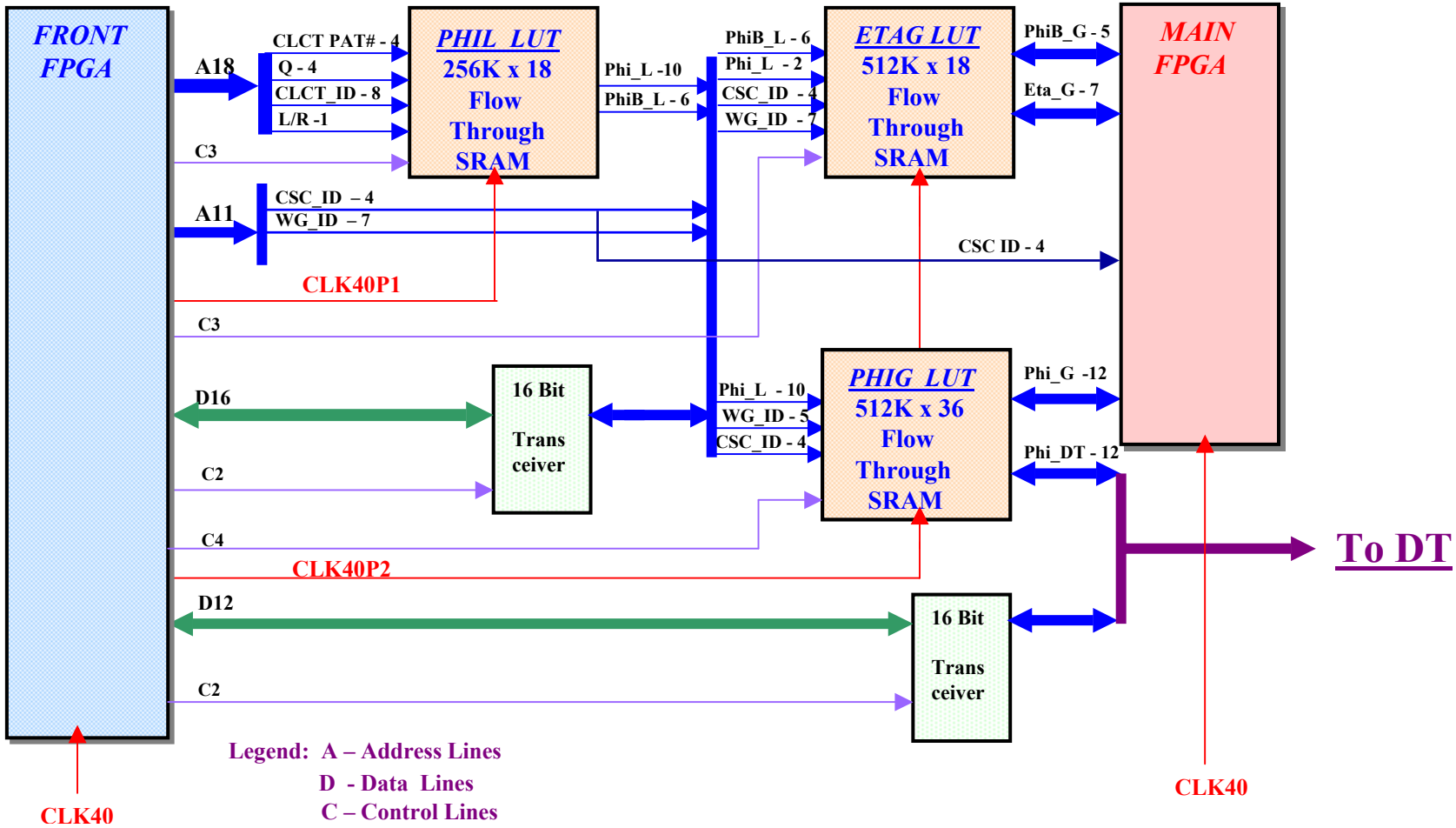


Signals specified, routing to commence

Sector Processor 2002 Board Layout

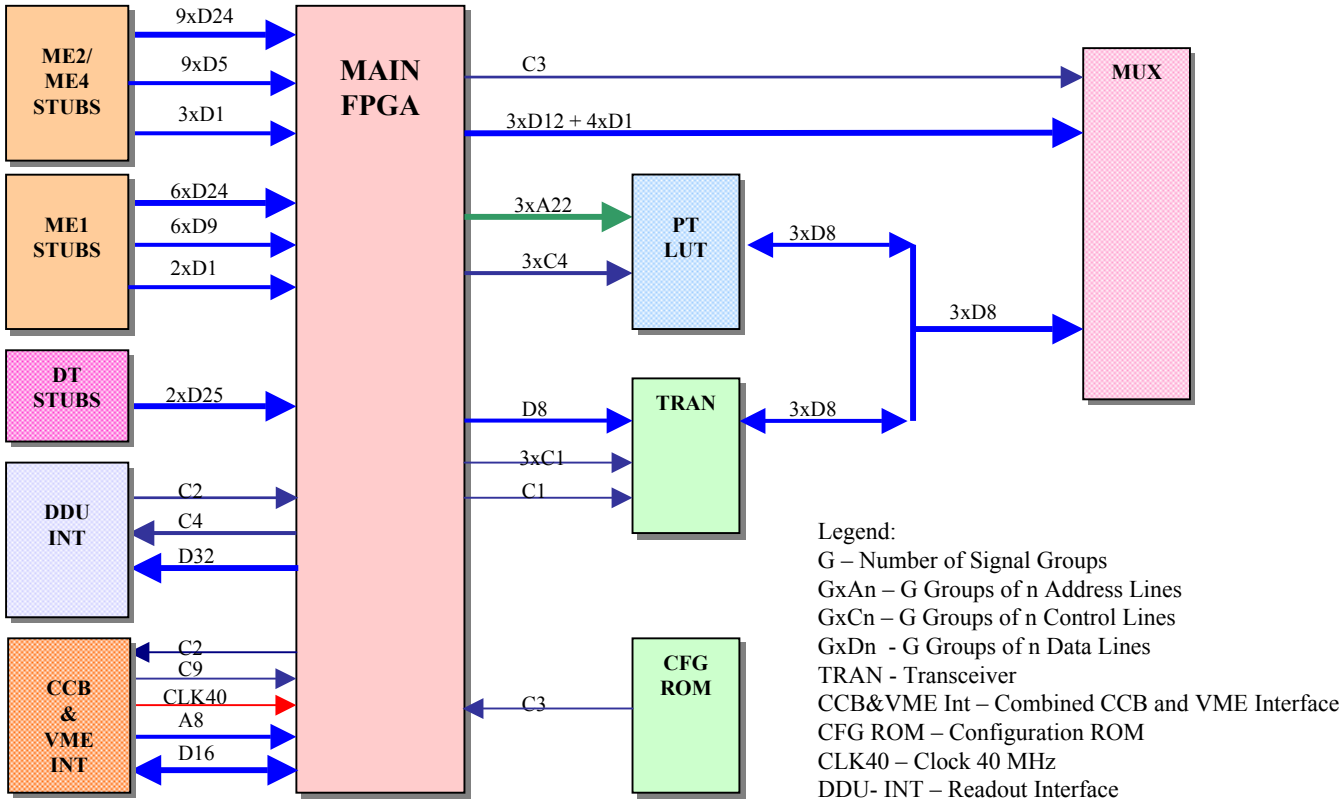


ME1 SR LUT Triad



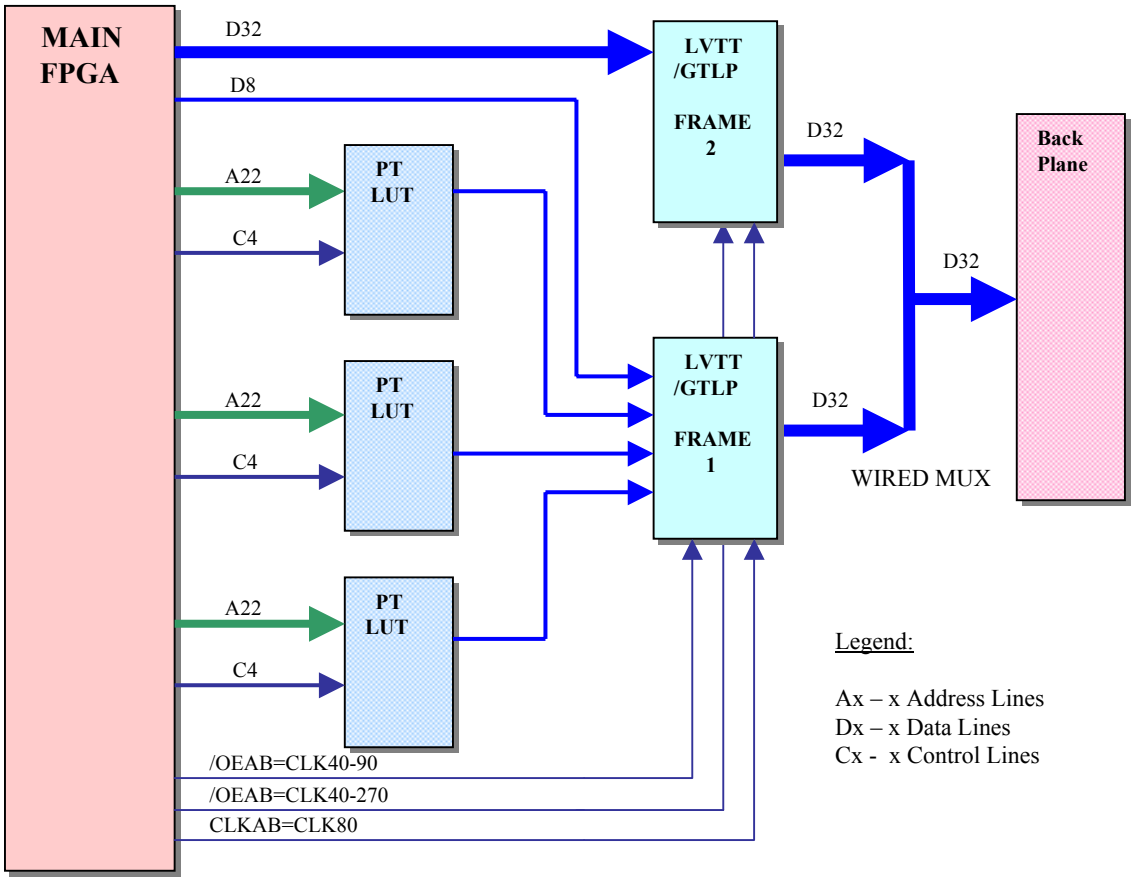
- 45 synchronous memories for conversion of 15 track segments
- >64 MB per board ⇒ Need high VME bandwidth, broadcast capability to identical chips, and crate broadcast capability to SPs

Main Sector Processor FPGA



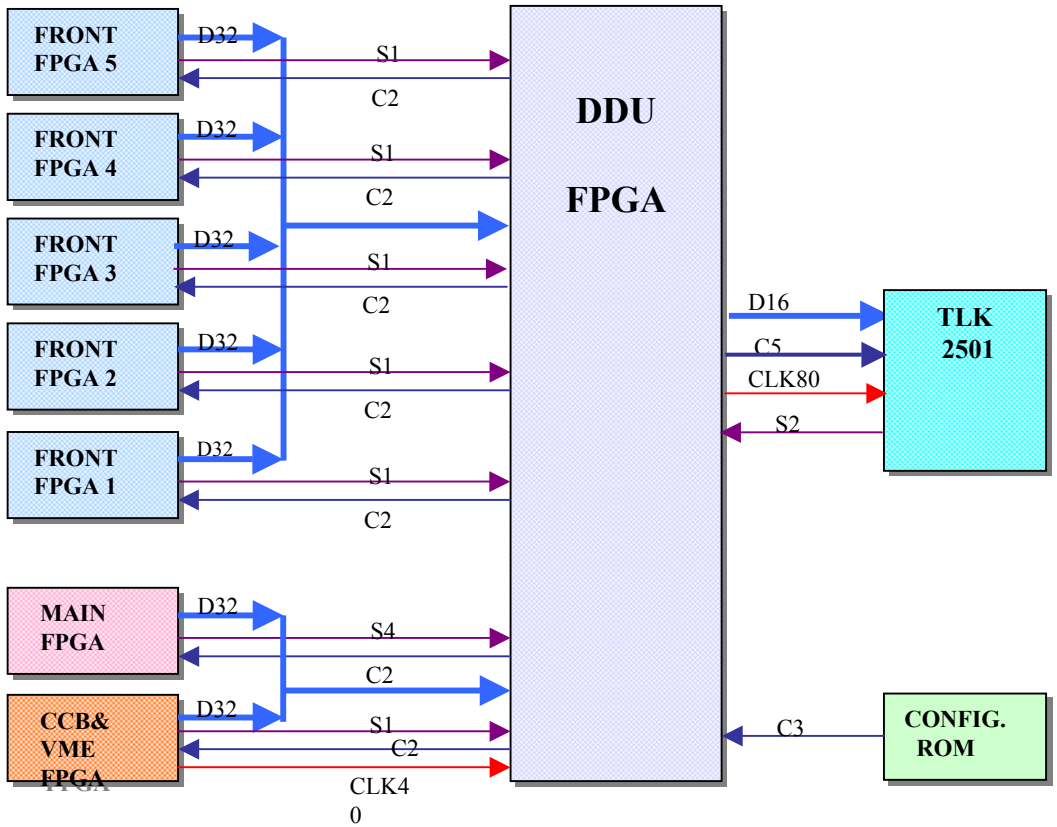
- Placed on mezzanine card
- Firmware written in "Verilog++" (see March TSWG talk) and implemented in ORCA as well
- Latency only 4 BX

PT LUT & MUX



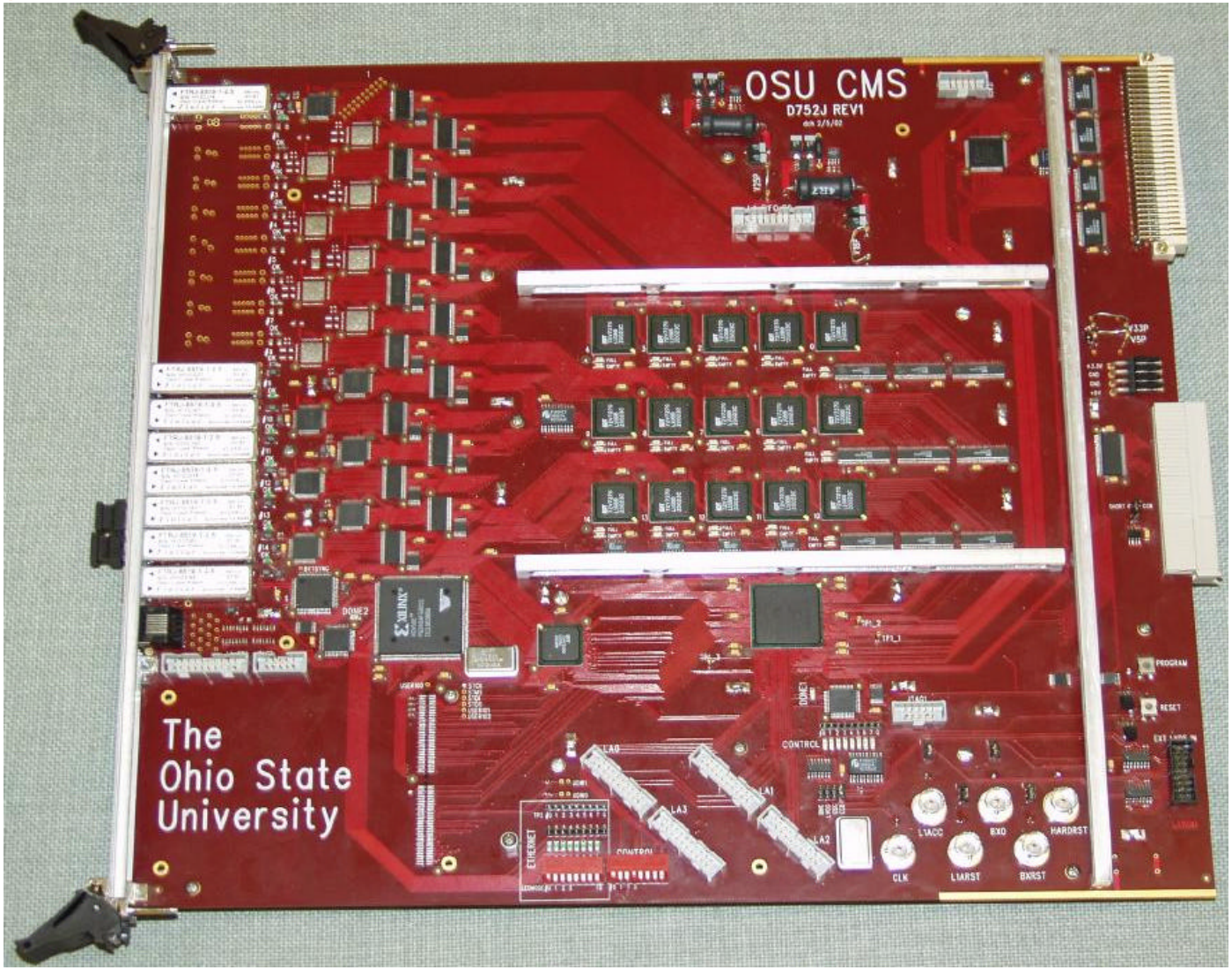
- Each Pt LUT is actually two 4M × 4 SRAMs
- Data multiplexed at 80 MHz onto GTLP backplane to Sorter

DDU FPGA



- DDU FPGA collects data from input and output buffers for transmission to a single CSC DDU (aka FED)
- Optical link is bi-directional (if needed) for asynchronous xfer
- CSC TF can exist in a separate partition from CSC chambers if we are allowed to send one SLINK connection to DAQ

Current DDU Prototype



SP2002 Interfaces

- VME Interface – updated for chip-level broadcasts (and crate broadcasts envisioned as well)
- CCB Interface – using same interface as CSC Local Trigger
- MPC Interface – updated (BC0 flag is sent through all TF cards now: MPC->SP02->MS, To/From DT)
  - ➔ MPC Data Validation - updated
- DDU Interface - updated (optional bi-directional)
- FM Interface – updated (RJ-45, 4 diff. signals)
  - ➔ Fast Monitoring Signals – updated (pinout)
- MS Interface – updated (BC0)
- DT Interface – updated (Synch/Calib -> BC0 ?)

Detailed accounting of all bits and protocols for these interfaces are specified in documents available from http://www.phys.ufl.edu/~acosta/cms/trigger.html

DT Interface

Data delivered from the Sector Receiver to the DT Track-Finder @ 40 MHz using LVDS.

Signal	Bits / stub	Bits / 3 stubs (ME1: 30°)	Bits / 6 stubs (ME1: 60°)	Description
ϕ	12	36	72	Azimuth coordinate
η	1	3	6	DT/CSC region flag
Quality	3	9	18	Derived from 4 bit Quality
BXN	–	2	4	2 LSB of BXN
Clock	–	1	2	Clock for data
BC0	–	1	2	Bunch Crossing 0
Total:	16	52	104	

Data delivered from the DT Track-Finder to the Sector Receiver @ 40 MHz using LVDS.

Signal	Bits / stub	Bits / 2 stubs (MB1: 60°)	Description
ϕ	12	24	Azimuth coordinate
ϕ_b	5	10	ϕ bend angle
Quality	3	6	
Muon Flag	1	2	2nd muon of previous BX
BXN	2	4	2 LSB of BXN
Clock	1	2	Clock for data
BC0	1	2	Bunch Crossing 0
Total:	25	50	

CMS Note on DT/CSC interface ~ready to be released

SP2002 FPGA Choices

Front FPGAs (3 Muons per FPGA, 5 FPGAs total)

- ➔ Interfaces require at least 365 I/Os
  - Choice: XC2V1000-?FF896C with 432 user I/Os
- ➔ May be socketed (BGA soldered to high-density pin array)

Main FPGA

- ➔ Interfaces require at least 716 I/Os
  - Choice: XC2V4000-?FF1152C with 824 user I/Os
- ➔ Placed on mezzanine board

VME & CCB FPGA

- ➔ Interfaces require at least 150 I/Os
  - Choice: XC2V250-?FG456C with 200 user I/Os

DDU FPGA

- ➔ Interfaces require at least 110 I/Os
  - Choice: XC2V250-?FG256C with 172 user I/Os

Additionally, there are 51 SRAM chips

- ➔ Board will be dense! (Merger of 4 boards)

CSC TF Milestones for 2002

CSC Track-Finder:

- Dec. 2001: Specify backplane connections ✓
- Apr. 2002: Conceptual design complete ✓
  - Reviewed by US trigger group during 2 day workshop in March
- May 2002: Schematics complete
- Sep. 2002: Layout complete
- Nov. 2002: Finish fabrication of pre-production prototypes
  - 2 month delay from original Sep. 2002 milestone

CSC Prototype Test Schedule

- MPC logic tests: 10/1/02 – 12/31/02
- SP logic tests: 12/1/02 – 4/30/03
- MPC → TMB: 7/1/02 – 12/31/02
- MPC → SP: 3/1/03 – 4/30/03
- FAST site chain test: 5/1/03 – 6/30/03
  - Cosmic ray test with chambers and full chain of prototypes
- Structured beam test: 7/1/03 – 9/30/03 ?
  - Chain test with detectors in beam line, sometime in '03
- DT TF → CSC TF: 7/1/03 – 9/30/03 ?
  - Crate test sometime before or after beam test
  - Transition boards need to be designed

Note: we still have a lot of software to design and write to perform these system tests. Must interface previous trigger test code to FAST site test code, XDAQ, etc. Fortunately, we have several students and postdocs identified to help in this area. But we could use some guidance and examples on how to get started.

CSC Production and Testing

Currently scheduled to complete CSC trigger production (CCB, MPC, SP) by Sep. 2004

Slice test scheduled for ~Oct. 2004

- ➔ **If production not yet complete, will use current prototypes**

Installation to begin Nov. 2004

Start integration with DAQ Mar. 2005

Special Triggers

After commissioning, we'll still want to monitor trigger efficiencies and alignment during data taking

Some ideas:

- **Prescaled low p_T thresholds**
  - **Useful to monitor efficiency, alignment, etc.**
- **Prescaled loose 2-station triggers or even single station triggers**
  - **Useful to monitor local trigger efficiency (BTI and LCT) since this is dependant on analog chamber performance (i.e. can't just run digital simulation)**
- **Accelerator muon triggers**
  - **CSC Track-Finder (and GMT) will have the ability to trigger on muons traveling parallel to the beam axis during normal running**
  - **Should be useful for in-situ alignment studies of chambers**

CSC Trigger Primitive Electronics Status

- **Wire boards: ALCT (Anode Local Charged Track)**
- **Strip/coincidence/readout boards: TMB (Trigger MotherBoard)**

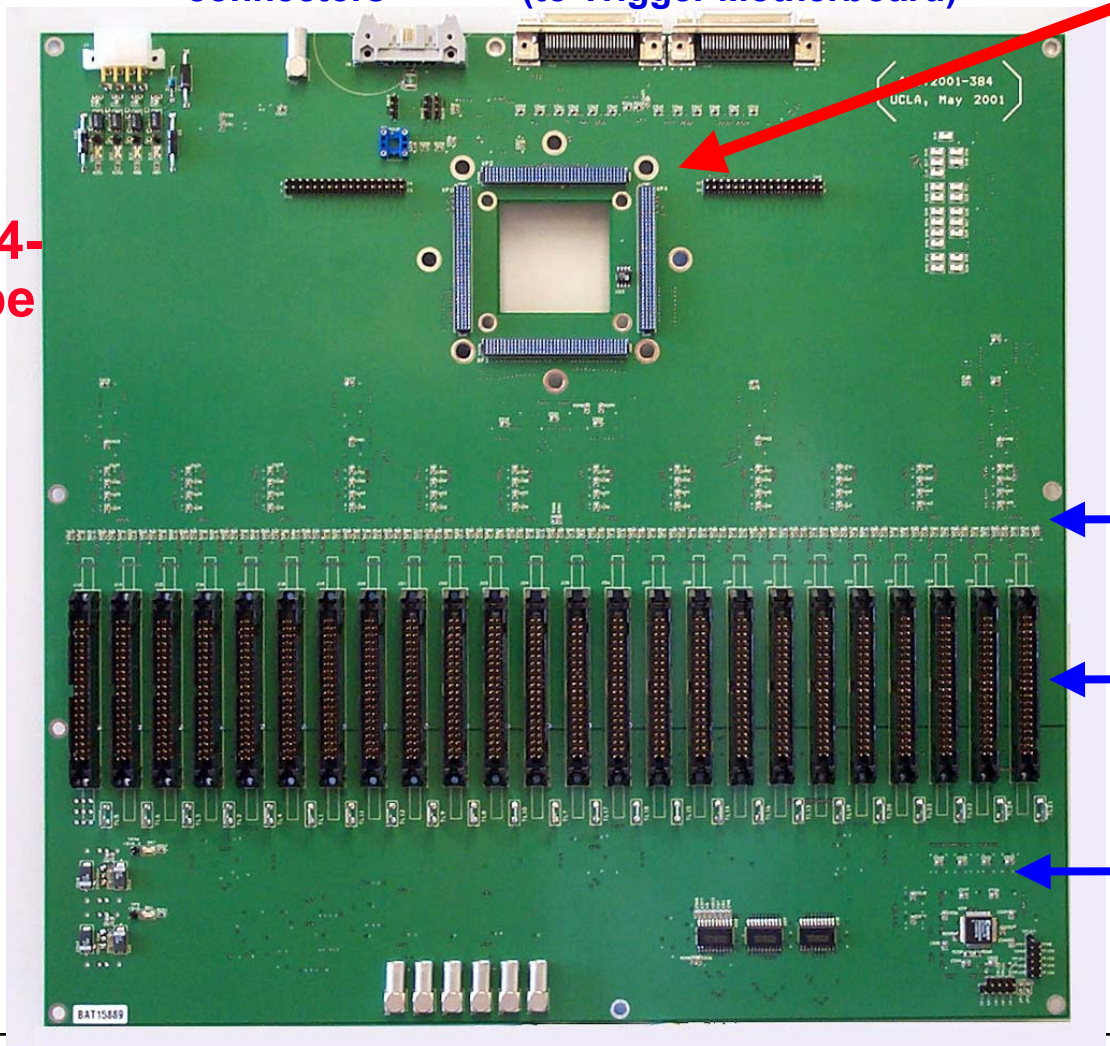
ALCT2001 Boards

Power, computer connectors

80 MHz SCSI outputs (to Trigger Motherboard)

Xilinx mezzanine card

Main board for 384-ch type



Delay/ buffer ASICs, 2:1 bus multiplexors (other side)

Input signal connectors

Analog section: test pulse generator, AFEB power, ADCs, DACs (other side)

ALCT Functions

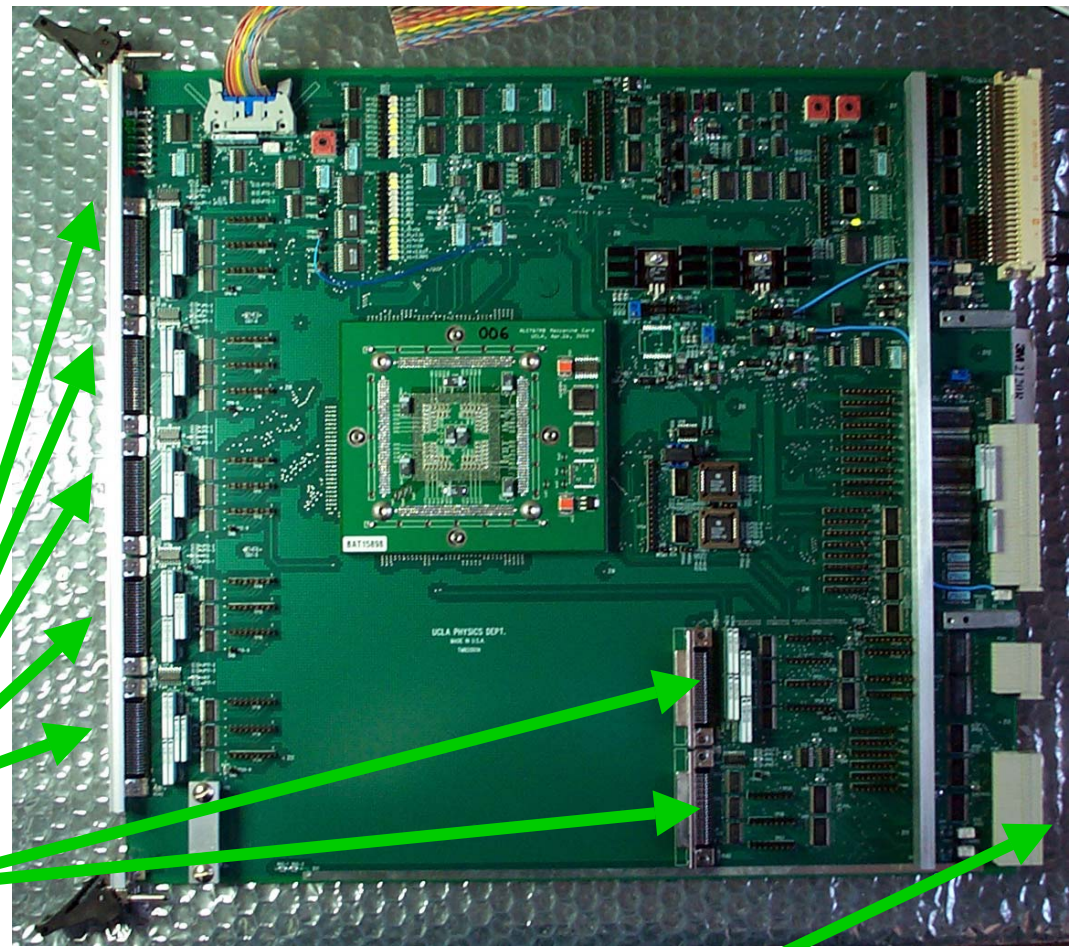
1. Inputs discriminated signals from AFEB front-end boards, provides AFEB support:
   - Distributes power, shut-down, test pulse signals.
   - Sets and reads back discriminator thresholds.
   - Monitors board currents, voltages, and temperature.
2. Delay/translator ASIC on input does time alignment with bunch crossings.
3. Searches for muon patterns in anode signals. If found, sends information to trigger motherboard.
4. Records input and output signals at 40 MHz in case of level 1 trigger.

ALCT Status

- Board has been thoroughly debugged
- Have extensive suite of testing software and an external test fixture.
- 3 versions:
  - ALCT2001-384 is in pre-production (30 boards, 40 mezzanine cards)
  - ALCT2001-672 have 6 prototype boards being assembled
  - ALCT2001-288 have 6 bare prototype boards, assembly soon.
- Now integrating with software for chamber tests at U Florida and UCLA

TMB - Trigger MotherBoard

- TMB2001 prototypes for use at FAST sites and for system tests
- Produces cathode patterns from comparator outputs
- Correlates cathode and anode (from ALCT) patterns
- Sends chamber-level trigger decision to MPC
- Raw hits data "spooled" to DMB
- Interfaces to "everything"
  - CFEBs
  - DMB
  - CCB
  - ALCT
  - MPC
  - VME
  - RPC (later)
  - JTAG



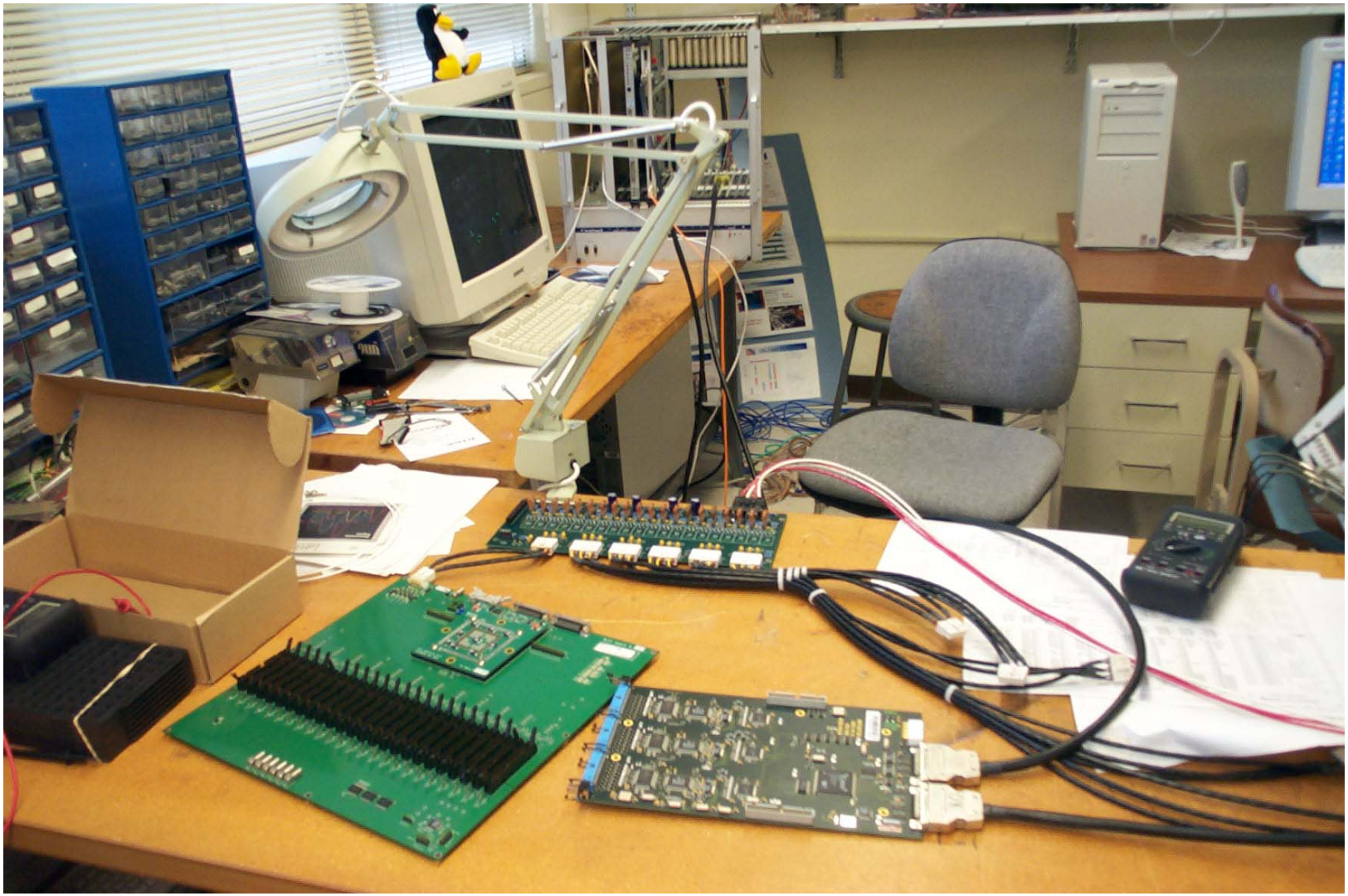
TMB Hardware Status

- 17 TMB boards were produced (all FAST sites plus development uses)
- Bad job done by assembly company:
  - Connectors soldered in crooked, boards could not be inserted
  - Connectors were removed and reinstalled properly by UCLA
  - Misc. errors (about seven per board)
- 2 boards have been fully corrected and debugged, including CFEB, ALCT, DMB, DDU, CCB interfaces
- 1 TMB was shipped to OSU for CFEB/DMB/DDU tests
- The other TMB is for continued firmware development at UCLA

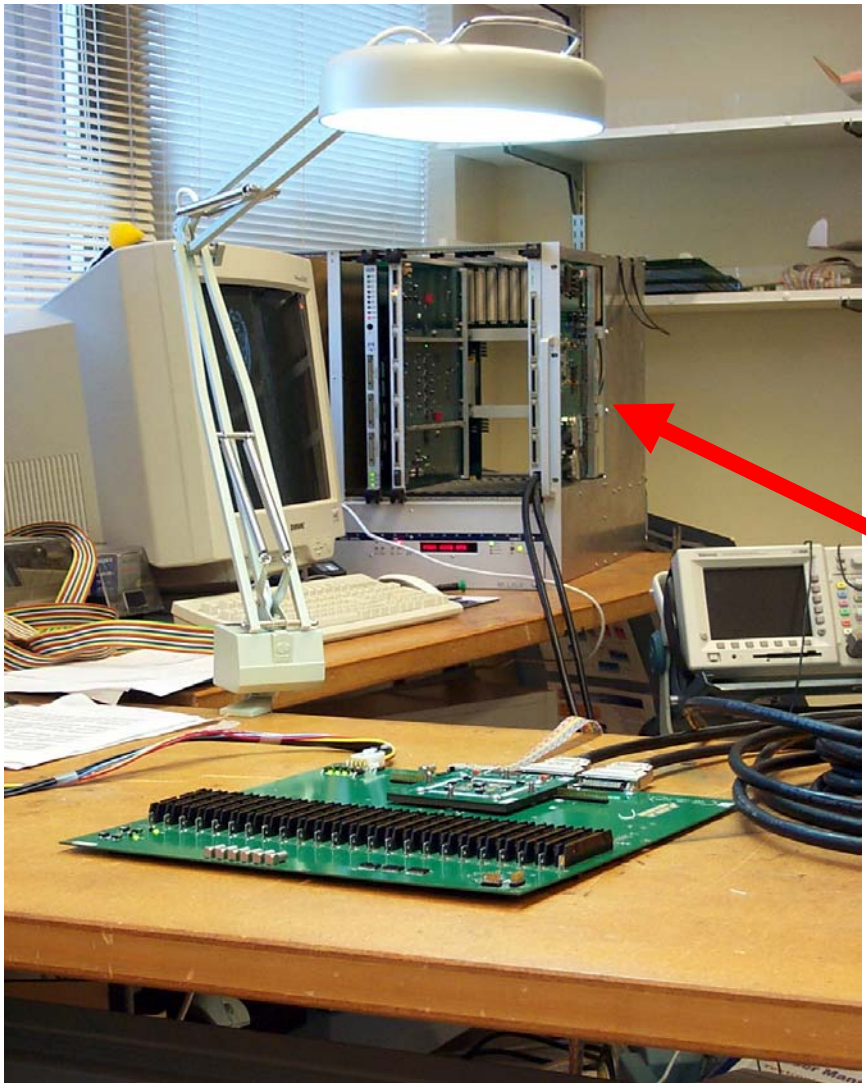
PHOS4 Problem

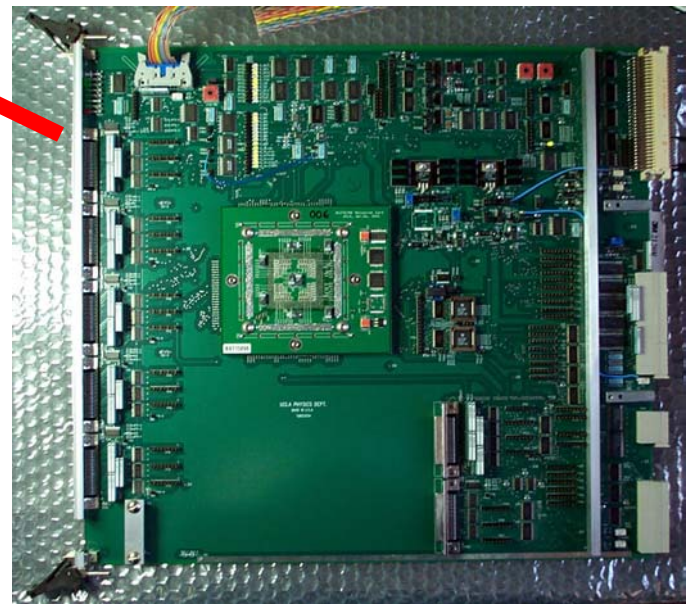
- **PHOS4 delay chips are convenient, so were used in TMB and CCB (Clock&Control Board)**
- **But…**
  - **They can only be reset once. This can be a big problem.**
  - **We have had a lot of difficulty getting them initialized properly (months of work). Sometimes power cycling a crate is the only solution (ugh).**
  - **They produce an asymmetric output clock, especially if one PHOS4 used in series with another.**
  - **Delay = 0 setting gives about 3 ns variance between chips, not very tight.**
  - **PHOS4 power-on sequence work-around allows board to operate**
    - Wait 1 second, send a reset, wait 1 second, program via I2C bus
    - (Previously, PHOS4 chips did not power up in clocking state (dead board!), 5ns delay sometimes became 10ns etc.)
    - Still have very asymmetric (58/42%) output clock

TMB-CFEB-LVDB Test



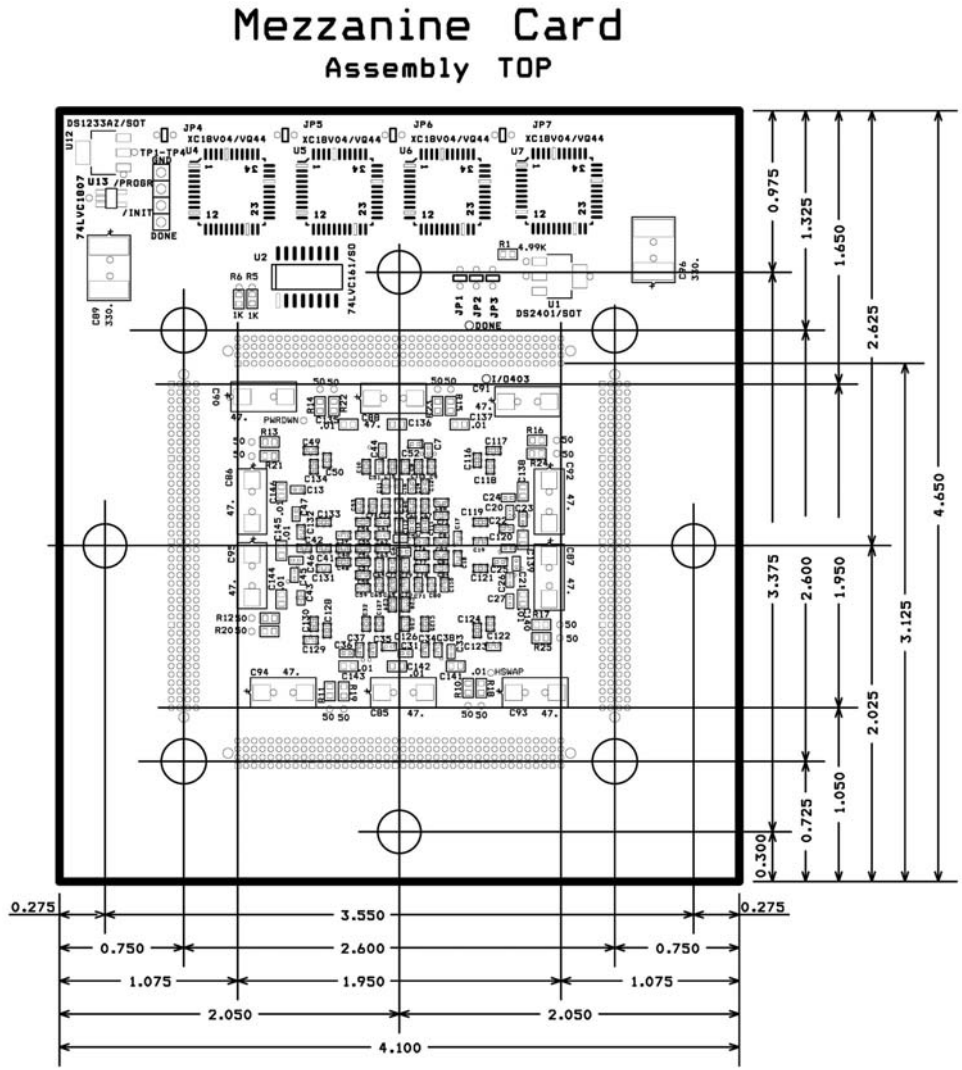
ALCT-TMB Testing



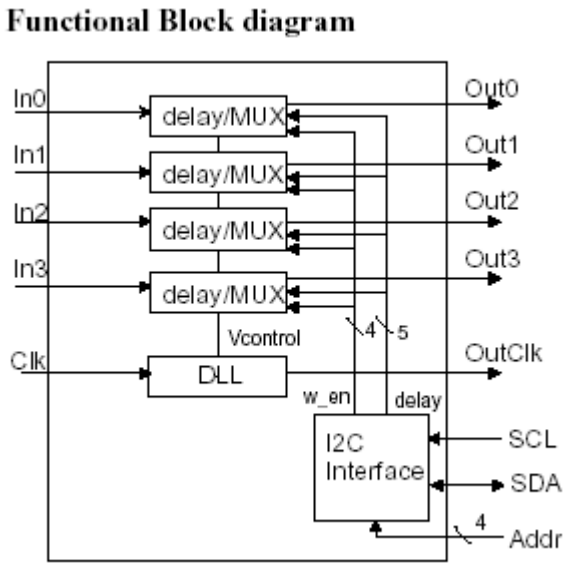


Virtex-II For Future Use in TMB

- Allows faster performance and some clocking and I/O advantages
- Initial layout done
- Designed for “medium” (896 ball) FPGAs for TMB (or ALCT)
  - XC2V1000, 1500, 2000 chips
- Ball locations compatible with “large” (1152 ball) FPGAs for e.g. Sector Processor
  - XC2V3000, 4000, 6000, 8000, 10000 chips



PHOS4 features



- CERN designed 4-channel delay ASIC with 1 ns delay precision
- Radiation Hard
- Programmable (write-only) over I2C bus

Issues with PHOS4

- The PHOS4 is intended for use with non-interruptable clock source (since the chip utilized DLL circuitry)
- If clock is interrupted, then the behavior is unpredictable
  - wrong delays
  - “dead-looking” channels
  - no direct way to identify what is wrong with the chip
  - **Only power cycling can help**

- Lack of dedicated “reset” pin
- Delay settings are not readable back via I2C bus

- We have suggested that the chip be redesigned

Clock Interruptions?

- In our opinion, the clock should never be interrupted (except on power cycling)
- TTC tree is designed so clock won't be interrupted
- A question to CMS/LHC is "How often can we expect the clock to be interrupted?"

Interruptions

- What to do if interruptions are a problem?
  - PHOS4 can be simply removed from the CCB boards (all 4 socketed) and clocks wired directly to LVDS transmitters
    - **no individual slot-to-slot and module-to-module clock adjustments**
    - **no extra effort to program I2C**
    - **same PCB layout, minimal on-board changes**

Another Question

- All clock lines in the custom peripheral backplane are point-to-point LVDS of the same length.
- **Do we really need to adjust the 40Mhz clock from slot to slot and from module to module?**

Another Alternative

- **If fine clock adjustments on the backplane are still needed**
  - PHOS4 can be replaced with another device, for example, 3D7408 proposed by OSU
    - 1-channel commercial CMOS programmable delay chip
    - This device has 45/55 output duty cycle instead of 50/50 at 40Mhz (tested at Rice). Is it acceptable for DMB/TMB/ALCT?
    - layout changes on a CCB board required
    - Radiation tolerance?

TTC Issues

Trouble Reported

- At the last CMS week (and continuing) reports from many groups that they can not drive optical links with a TTC derived clock
- (Sorry, but nobody [but us] is documenting what they are doing, so I can't point you to anything written on the topic)
- Our report is at

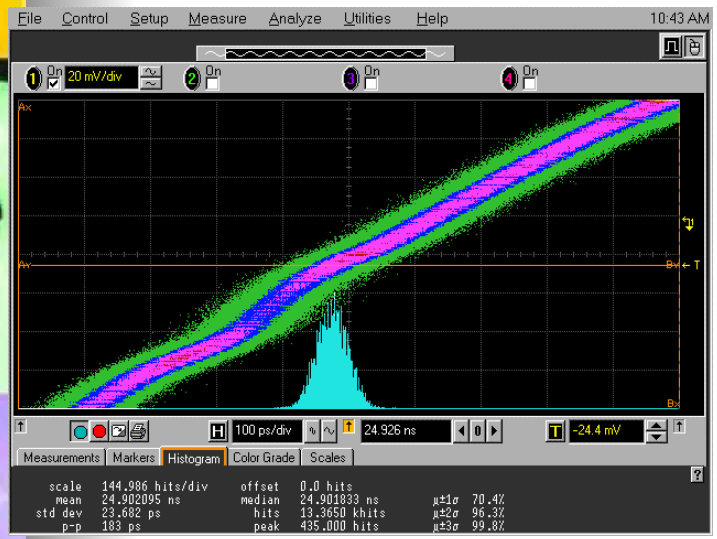
  http://bonner-ntserver.rice.edu/cms/jitter.pdf

The Issue

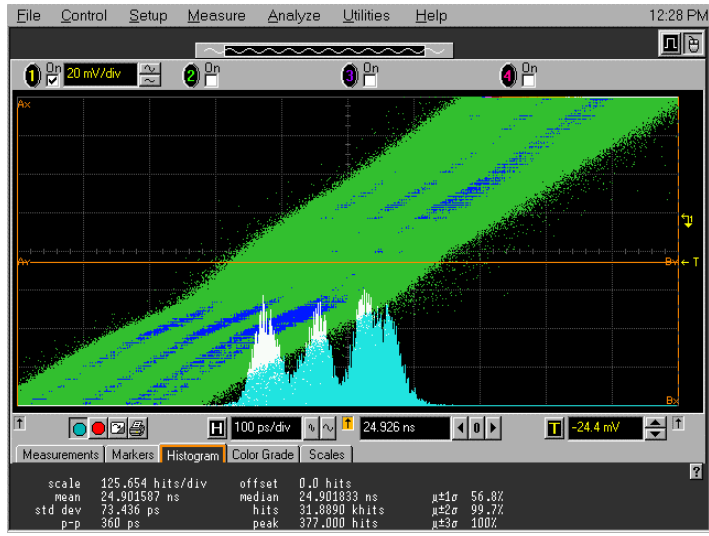
- TTC group has specified that they will deliver clock good to 50ps rms.
- Groups using CERN GOL (not us) claim TTCrx can't drive their links
- Reports of jitter measurements ~500ps
- At last CMS week microelectronics group agreed to improve TTCrx
  - (time scale?)

Our Measurement

Mezzanine Card	ECP680-1102-630C		ECP 680-1102-610B
TTCrx ASIC operating voltage	+5.0V	+3.3V	+5.0V
Clock40Des1 jitter, ps (no BC, no L1A)	153	170	330
Clock40Des1 jitter, ps (BC commands + L1A)	183	215	360

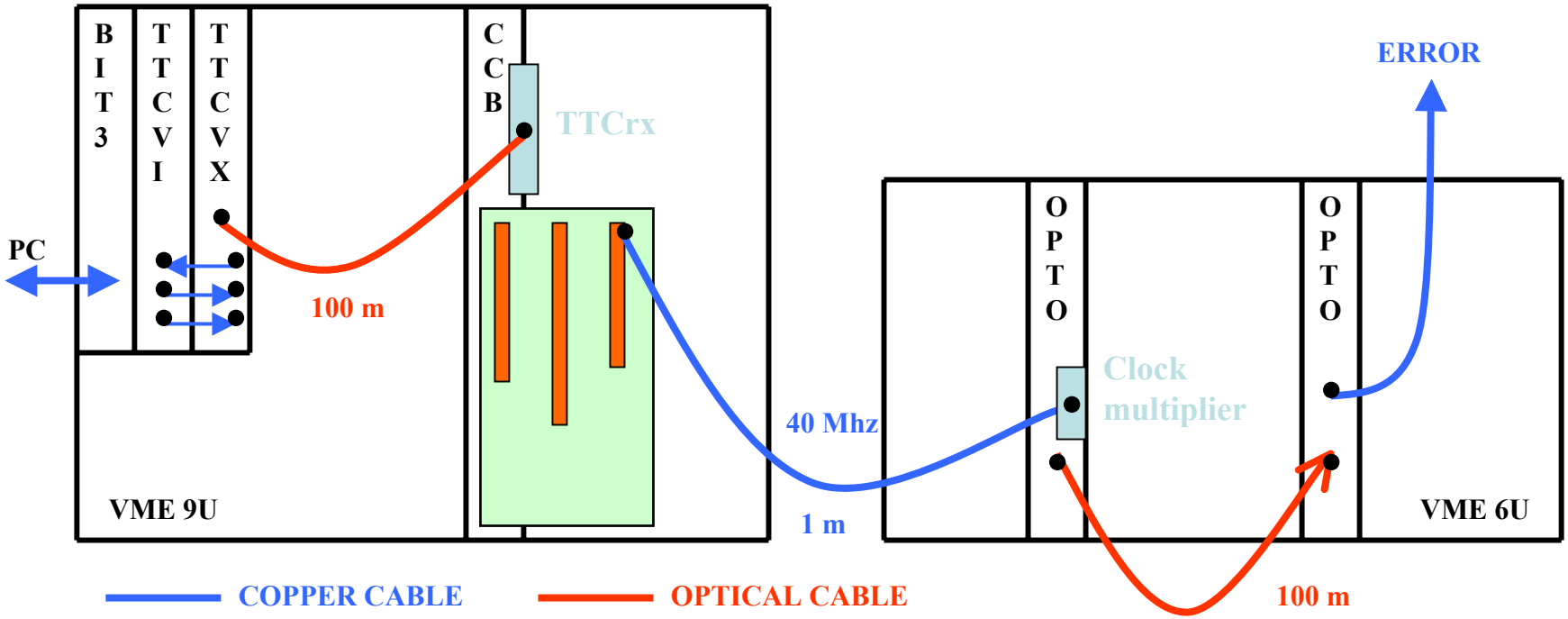


New TTCrx



Old TTCrx

Our Test



- **OLD AND NEW TTCrx BOARDS WERE TESTED WITH 40.00 Mhz CLOCK SOURCE FROM TTCvx MODULE**
- **40.00 Mhz CLOCK WAS MULTIPLIED BY 2 BY AV9170 CHIP**
- **NO ERRORS OBSERVED IN PRBS TEST FROM ONE OPTOBOARD TO ANOTHER AT 80.00 Mhz (BER < 10^{-13} c^{-1})**

Our Result

- Clock jitter is lower for the newest TTCrx ASIC (Version 3.1, 12/01)
- Jitter increases if broadcast commands and L1A are transmitted from the TTC system
- Jitter distribution for ASIC Ver.3.1 looks “normal” (unlike previous version)
- Clock jitter is lower if the new ASIC is powered from +5V
- Jitter introduced by any of two TTCrx ASICs and other components in the clock distribution circuitry at our testing setup is tolerable for TLK2501 transceivers operating at 80.00 Mhz using prototype MPC-SR link