

# CSC Trigger Developments

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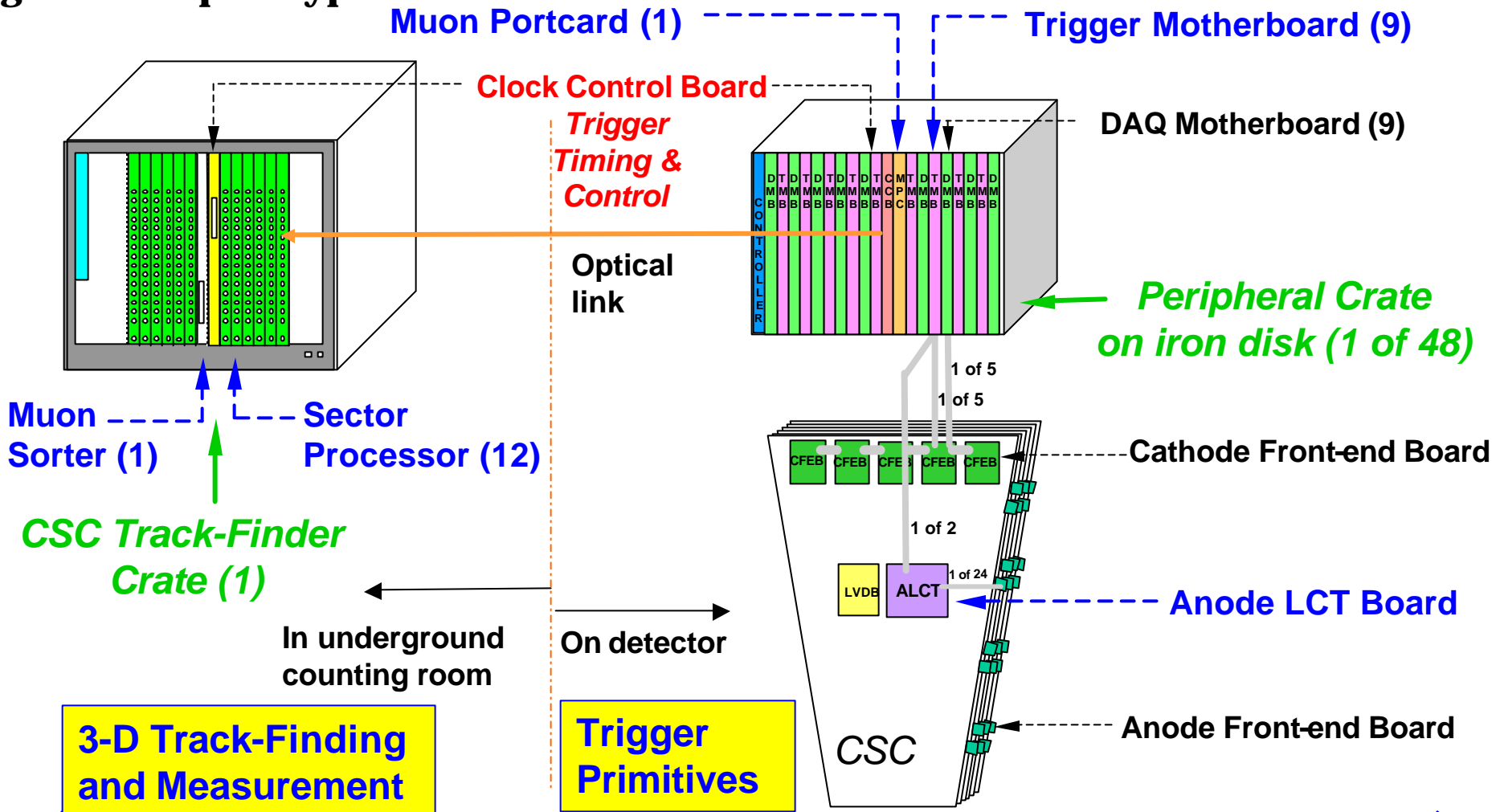
- **Prototype Status:**
  - **Muon Port Card**
  - **Sector Processor**
  - **Muon Sorter**
- **Study on the recovery of TeV muons by an improved  $P_T$  assignment algorithm**



# CSC Muon Trigger Scheme

**TriDAS part: Second generation prototypes**

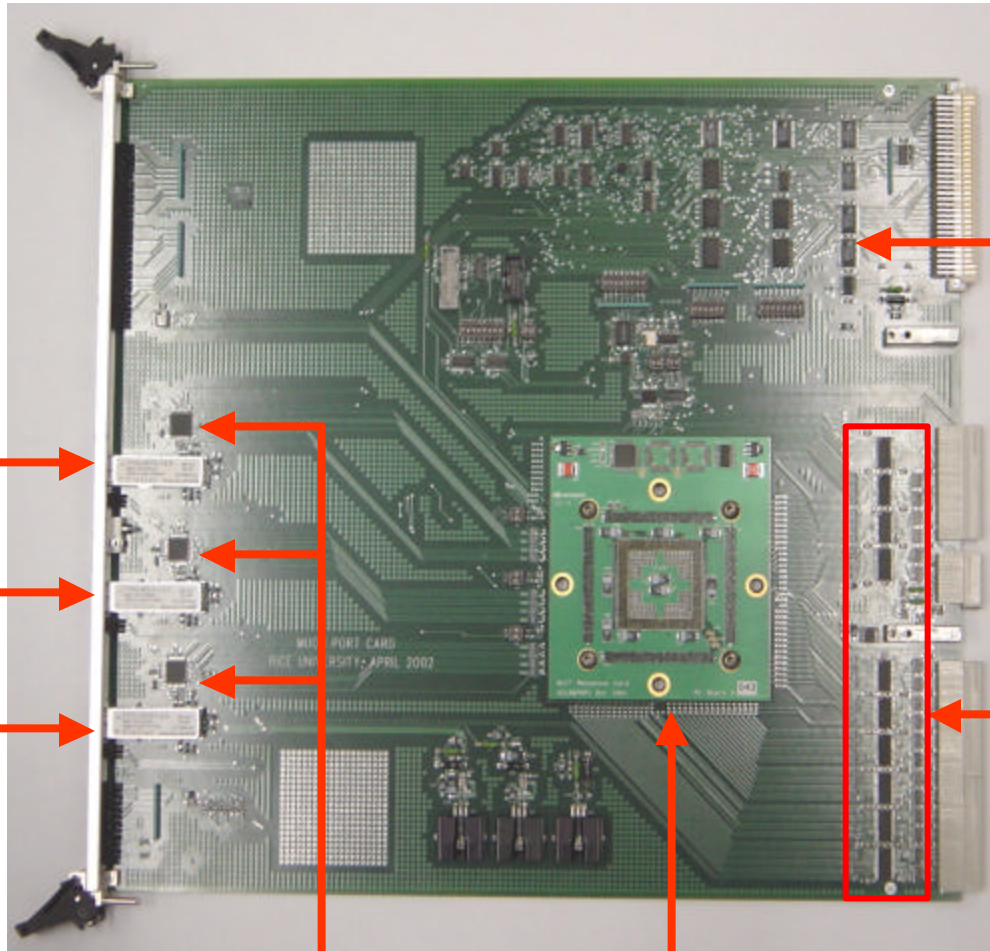
**EMU part: mostly in production**





# Muon Port Card (2<sup>nd</sup> Prototype)

Rice



VME Interface (glue logic)

GTLP Receivers

Optomodules

TLK2501 serializers

Mezzanine card





# MPC Design Status

Rice

- 3 boards have been fabricated and assembled in summer
- Have 6 UCLA mezzanine cards in hand
- Tested MPC standalone (sorter logic) and with one and two Trigger Motherboards and full-size custom backplane
  - various patterns sent from TMB to MPC at 80Mhz
  - feedback “winner” bits from MPC to TMB
  - periodic FPGA reconfiguration from EPROMs (both MPC and TMB) upon “hard reset”
  - measured the board latency

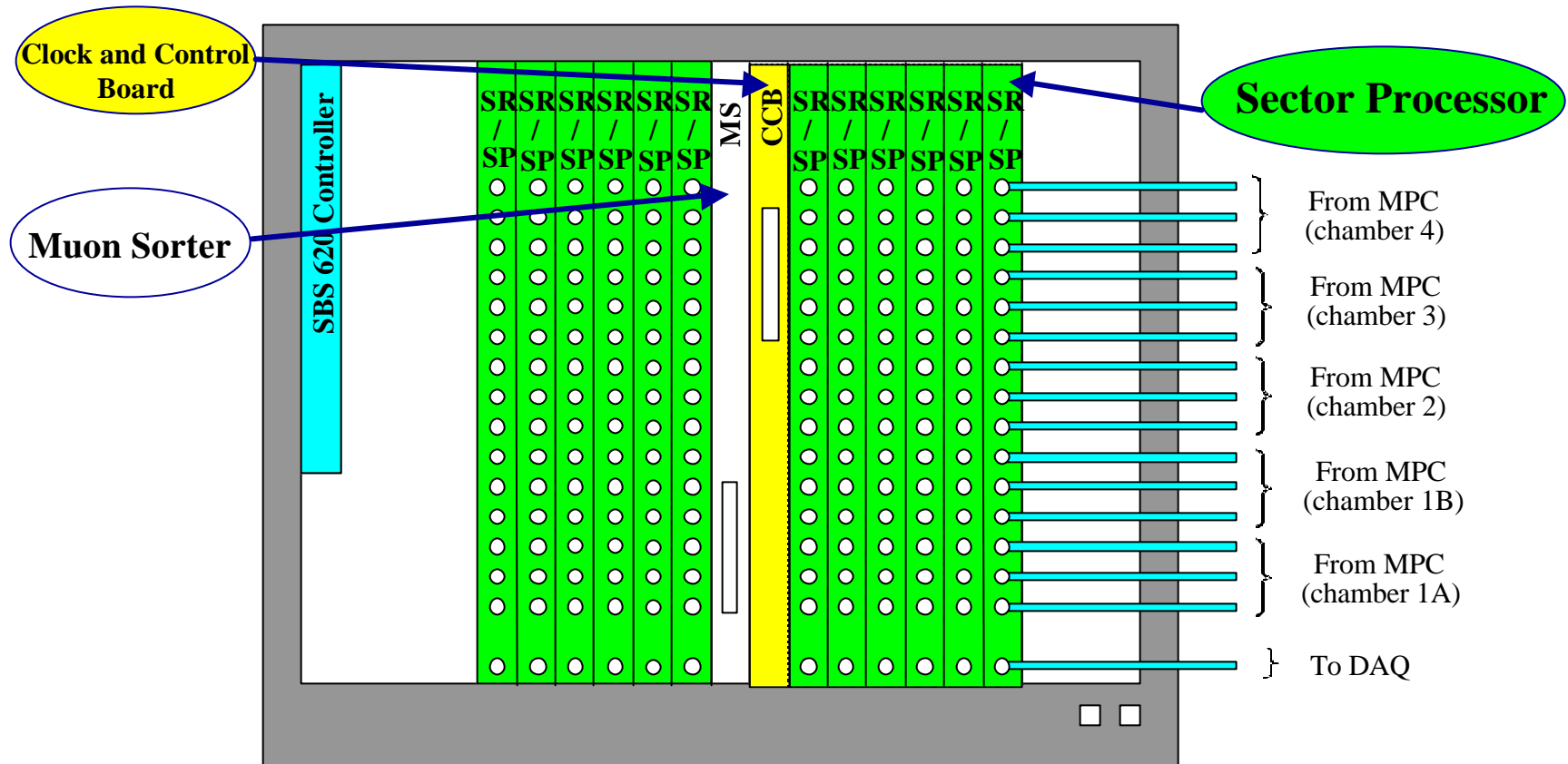
**Waiting to test with Sector Receiver/Processor**





# CSC Track-Finder Crate

## Second generation prototypes



- Single Track-Finder Crate Design with 1.6 Gbit/s optical links





# Next Generation Sector Processor

**New SR links  
and LUTs**

**Phi Global LUT**  
**Eta Global LUT**  
**Phi Local LUT**

**DC-DC Converter**

**EEPROM**

**VME/CCB  
FPGA**

**Main FPGA  
XC2V4000**

**Fits all of previous  
SP board logic!**

**Stiffener**

**Indicators**

**FM RJ45**

**TLK2501  
Transceiver**

**Front FPGA**

**DDU FPGA**

**Optical  
Transceivers  
(16)**

**From CCB**

**To MS**

**PT LUT**

**MB1-to-SP**

**ME1-to-DT**

**Mezzanine  
Card**

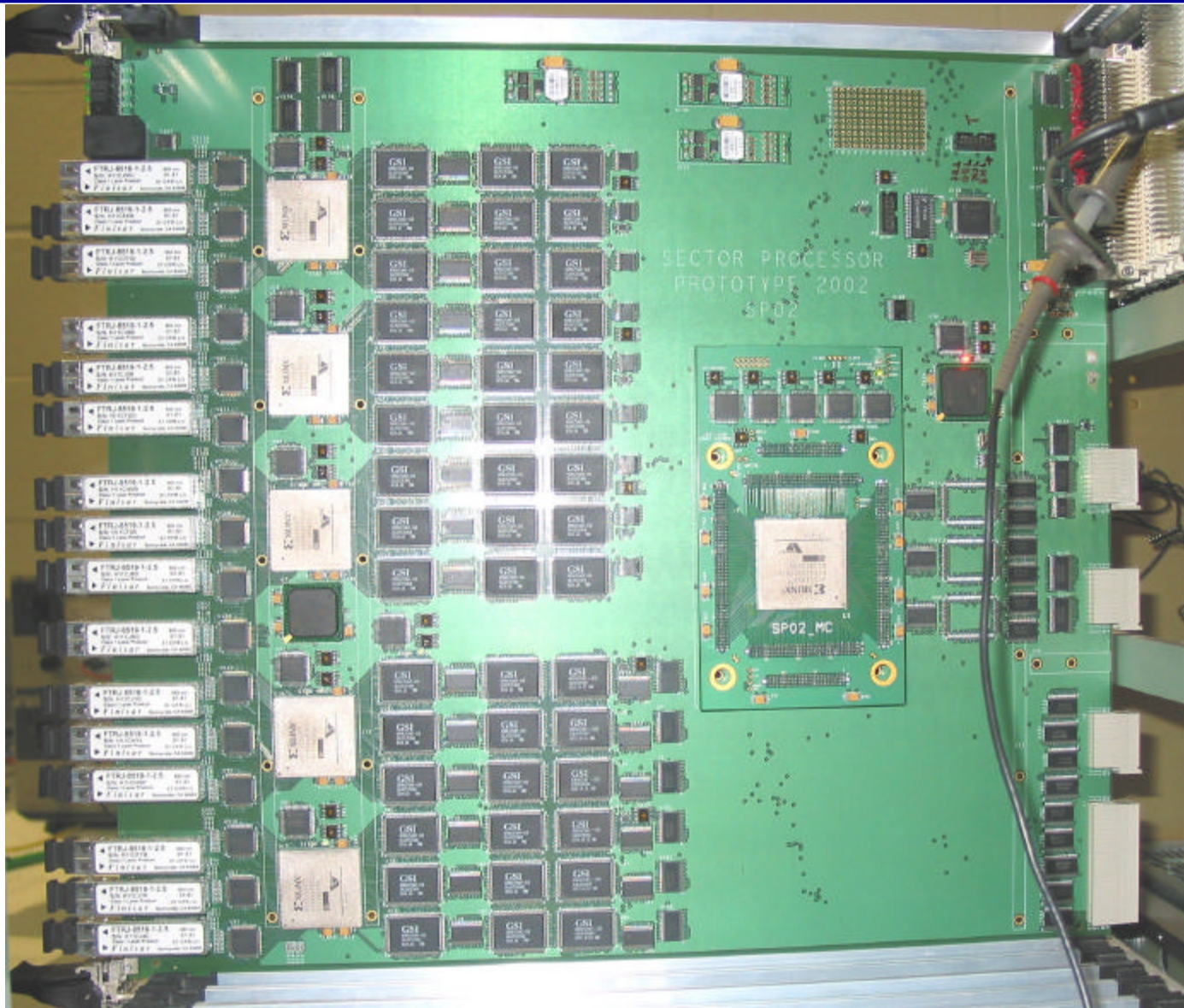
**SRAM**







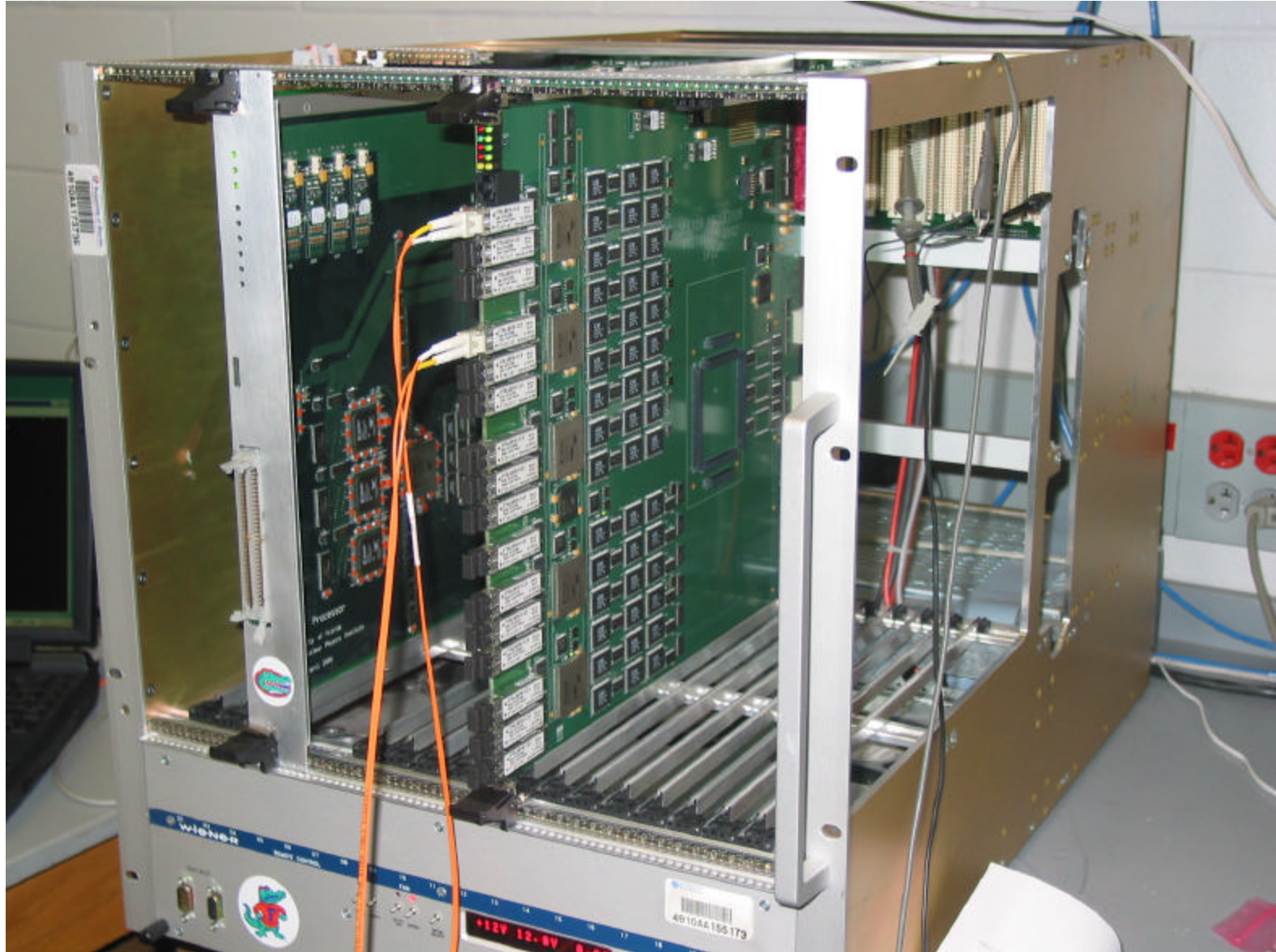
# Next Generation Sector Processor







# Tests underway...





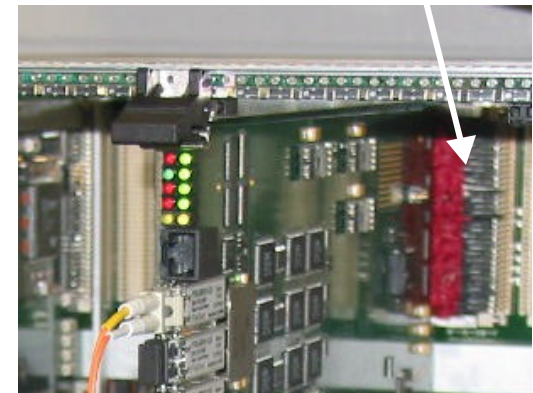


# Track-Finder Test Plans

## Tests

- Both SP main board and mezzanine board pass power-up and initial FPGA programming tests
  - EEPROMs programmed via JTAG through VME bus
- Validation of VME interface is underway
- Optical link tests are next

Oops...



## Approximate schedule

- Feb.'03: SP prototype completed, initial tests begin
- Mar.'03: MPC® SP optical link tests
- Apr.'03: SP trigger logic tests
- May.'03: CSC system tests with cosmic rays and beam tests at CERN
- June '03... : Tests with Muon Sorter and DT Track-Finder





# CSC Muon Sorter

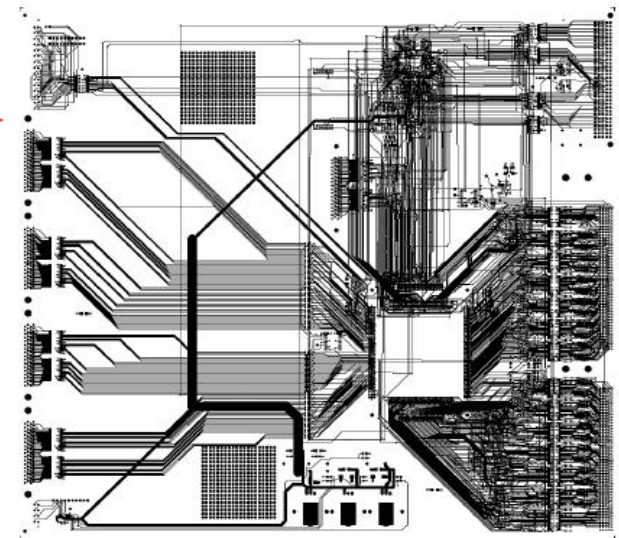
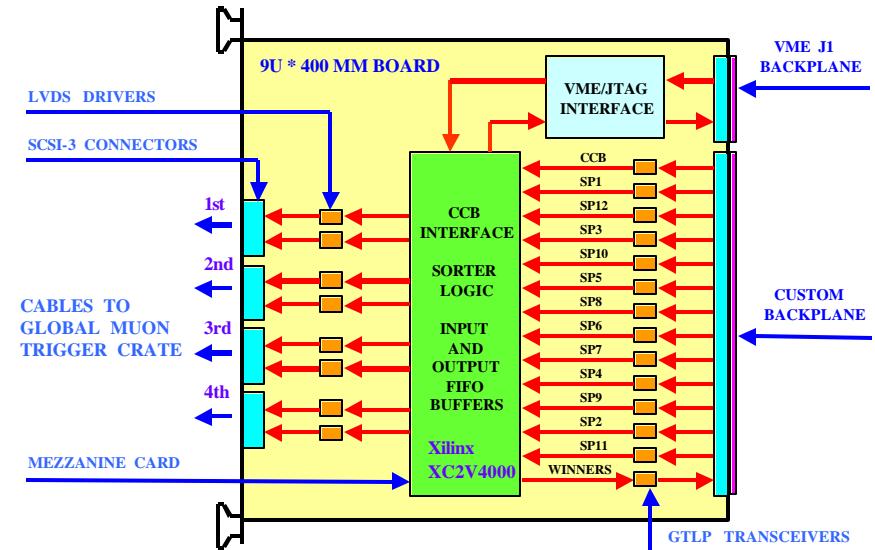
Rice Univ.

## Functionality

- Selects 4 best muons out of 36 arriving from 12 Sector Processors
- Sorting is based on 7-bit Rank
- Transmits 4 best muons to Global Muon Trigger crate over LVDS links in ranked order

## Status

- Board layout just completed
- Expect 3 PCBs in early March
- Uses same mezzanine card as SP
- Standalone tests in March-May
- Tests with SP starts in summer





# CSC Track-Finder Control and DAQ

**A draft document on the control and DAQ software framework for CSC Track-Finder has been started:**

- <http://www.phys.ufl.edu/cms/tfcvs/cgi-bin/cgi/viewcvs.cgi/TrigDAQ/doc/trigdaq.ps>
- (includes brief description of data format)

**Inputs and outputs of Sector Processors are read out upon L1A (including Sorter “winner bits”)**

- Useful for High Level Triggers as well as monitoring and debugging
- Send by optical links to an Endcap Muon FED





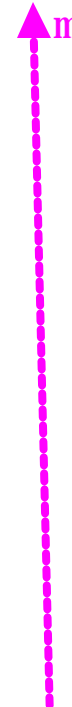
# Study: $P_T$ Misassignment from Muon Bremsstrahlung

- Poor  $P_T$  assignment is caused by track segments not collinear with actual muon.
- We should be able to eliminate these segments by examining all  $Df$  values from 4 ME stations.
- Example, for Generated  $P_T=75$  GeV, reconstructed  $P_T=14$  GeV:

## Overlapped Event Display

- $Df_{12} = 1$  Strip
- $Df_{13} = 1$  Strip
- $Df_{23} = 1.5$  Strips
- $Df_{24} = 1$  Strip
- $Df_{34} = 1/2$  Strip

Station 3 Hits  
Station 2 Hits



Should be  $< 1$  strip

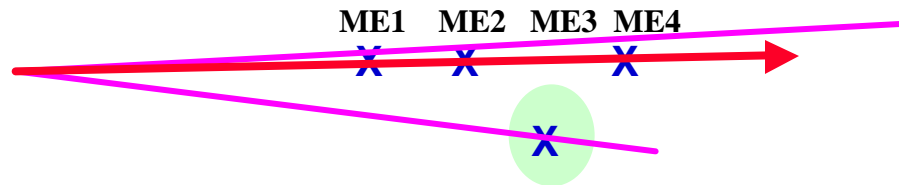






We can eliminate bad LCTs by adding some simple “trajectory cleaning” logic within the Sector Processor.

For Example:



- If  $|Df_{13}| > |Df_{12}|$  AND
  - $|Df_{23}| > |Df_{24}|$  AND
  - $|Df_{13}| > \text{threshold}$ ,
- \ should drop ME3 segment from track and use  $(Df_{12}, Df_{24})$  for  $P_T$  assignment.

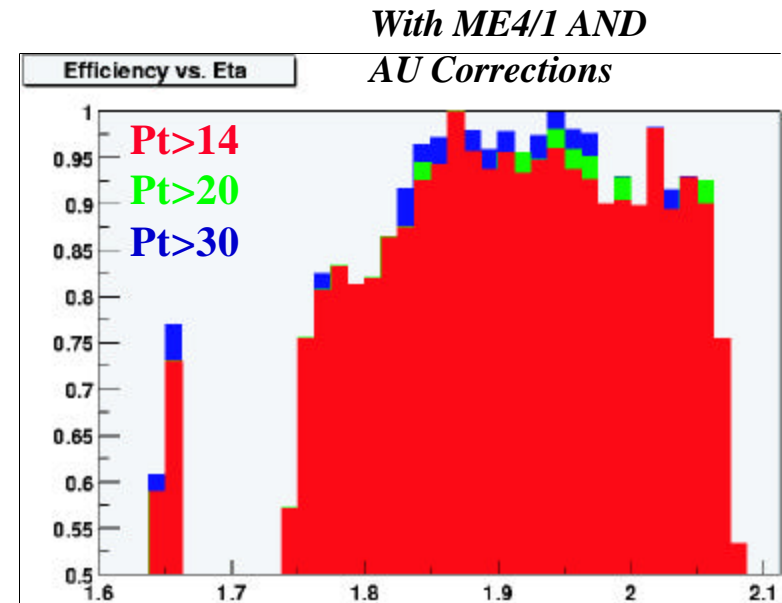
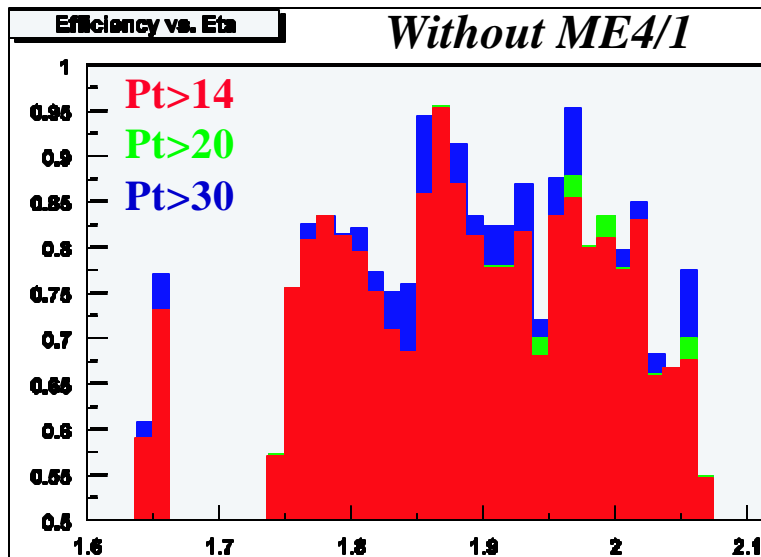
*n.b.* Translation to Verilog, and latency, must still be studied...





# TeV m Pt Assignment: Using ME4/1 and AU Correction

•Plot Level-1 trigger efficiency for  $P_T=300$  GeV ( $P \sim 1$  TeV) muons to pass “tight” (3-station) CSC T-F requirement for adequate rate reduction. ME4/1 does recover efficiency.



↑  
RPC Limit

ME4/2 | ME4/1

$1.8 < h < 2.1$  and  $Pt > 20$

**With ME4/1 AND AU Corrections:**

$\epsilon = 87.8\%$ , was 74% (No ME4/1)

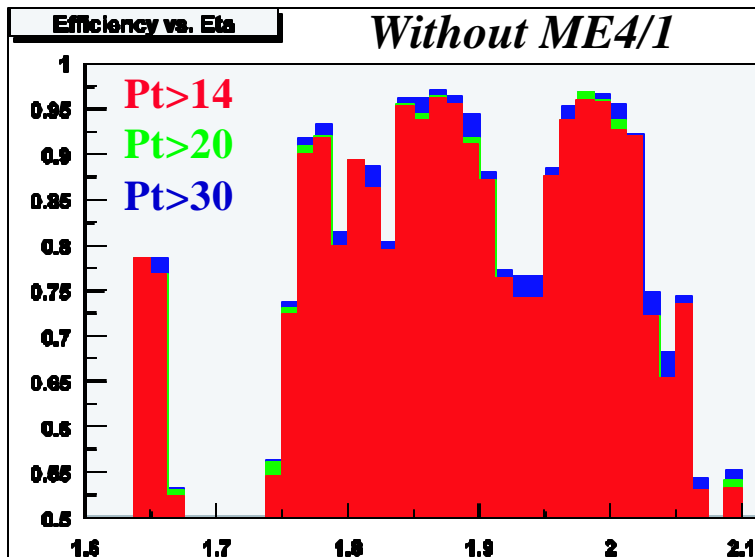
**De/e=15.4% !**





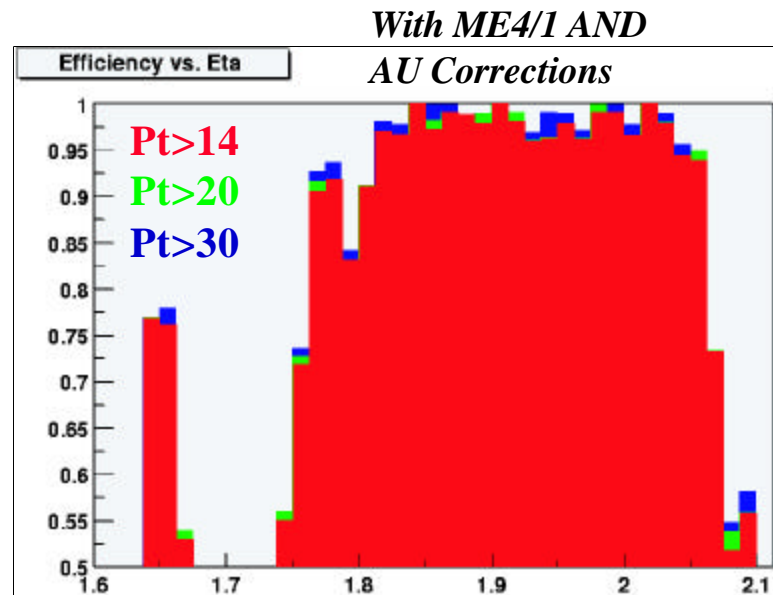
# 50<Pt<100 Assignment: Using ME4/1 and AU Correction

- Plot same CSC T-F efficiency for muons with 50 GeV<P<sub>T</sub><100 GeV to pass “tight” (3-station) requirement.



↑  
RPC Limit

ME4/2 | ME4/1



1.8 < h < 2.1 and Pt > 20

**With ME4/1 AND AU Corrections:**  
 $\epsilon = 92.6\%$ , was 82% (No ME4/1)

**De/e = 11.5%**

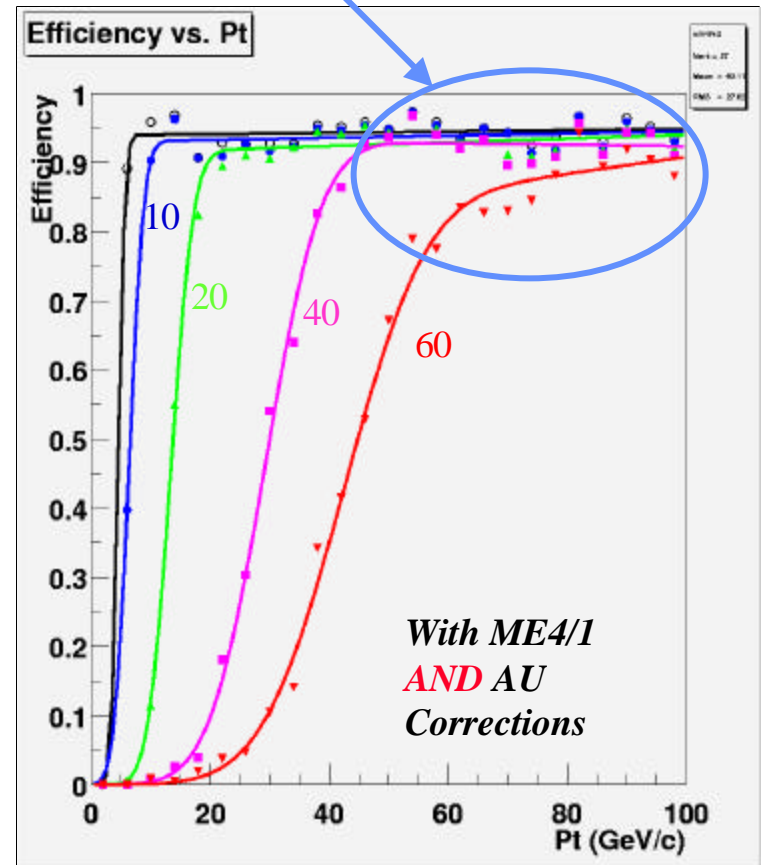
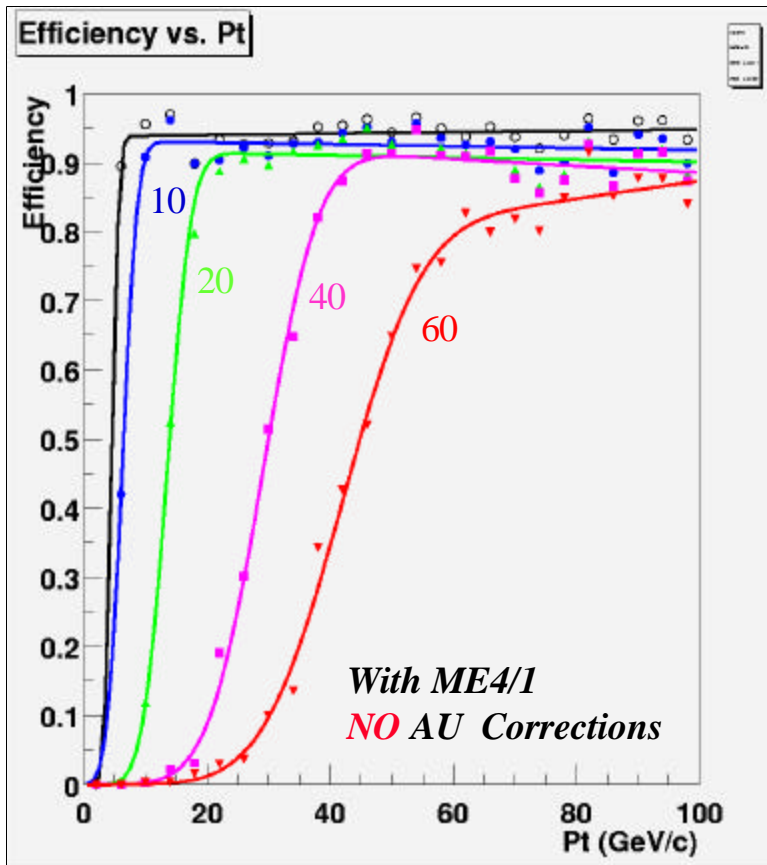




# 50<Pt<100 Assignment: Using ME4/1 and AU Correction

- Plot Pt Efficiency for muons with 50 GeV<P<sub>T</sub><100 GeV.

Note: Negative Slopes disappear



B. Scurlock





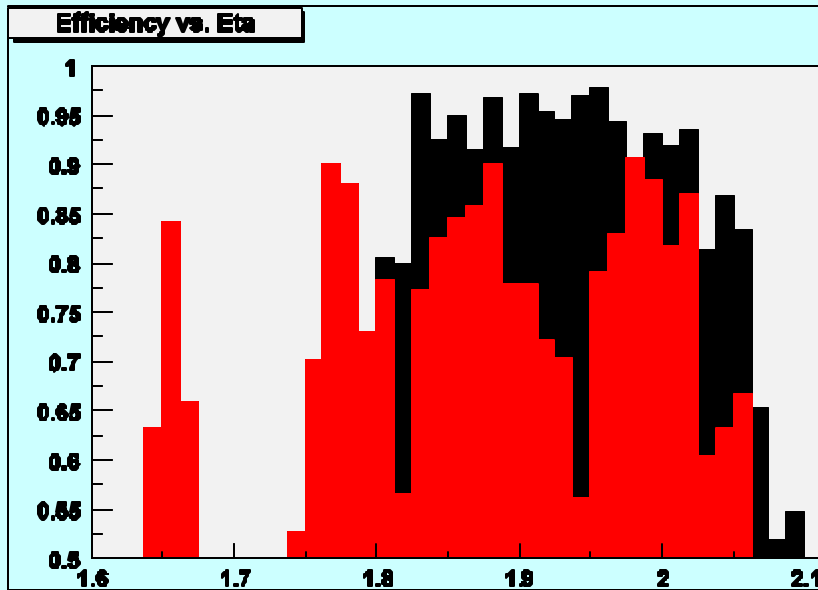


# Adding Neutrons at $L = 3 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$

$P_T > 20$

↑ Conservative choice

## Single TeV m Events

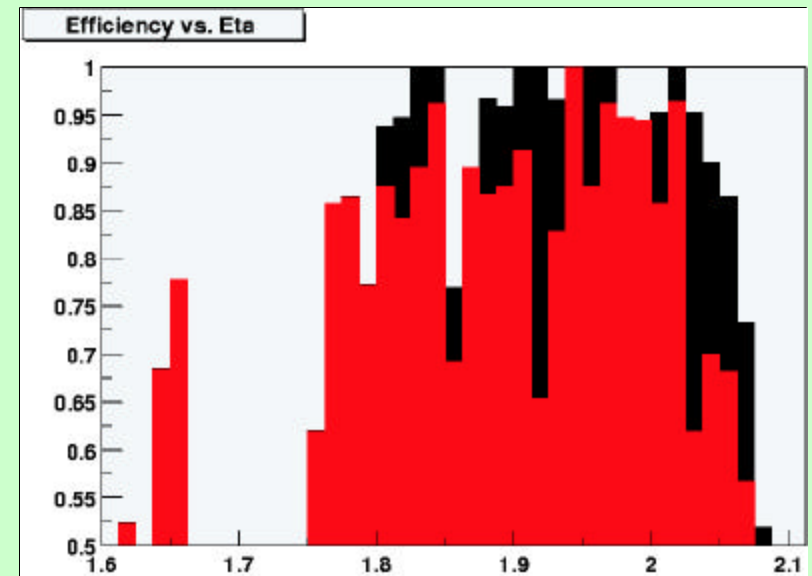


Without ME4/1:  $e = 72\%$

With AU Corrections:  $e = 86.3\%$

$De/e = 20\%$

## Single m Events $50 < P_T < 100$



Without ME4/1:  $e = 79.5\%$

With AU Corrections:  $e = 90.8\%$

$De/e = 14\%$

Even larger improvement seen





# Summary of Study

In Region  $1.8 < h < 2.1$ :

$e$	No Neutrons No ME4/1	No Neutrons AU Correction	With Neutrons No ME4/1	With Neutrons AU Correction
$50 < P_T^{\text{gen}} < 100$	82%	92.6%	79.5%	90.8%
TeV	74%	87.8%	71.9%	86.3%

$De/e$	Neutron Effect No ME4/1	Neutron Effect AU Correction	AU Correction Effect No Neutrons	AU Correction Effect With Neutrons
$50 < P_T^{\text{gen}} < 100$	-3%	-2%	+13%	+14.2%
TeV	-2.8%	-1.7%	+18.6%	+20%

Only works if we re-scope ME4...

