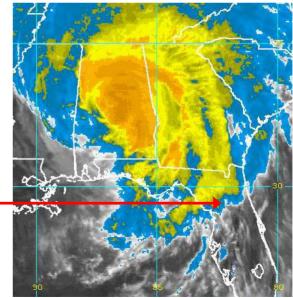
CSC Trigger Report:

Results from June 25 ns beam test Production plans Software

Darin Acosta University of Florida





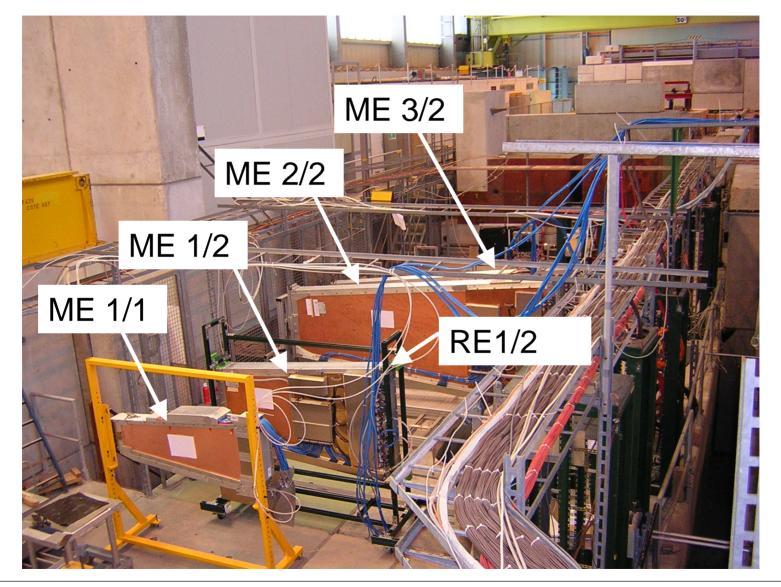
A Little Windy This Month



This is what a Category 1 hurricane did that was 200km away

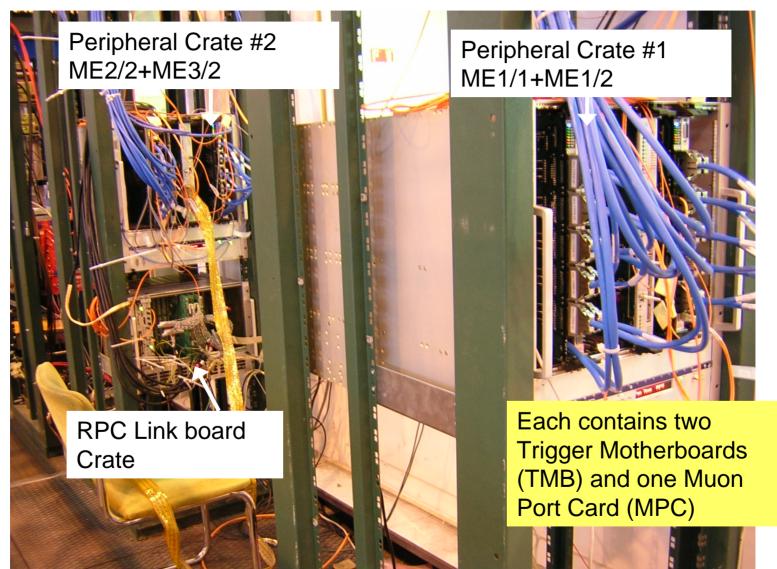


June 25ns Beam Test (Muon Slice Test)



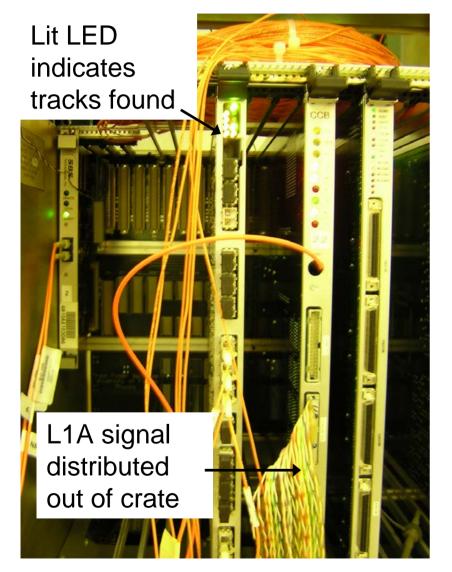


Peripheral Electronics Configuration





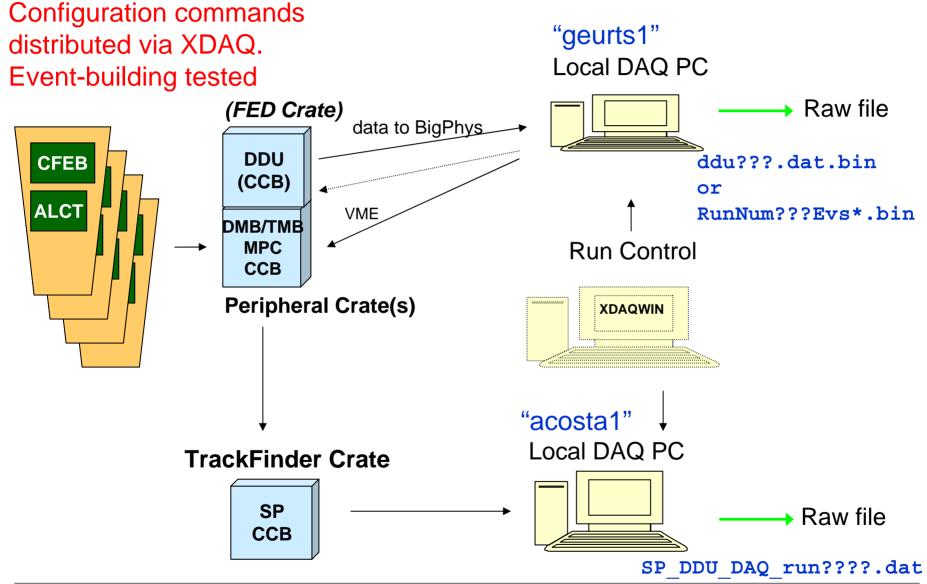
CSC Track-Finder



- First time we tested with full Track-Finding logic to identify tracks in data
- Full DAQ logging of inputs and outputs for offline comparisons
 - Can compare with data sent by Peripheral Crates as well as internal TF logic
- L1A generation a major synchronization accomplishment for trigger
 - Data must be aligned spatially and temporally
 - Very useful for slice tests



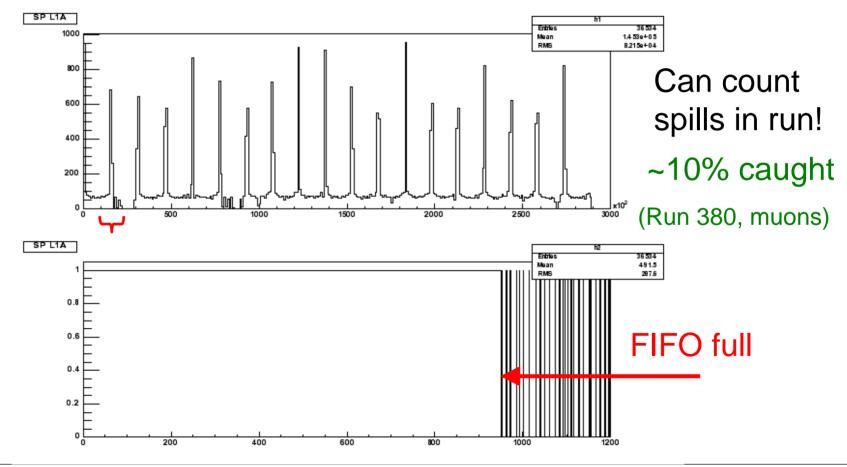
Test Beam 2004 DAQ Configuration





SP DAQ

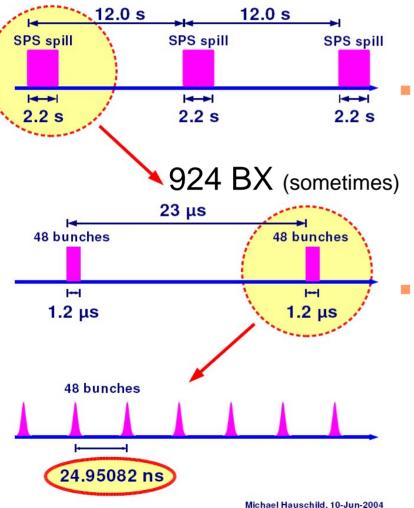
The Track-Finder DAQ is currently via VME read out, which is slow, since the CSC DAQ board (DDU) is still under development





25 ns Structured Beam

25ns Structured Beam 2004



LHC-like bunch structure during synchronous running

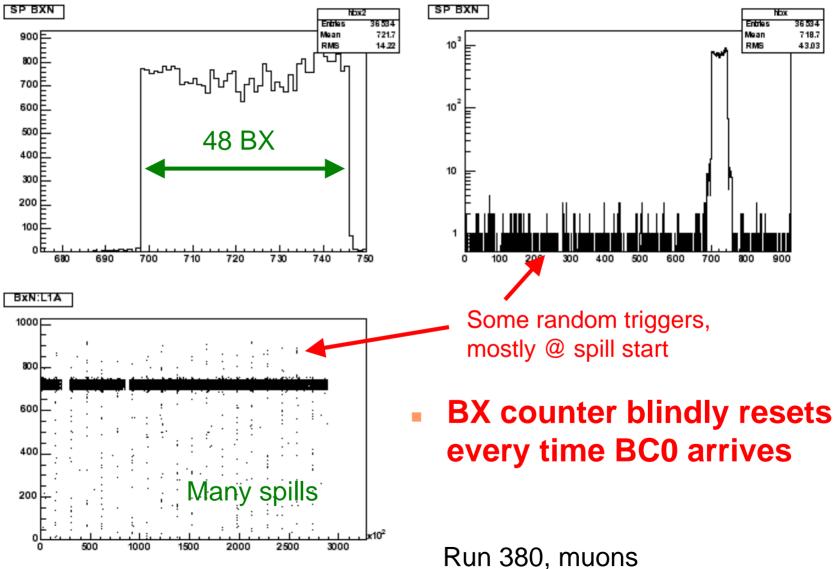
Trigger rates at X5A during spill

- Muons: 3–10 kHz
- Pions: >100 kHz

CSC readout system is designed for a L1A*LCT rate at LHC design luminosity of order 5 kHz



Sector Processor BX Distribution

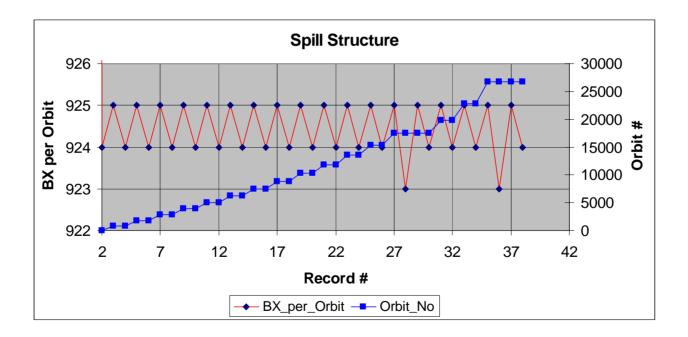




Plot below shows a single spill structure and looks like a ladder with narrow and wide steps.

Record 1 is omitted, since it serves only as a begin-of-spill mark. Each narrow step represents two successive orbits:

a 925bx orbit period immediately reverts to a 924bx orbit period. Each wide step represents four successive orbits, orbit period oscillates: 925bx -> 923bx -> 925bx -> 924bx.







Plots below show:

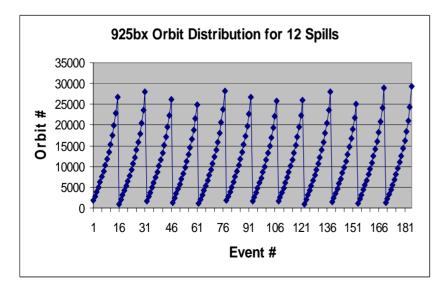
- → Distribution of orbit disturbances versus orbit # (versus time!)
- Distribution of orbits elapsed since previous orbit disturbance versus orbit number (versus time!), superimposed for 12 spills.

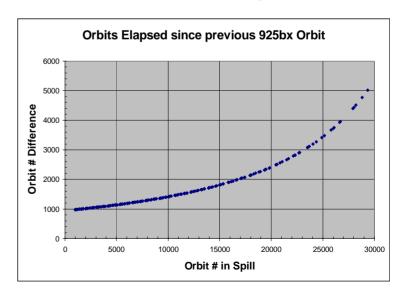
Only first orbit of the "ladder step" is plotted (remember, a disturbance always begins with a 925bx orbit).

Conclusion:

Orbit disturbances occur 15-16 times during first 0.7 sec (23 us * 30000) of spill.

If BC is synchronized to BC0 only at the beginning of spill, it will be apart from BC0 by 15-16bx to the end of spill -> BXN distribution of the events gets wider.



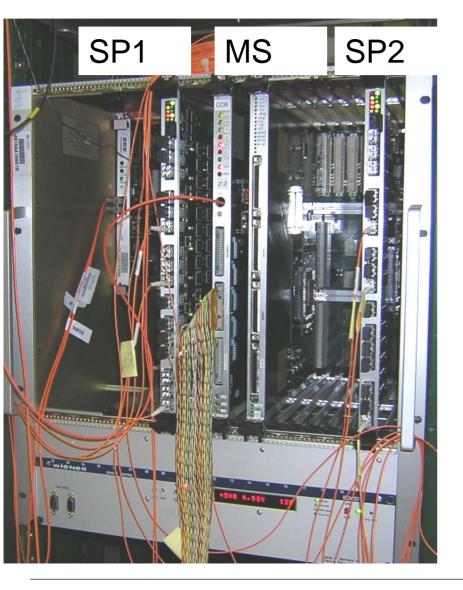


Trigger Meeting, July 30, 2004.



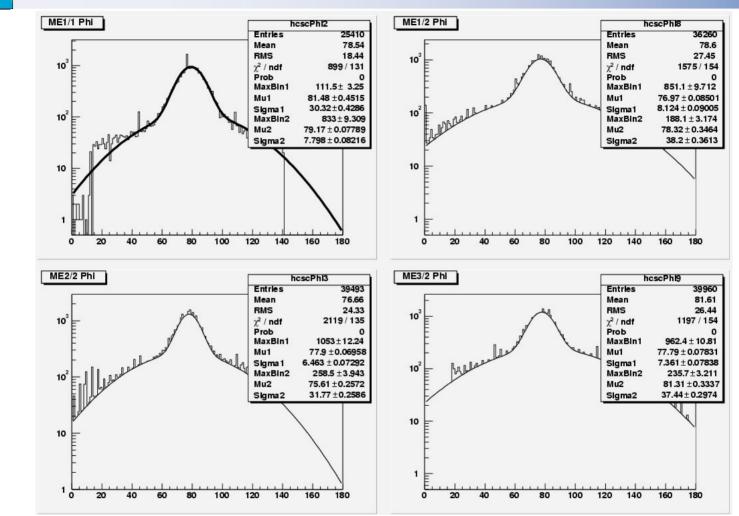


Track-Finder Crate Tests



- First test of multiple peripheral crates (multiple MPC) to TF crate
 - Synchronization test
- Various clocking solutions tried to test robustness of optical links
 - MPC used QPLL 80 MHz clock on backplane for all 25 ns runs
- First test of multiple
 Sector Processors (SP)
 to one Muon Sorter (MS)





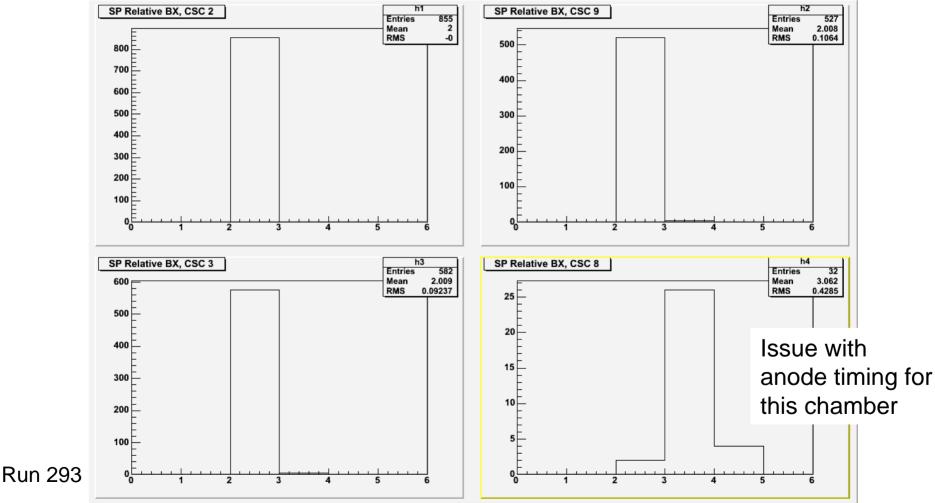
"Phi" was set equal to ½-strip units in each CSC, with alignment corrections applied in the SP LUTs

Run

380

Time Alignment of CSC data in Track-Finder

Able to get all trigger data from multiple chambers and crates on same BX (at least for some runs):

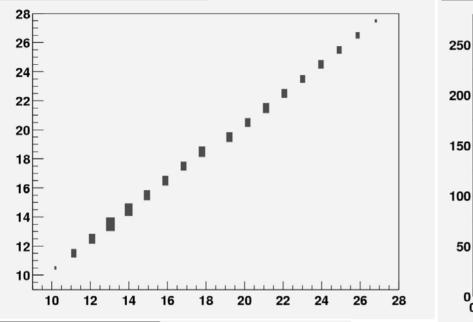


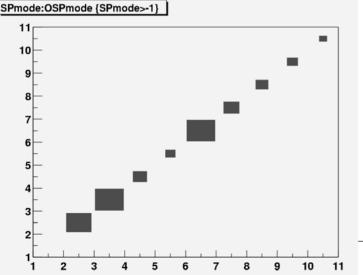


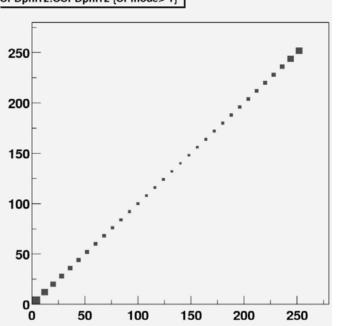
SP: ORCA vs. Hardware Check

SPeta:(OSPeta/2) {SPmode>-1}

SPDphi12:OSPDphi12 {SPmode>-1}







 Check logged outputs of SP with ORCA emulation based on inputs
 Correlation of track η, Δφ between 2 stations, and track type agrees perfectly
 Checked with 150K events



Track-Finder Beam Test Results

- Fully operational CSC TF tested with full data format
- Agreement between the output of the SP with a simulation based on the logged inputs is 100%
- Agreement between the recorded trigger primitive data (TMB) and received SP data is at the level of 99.7%, but worse for some chambers and runs
 - Same level of agreement as obtained from the Sep.'03 beam test
 - Likely to be due to DAQ issues from peripheral crates (data corruption from high rates)
- The SP in conjunction with a specially modified CCB was able to self-trigger the experiment (including RPC)
- Muon Sorter winner bits appear to be properly recorded
- New DT/CSC transition card works



October Beam Tests

- Will repeat and further refine system tests during
 October 25 ns beam test period at the H2 beam line
- Combined HCAL/EMU beam test





DT/CSC Transition Card Test

- In June '04 we tested a new DT/CSC transition card for the Track-Finder
 - New design solves connector space problem
 - Tester board allows loopback test without DT Track-Finder
 - Data pumped from input FIFO to output FIFO on SP
- Data test succeeded, except for 1 broken backplane pin
- Next step:
 - Second integration test with DT TF (Oct.'04 or later)





SP Production and Test Schedule

- Schematics for final design modifications completed
- Routing modifications submitted to vendor, about 2 weeks to complete
- Production to commence in October:
 - Will assemble 2 boards first as pre-production prototypes and test before launching full production (12 SR/SP + 4 spares + parts for 3)
 - Tests of initial samples expected to take 1 month
 - Rest of production completed by Feb.'05
- Testing of SP production boards completed by Apr.'05
- Full TF crate integrations tests (with Muon Sorter) completed by June '05
- Ready for tests at CERN June '05
 - 6 months later than milestone



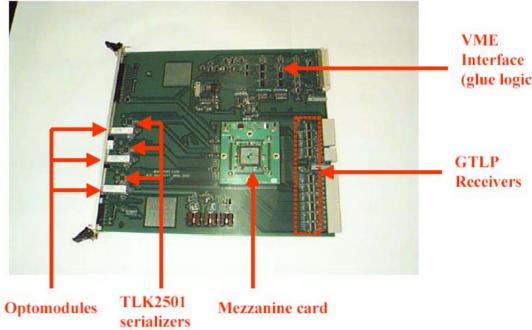
Detailed cost estimate performed

- FPGAs: \$4.1K/board
 - Main FPGA: \$1.1K/chip, 20 procured with TMB order
 - Others + EPROMs: \$3.0K
- Optics: \$1.4K/board
 - Working on ordering remaining quantity of original part # (Pin compatible replacement also available, but not tested)
 - TLK included
- Misc: \$2.0K/board
 - Includes LUTs, mezzanine and transition cards
- Setup, Fab., Ass.: \$2.5K/board
 - Main board + mezzanine + transition cards
- Estimated total: \$10K/board, \$190K total



MPC Status and Test Results

- 6 boards were built in 2002, all equipped with FPGA mezzanines
- Have been tested on the bench
- Have been tested with 7 Trigger Motherboards and one Sector Processor
- Have been checked in the peripheral crates at the beam test at CERN in September 2003 and June 2004
- Have been tested under irradiation at UC Davis cyclotron





MPC Production and Testing Plans

- Need to make ~20 changes in schematic/layout, add 4-5 small chips to VME interface. List of changes is being prepared
- Design documentation is available on the web at http://bonner-ntserver.rice.edu/cms/projects.html#mpc, including
 - specification
 - schematics
 - configuration file for EPROM
- 70 MPC motherboards will be built and assembled (including 15% spare)
 - will order ~5% more components for future repairs
- In-house testing (Matveev, Lee, Tumanov)
 - will use two crates and run testing patterns from TMBs through MPC to SP
 - software is under development (including convenient GUI)
- Burn in 24 hours at 60..70 C then test again (intend to use OSU oven)

MPC main board

- Components \$1025 x 70 = \$71,750
- Services (PCB & front panel fabrication, assembly)... \$500 x 70 = \$35,000 Mezzanine card
- Components and services for 70 cards (assembly, test at UCLA) ... \$65,970

Total..... \$172,720

Make schematic/layout changes and build 3 sample boards... Oct - Dec 2004Order all componentsOct - Dec 2004Assemble/Test 3 sample boardsJan - Feb 2005Need to test this sample with 9 TMB's in the production peripheral crateIf OK fabricate the rest 67 boardsMarch 2005Assemble and test 67 boardsApril – Aug 2005

8 months later than milestone



CCB Status and Test Results

- 6 boards were built in spring of 2004, all equipped with the TTCrq mezzanines
- Have been tested on the bench
- Have been tested with (almost) fully loaded peripheral crate
- Have been checked in the peripheral crates at the beam test at CERN in June 2004
- Have been tested under irradiation at UC Davis cyclotron





CCB Production and Testing Plans

- Need to make ~10 minor changes in schematic/layout. Do not expect to add or remove any active components on board.
- Design documentation (specification, schematics, configuration file for EPROM) is available on the web at http://bonner-ntserver.rice.edu/cms/projects.html#ccb
- 70 boards will have to be built and assembled (including 15% spare)
 - will order ~5% more components for future repairs
 - TTCrq mezzanines have been ordered from CERN, expect by December
- In-house testing (Matveev, Lee, Tumanov)
 - need just a short chain (TTCvi/vx+CCB+MT) to test the functionality
 - may use small 9U crate and run a program similar to irradiation test
 - need to enhance this program including convenient GUI

• Burn in 24 hours at 60..70 C then test again (intend to use OSU oven)



Components (including TTCrq mezzanine)..... \$530 x 70 = \$37,100
Services (PCB & front panel fabrication, assembly).... \$500 x 70 = \$35,000

Total......\$72,100

6 months later than milestone



Muon Sorter Current Status and Tests

- 4 boards were built in 2003, 3 boards are completely assembled
 - Need only 1 in final system
- Have 2 mezzanines assembled
- Two MS boards with mezzanines have been tested on the bench
- Have been tested with Sector Processor prototype
- Have been checked in the Track Finder crate during beam test at CERN in June 2004
- Do not require irradiation test





- Design documentation is available on the web at http://bonner-ntserver.rice.edu/cms/projects.html#ms, including
 - specification
 - schematics
 - configuration file for EPROMs
- Need more tests with at least 2 SP and/or 12 Muon Tester cards (until December of 2004)
- Need to test with the GMT receiver card (never been done before). This fall or early next year?
- Plan to complete all tests by summer 2005.
- Based on results, we should decide if the final PCB should be built (currently have 5-6 minor PCB fixes).



MS Cost Estimate

MS main board

• Components	< \$1000
Services (PCB & front panel fabrication, assembly)	< \$1000

Mezzanine card

• Components and services (FPGA, assembly) \$2500



CSC Track-Finder Configuration & Testing

Load

Load

🗌 Load

Load

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Verify

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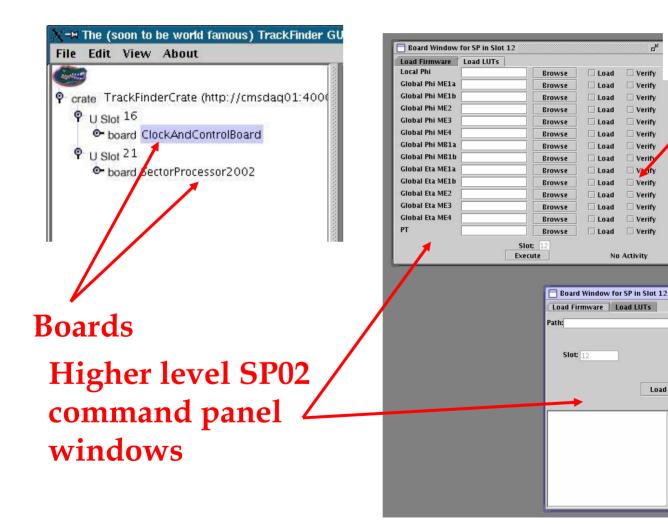
Verify

Verify

Verify

No Activity

Java interface to XDAQ-based software framework



e.g. LUT tests have verify feature

r × ×

Browse

No Activity

Chain:

Load



The Integrated EMU GUI

X-X EMU Commander (the TFGUI-RunControl Love Child File XDAQ Edit View Help

• 🗆 🗙

Crate TTC Crate (http://acosta1:40000) Crate TrackFinder Crate (http://acosta1:40000) Crate Peripheral Crate (http://acosta1:40100) The Track-Finder GUI has been extended to include

the XDAQ-based run control system for CSC beam tests

Controls 4 crates: 2 Peripheral crates, Track-Finder crate, TTC crate

DB calls to store configuration parameters

Evolving to become a Slicetest control

🛛 🦳 XDAQ output for host: acosta1:40000	🖞 🔤 🗂 XDAQ errors for host: acosta1:40000
-	<u> </u>
06-05-04 15:23:24,834 [1024] INFO [137.138.176.241:4000	
06-05-04 15:23:24,860 [1024] INFO [137.138.176.241:4000	
06-05-04 15:23:24,861 [1024] INFO [137.138.176.241:4000	
06-05-04 15:23:24,865 [1024] INFO [137.138.176.241:4000	
06-05-04 15:23:24,867 [1024] INFO [137.138.176.241:4000	
06-05-04 15:23:24,920 [1024] INFO [137.138.176.241:4000	
06-05-04 15:23:26,82 [1026] INFO [137.138.176.241:40000]	🗂 CMS Beam Test Run Control 🚽 🗹
06-05-04 15:23:26,121 [1026] INFO [137.138.176.241:4000	
	Help

GUIDriver XDAQ module \$Revision: 1.8 \$	Struct XML:

	Sequence File: Reset
GUIDriver_CTOR-INFO: Module load successful	
Goldhiver_chok-intro, module load successful	Hardware Config File:
4	
1	Number of Events: 1500
	Number of Events: 1500
	Set Run Type:
🛛 🗂 XDAQ output for host: geurts1:40100	
calling DDU::end	
BXR and EVTCNTRST	Set Run Number: 0 🔲 Automatic Run #
CCB: Start Trigger	
CCB BCO	Choose Command: UckeyeShiftTest 🔻 Choose Board: DAQMB 💌
CCB: BX-zero	
CCB: Enable TTC control	
CCB: CSRB1(read)=0xdff9changed to CSRB1(set)=0xdff8	Slot Number: Crate Number:
CCB: Enable L1A	
	Read XML File:
CCB: CSRB1=0xdf70	
TAKING DATA	
CCB: Disable L1A	Setup Start Stop Execute
CCB: CSRB1=0xdff8	
CCB: disable	Events: 1500 Type: Uninit
CCB: disable TTC control	
CCB: Stop Trigger	Run #: 0 Status: Ready
data taking disabled	Run #: 0 Status: Ready
data taning dibabica	-1
T XDAQ output for host: acosta1:40100	
	XDAQ errors for host: acostal:40100
37CSK1/1	
3/CSR1/1	
Enabled!	
Disabling TF and TTC Crates!	
3/B_GO_3_MODE/11	
3/B_G0_2_MODE/11	
3/B_GO_1_MODE/11	
3/B_GO_0_MODE/11	
3/CSR1/0	
3/L1AR/12	
3/L1AR/12	
12/CSRB1/57080	
12/CSRB1/57080	
10/VM/MA/CSR_FCC/256	
10/VM/MA/CSR_FCC/0	
10/VM/MA/CSR_FCC/0	
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