Status of CSC Track-Finder

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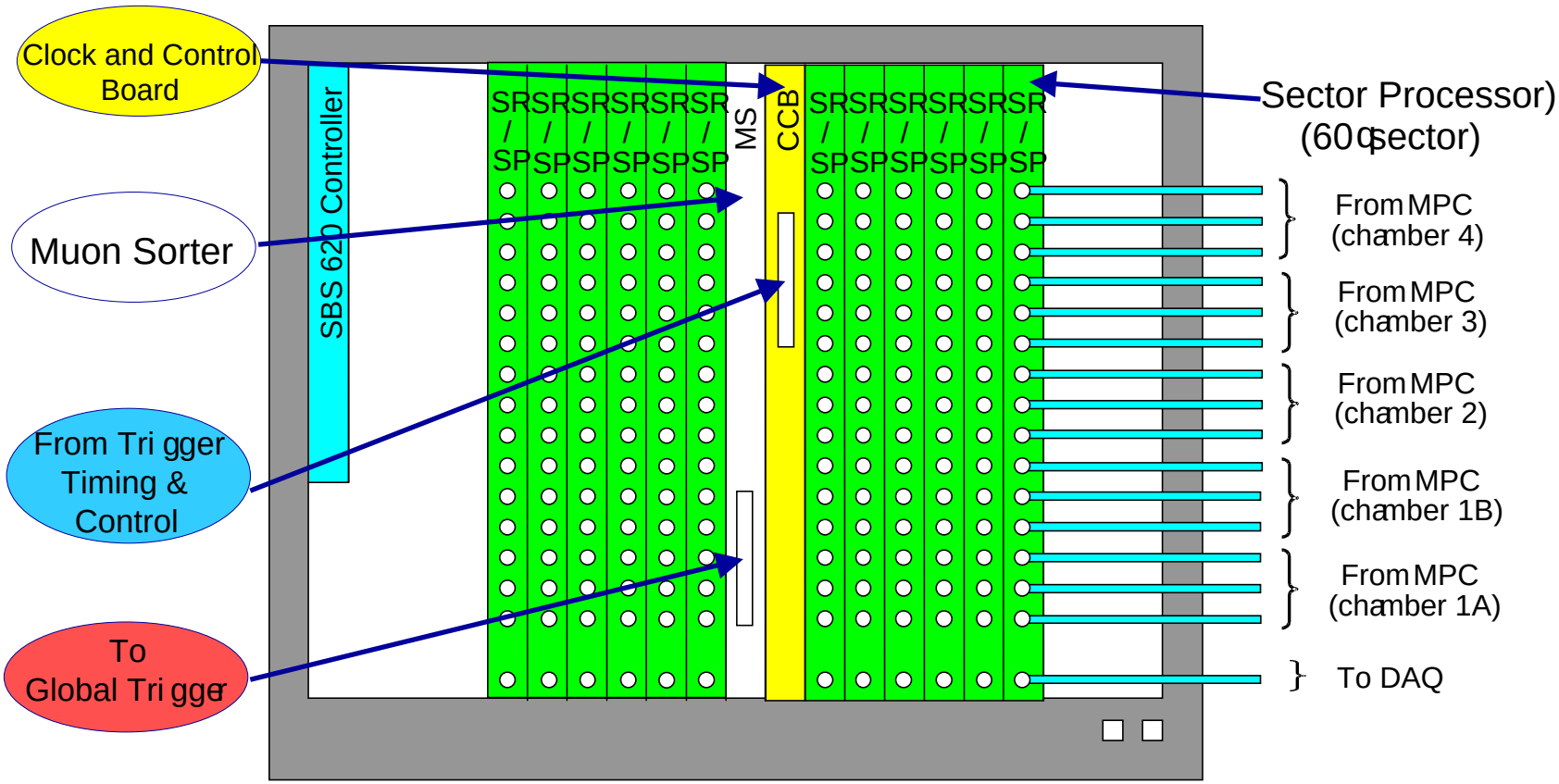
PNPI

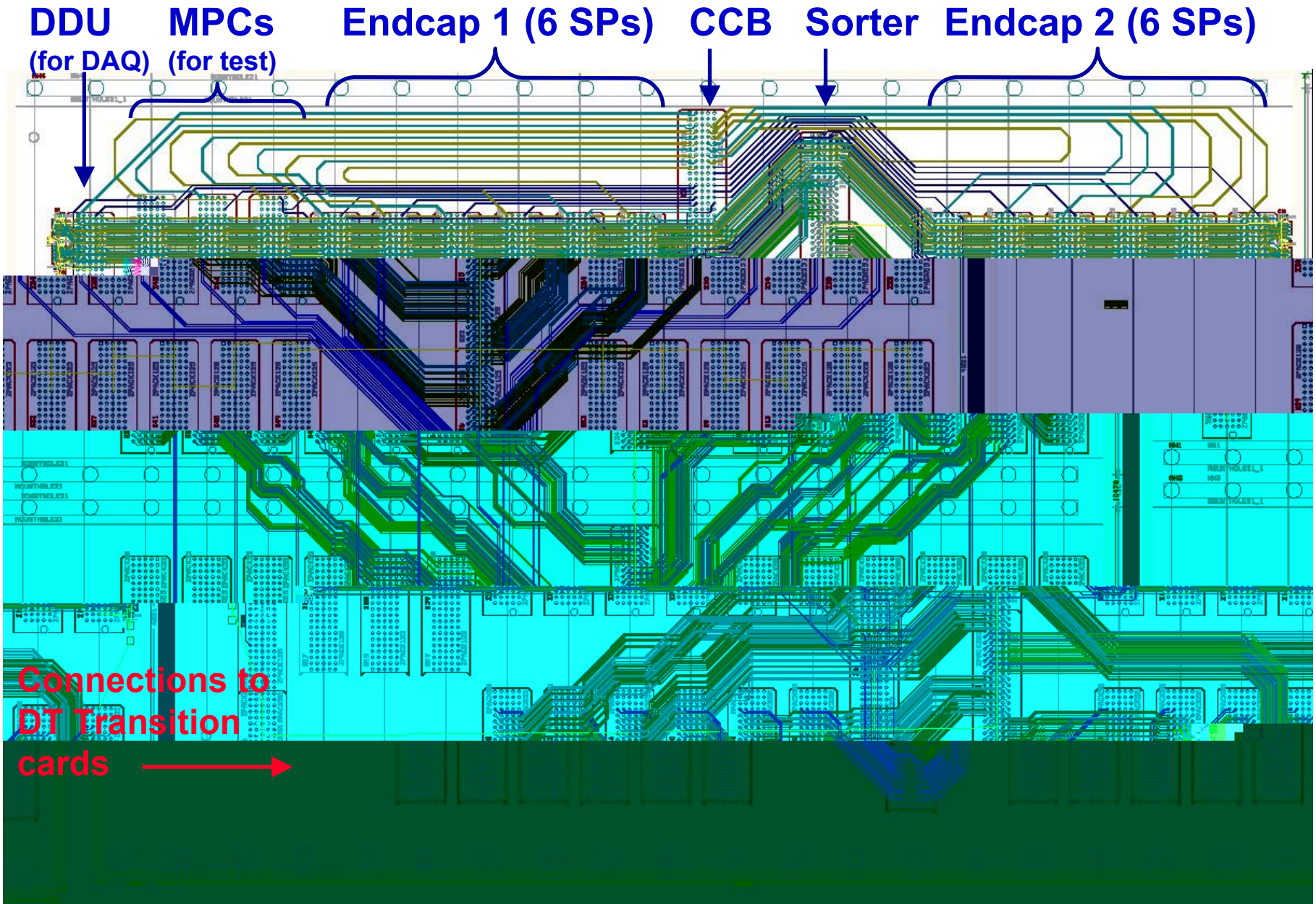
CSC Track-Finder Crate Design

Second generation prototypes

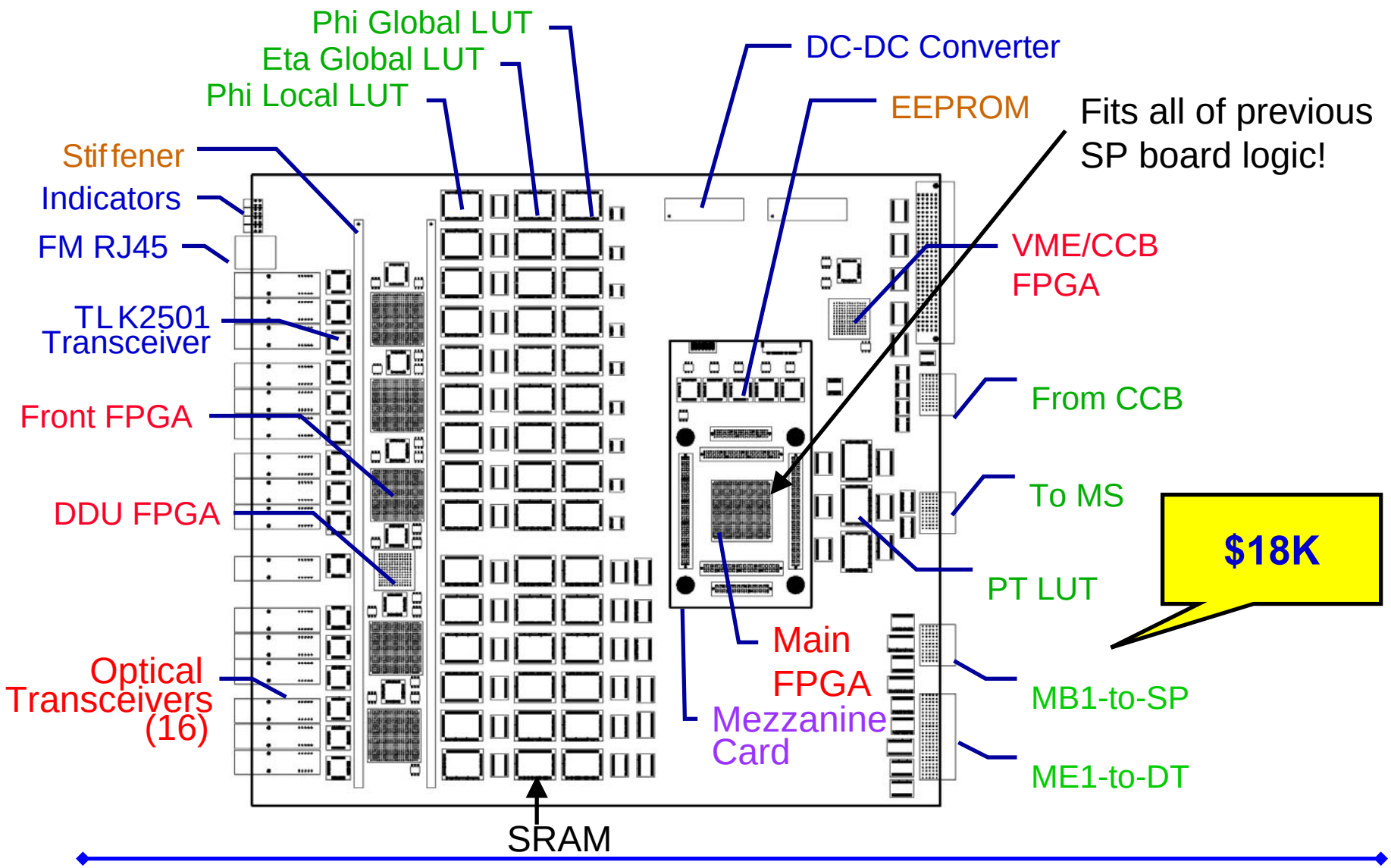


- Single Track-Finder Crate Design with 1.6 Gbit/s optical links

CSC Track-Finder GTLP Backplane



CSC Sector Processor (2nd Prototype)



Sector Processor Layout

16 layers

Sector Processor Status

Schematics complete

Mezzanine card layout complete

- **Submitted for fabrication**

Main board:

- **Problems encountered using OrCAD Layout**
  - **Board is too complex, manual routing is labor intensive, and program pushed to its limits**
  - **Suffered catastrophic failure**
- **Sent routing to outside vendor (Conquest) for completion (they use Cadence Allegro for layout)**
  - **Preliminary layout received Nov. 27**
  - **Reviewed by design engineers and completed Dec.19**
- **Fabrication complete**
  - **Board should be received today (in Florida)**
- **Assembly should take about 2 weeks**
  - **Prototype ready by end of January**

SP Firmware Development

1. **VME/CCB interface and Front FPGAs**
   - Started. Necessary for optical link tests to MPCs
   - Uvarov has draft document detailing VME registers
2. **SP chip**
   - Trigger logic done, but supporting logic still to do
3. **DDU (DAQ interface) firmware**
   - Started. Expect preliminary version in Feb.
   - Assume not critical for initial tests (i.e. will read out board via VME)

Plan to have preliminary version of first two items ready when board fabrication is complete

- Approximately end of January

Track-Finder Test Plans

Target schedule:

- Jan.'03: SP prototype completed
- Feb.'03: power-up and MPC o SP optical link tests
- Mar.'03: SP trigger logic tests
- Apr.'03: CSC system tests with cosmic rays
- May'03: beam tests with CSC chambers at CERN

Time is very tight, and still have a lot of firmware and software to write

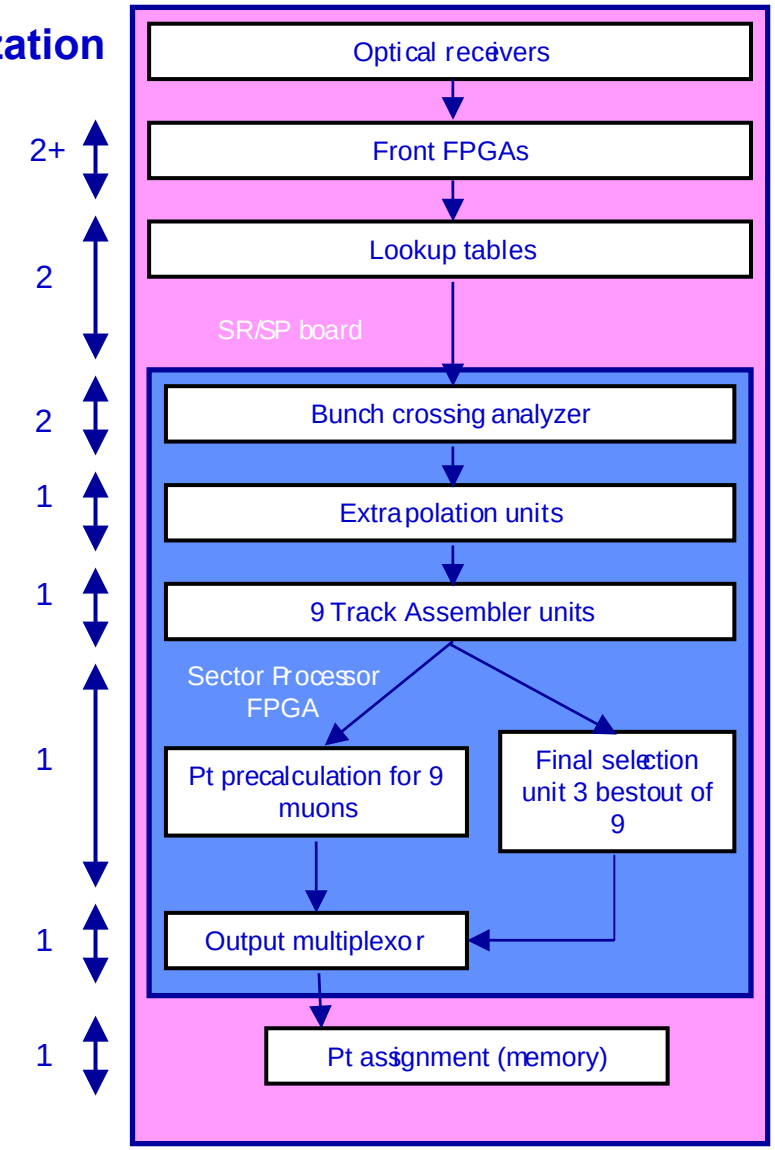
- Software will be written using XDAQ, hopefully in a way that is relevant for future slice tests of muon system

Need to start planning how to incorporate SP into multi-chamber tests with cosmics and test beam

- Will the SP generate L1A?
- How to integrate software for DAQ?

SP Latency

After de-serialization



Estimated total: 11+ BX

People involved with T-F software

Song Ming Wang

- Post-doc, 50% time, XDAQ interfaces and communication

Holger Stoeck

- Post-doc, 50% time, VME test software, code manager

Bobby Scurlock

- Student, full-time, VME test software, simulation code

Alex Madorsky

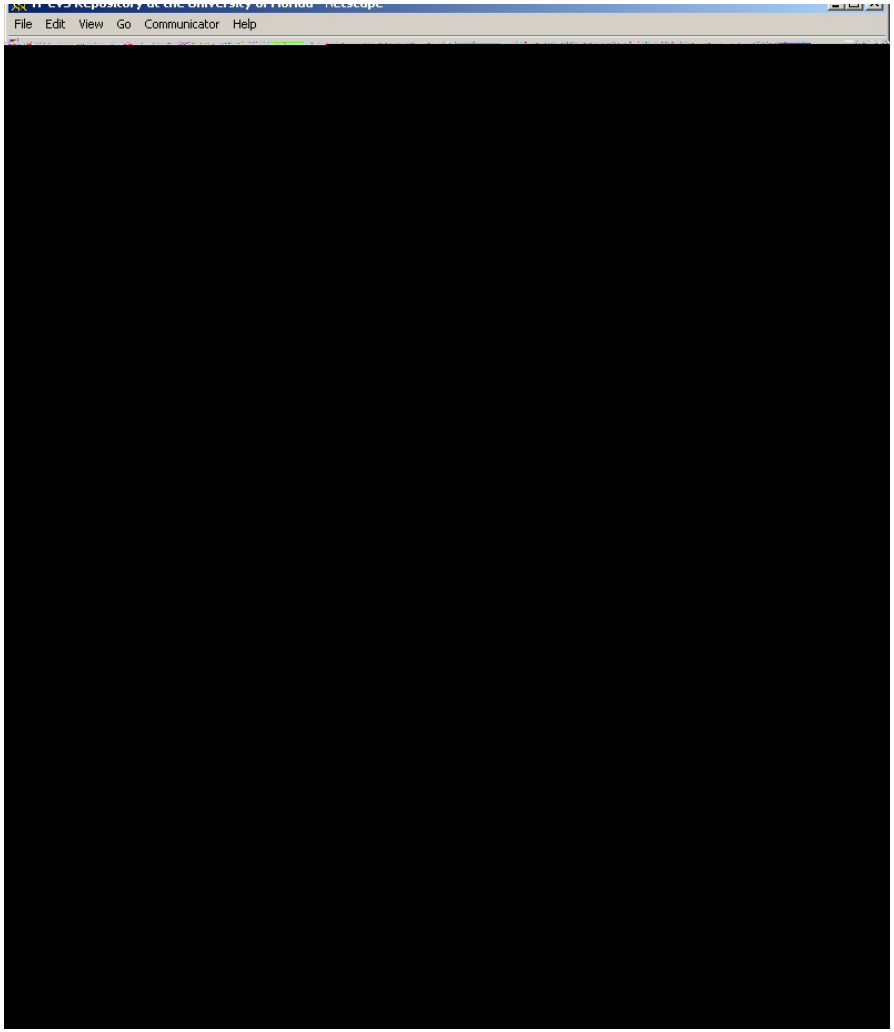
- HW and SW engineer, author of some original SP code and our “technical consultant” for new development
- 100% time during testing period in 2003

Longer term:

- Barashko and Drozdetski available to help with interface to EMU FAST-DAQ software (starting ~ March 2003)

CVS Repository and Web Page

http://www.phys.ufl.edu/~tfcvs



New Software and Test Plans

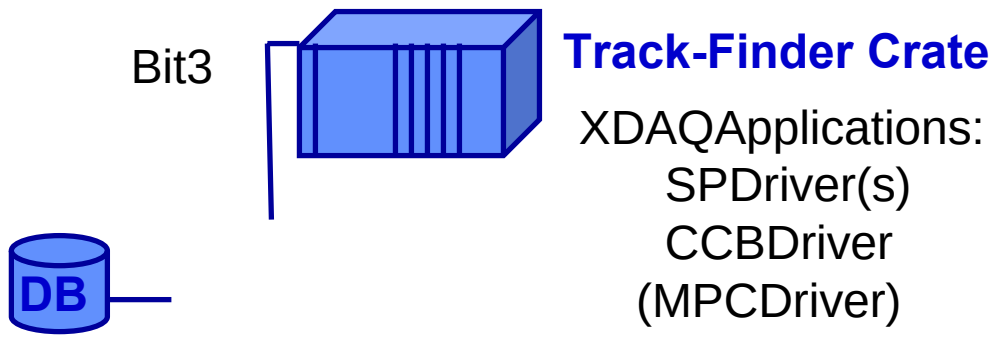
Implementing a XDAQ compliant set of software to run CSC trigger tests

VME control (using HAL library):

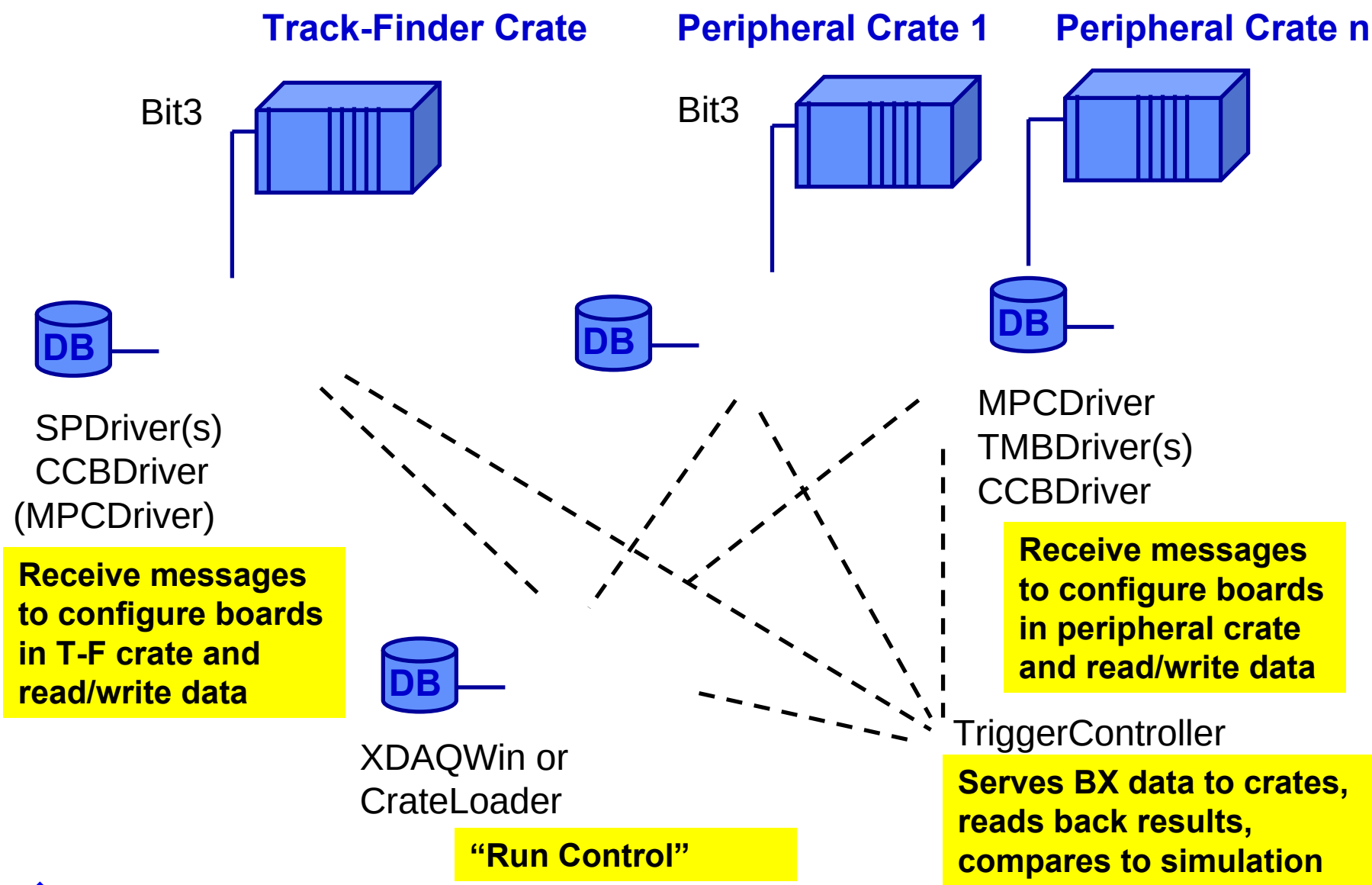
- **Classes exist for VME configuration of TMB, MPC, CCB, and TTC from Rice University (Greg Pawloski)**
- **Developed similar SP classes with additional capability to download LUTs and FPGAs from external files (done)**
  - **Integrated previous code from prototype tests in 2000**

"Front-End Drivers" (XDAQApplications)

- **Developing "Driver" classes that instantiate VME classes and execute configuration commands based on XDAQWin messages or SOAP message from other applications**
- **Could wrap existing non-HAL code here (i.e. Dynatem)**



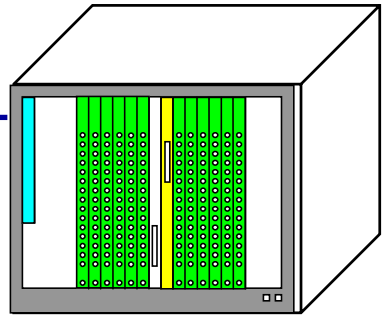
CSC "TrigDAQ" Implementation



Possible EMU DAQ System

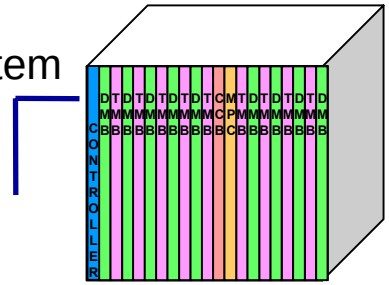
Track-Finder Crate

Bit3



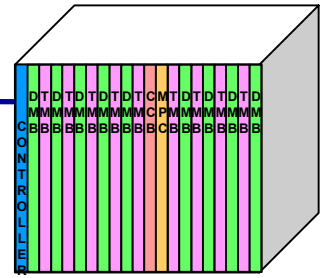
Peripheral Crate 1 . . .

Dynatem

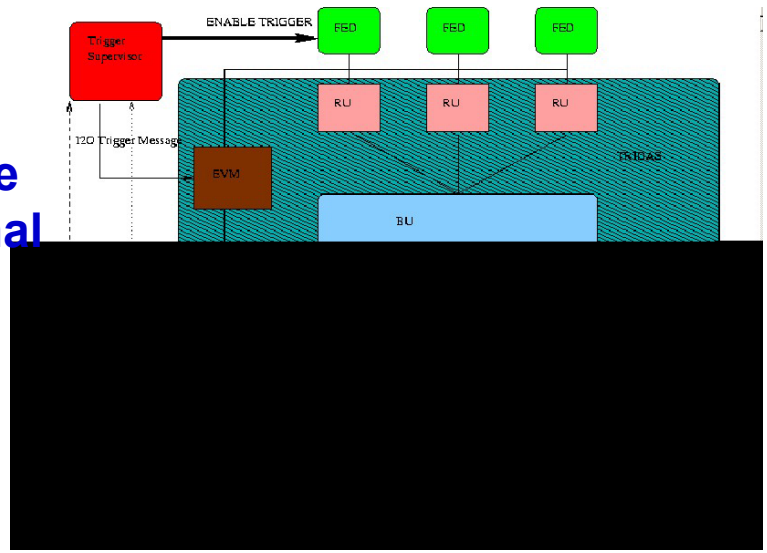


Peripheral Crate n

Dynatem

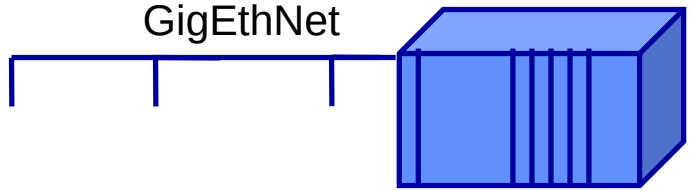


hardware for normal DAQ



DDU/DCC Crate(s)

GigEthNet



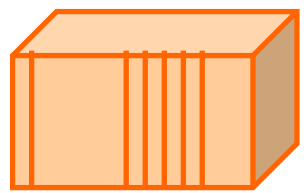
PC1

Farm for Local DAQ

PCn

TTC Crate

Bit3



Run Control

Event Builder/Logger

Monitoring