A 3-D Track-Finding Processor for the CMS Level-1 Muon Trigger

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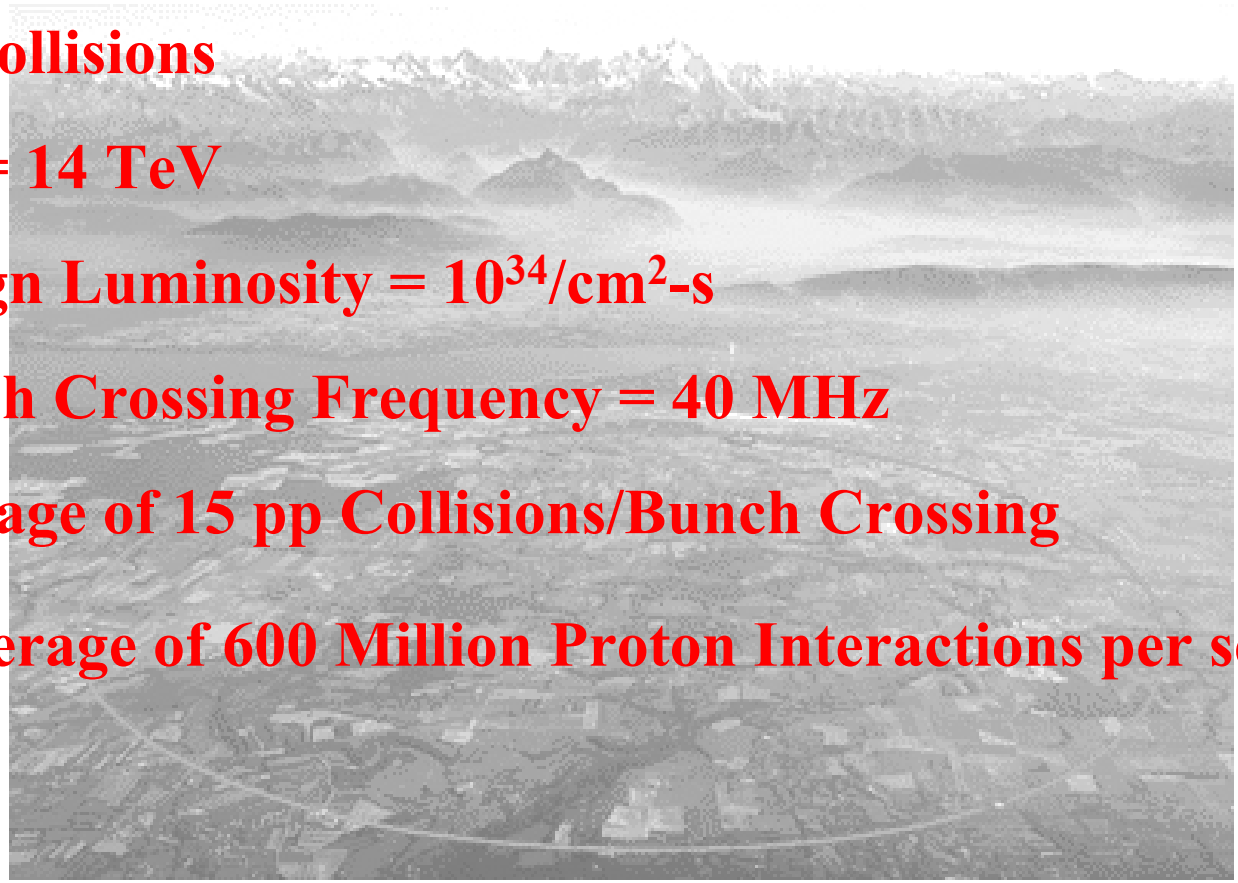
Outline

- Level-1 Trigger System
- Track-Finder Electronics
- First Prototype
- Pre-Production Prototype
- Firmware
- Test Results and Plans

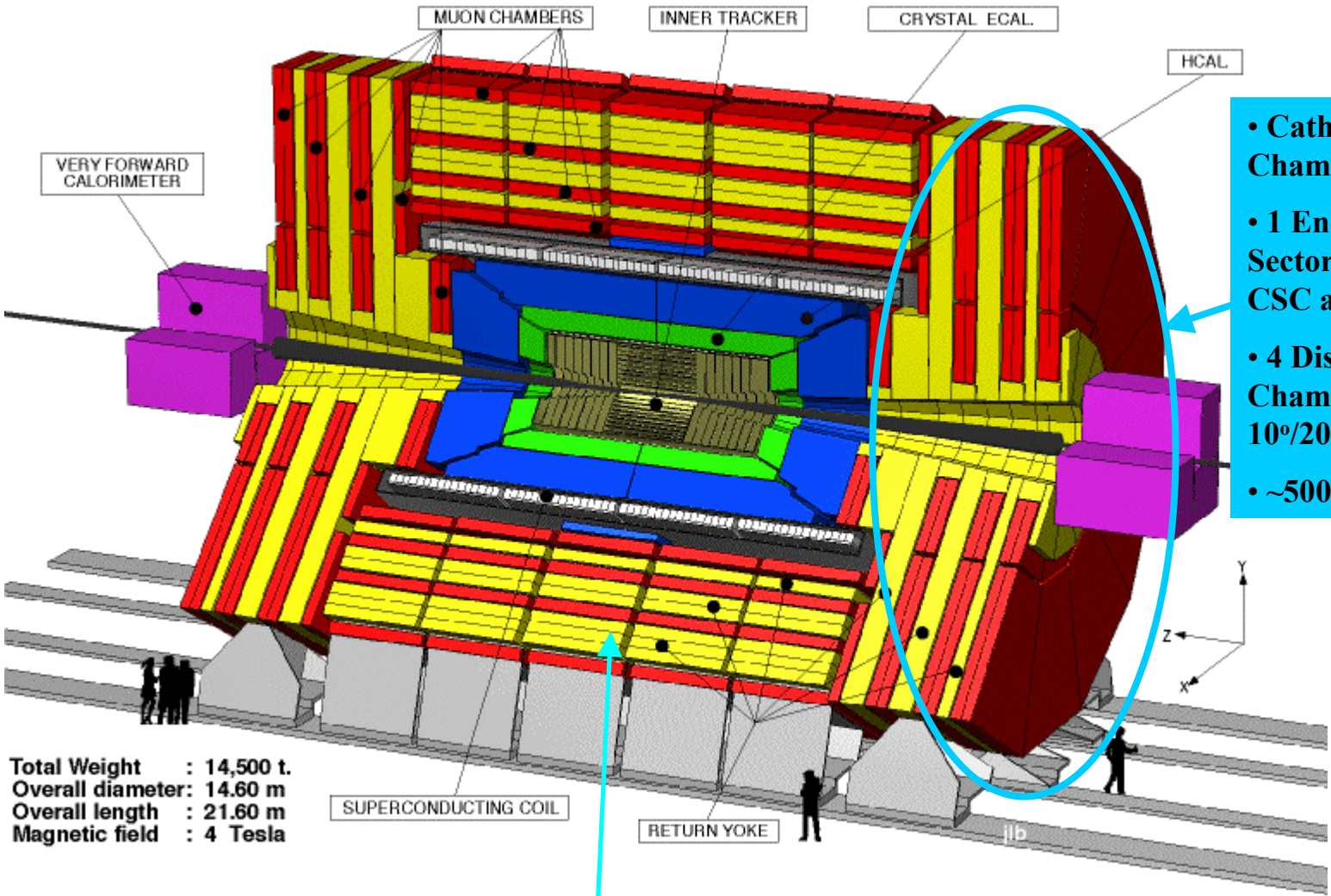
The LHC at CERN



- p-p collisions
- E_{cm} = 14 TeV
- Design Luminosity = $10^{34}/cm^2$-s
- Bunch Crossing Frequency = 40 MHz
- Average of 15 pp Collisions/Bunch Crossing

=> Average of 600 Million Proton Interactions per second!!

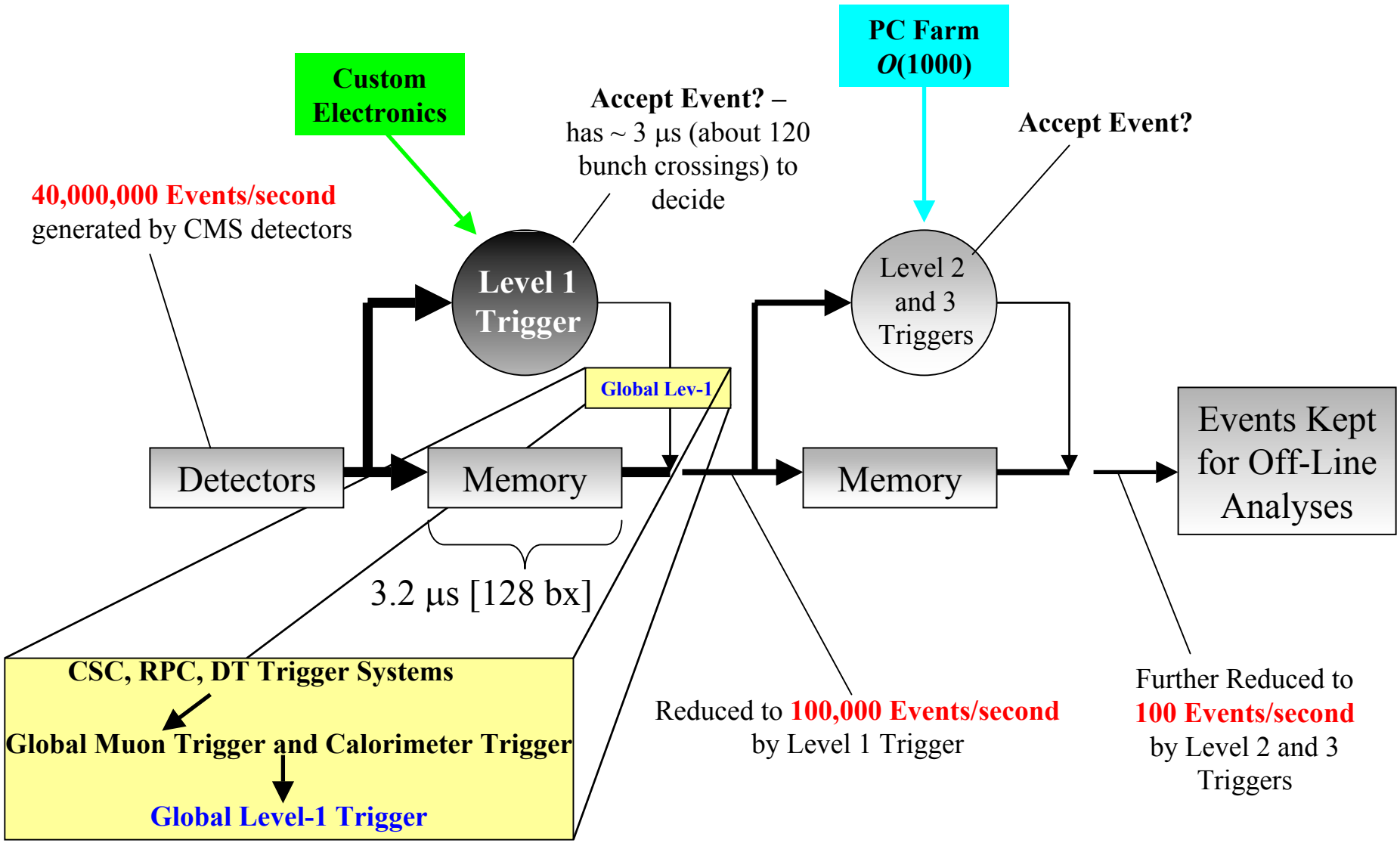
CMS Detectors



- Cathode Strip Chamber (CSC) System
- 1 End Cap = Six 60° Sectors which contain CSC and DT Detectors
- 4 Disks (Stations) with Chambers extending 10°/20° in azimuth
- ~500 Total Chambers

Drift Tubes and Resistive Plate Chambers

Trigger and Data Acquisition Scheme of CMS



CSC Electronics Scheme

CLCTs and ALCTs

[Through Channel Links: ~8m]

Track Segments

[Through Optical Fibers: ~100 m]

Track Finding Processor is implemented as 12 Sector Processors

[each for 60° azimuth].

CSC Front End Electronics

Peripheral Electronics

Sector Receiver/Sector Processor

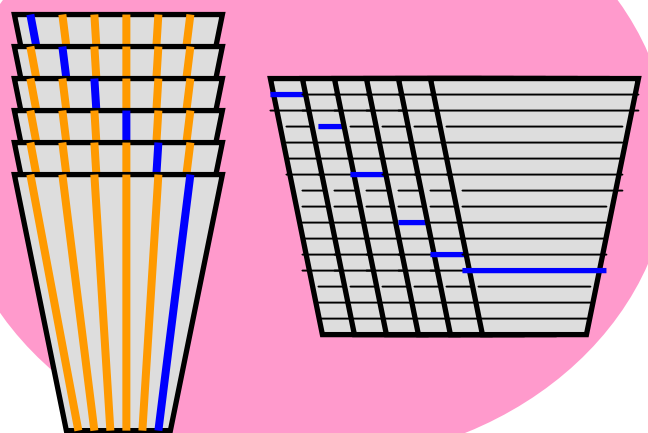
Best Muon Candidates

On Chambers

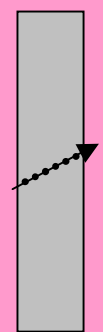
On Disks

In Counting House

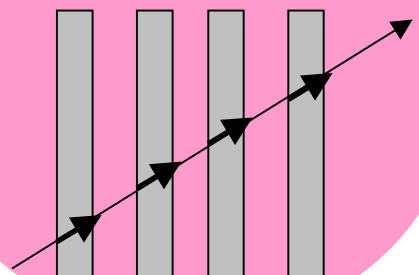
Forms Anonde Wire Patterns and Cathode Strip Patterns



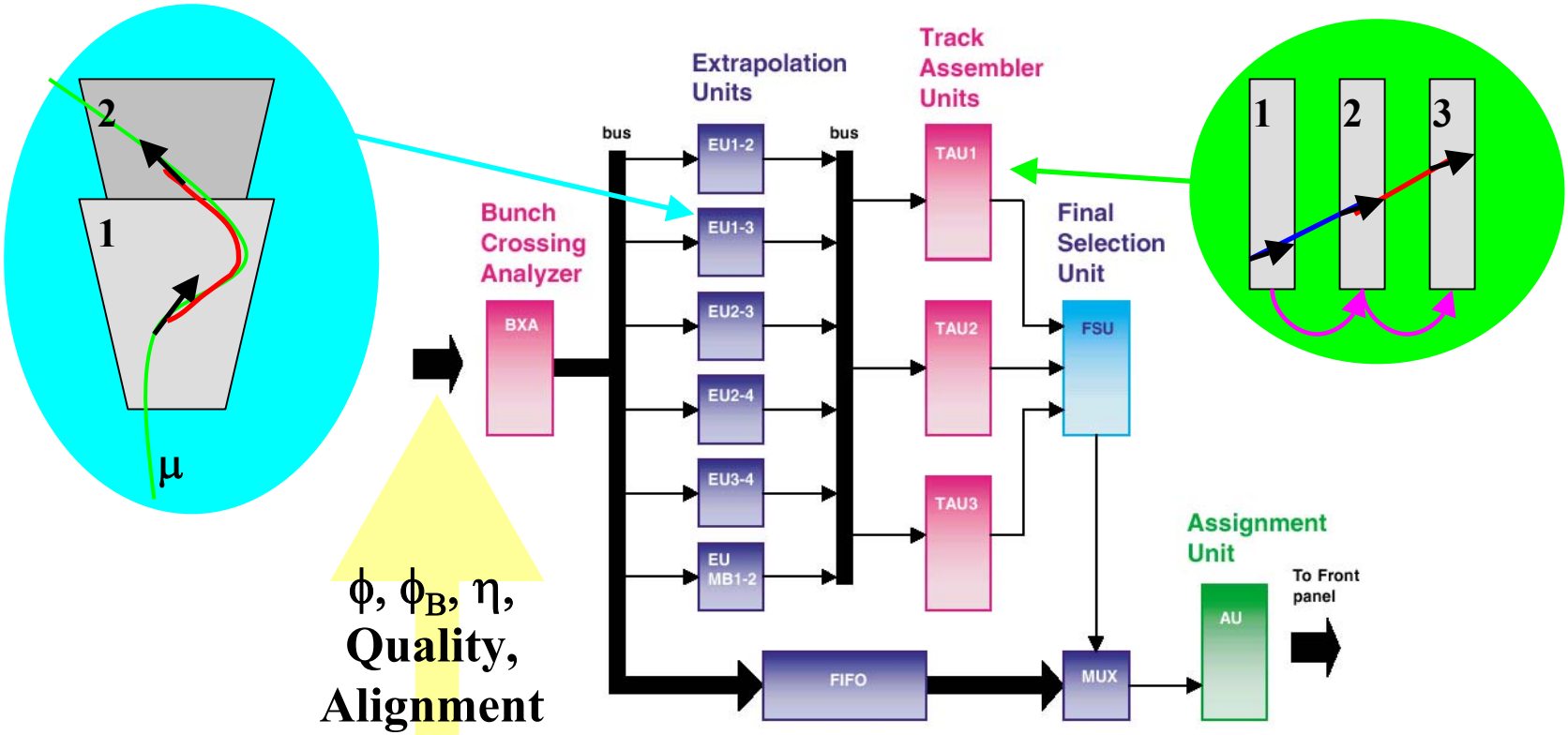
Constructs Track Stubs



Constructs Full Tracks



Basic Design of SR/SP Logic



Anode/Cathode Patterns

SR Logic

ϕ, ϕ_B, η, Quality, Alignment Corrections

BXA: Allows SP to analyze track segments received out of time.

EU: Test consistency of 2 track segments to share track.

TAU: Links successfully extrapolated segments.

FSU: Selects best 3 tracks, cancels redundant tracks.

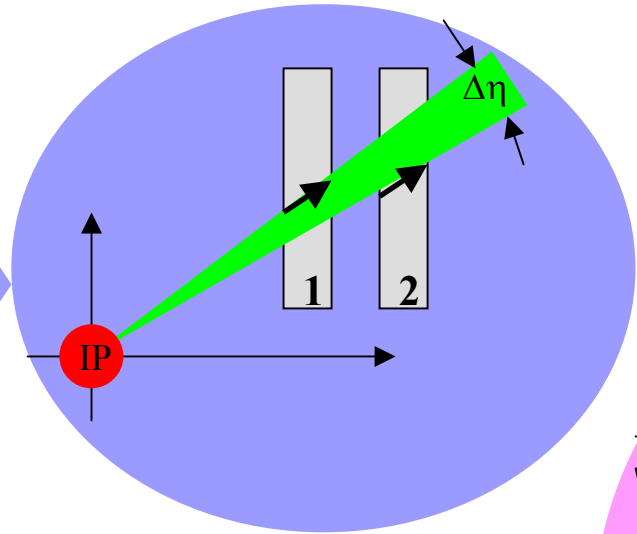
AU: Assigns P_t value and uncertainty.

Extrapolation Unit

η Road Finder:

•Check if track segment is in allowed trigger region in η.

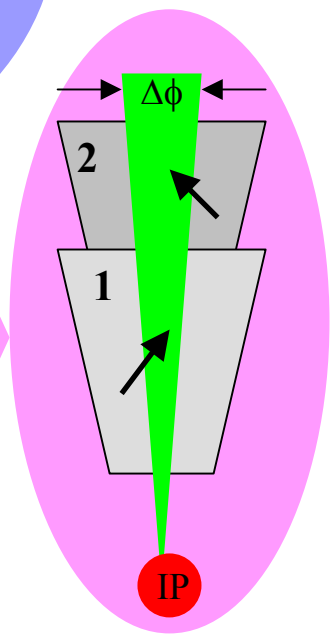
•Check if Δη and η bend angle are consistent with a track originating at the collision vertex.



φ Road Finder:

•Check if Δφ is consistent with φ bend angle ϕ_B measured at each station.

•Check if Δφ in allowed range for each η window.

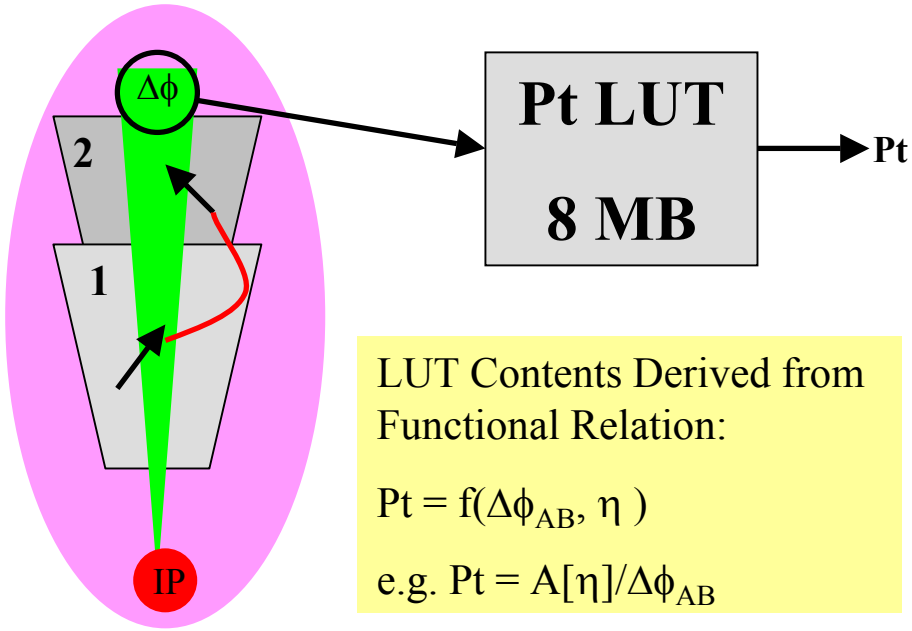


Quality Assignment Unit:

•Assigns final quality of extrapolation by looking at output from η and φ road finders and the track segment quality.

Extrapolation Units utilize 3-D information for track-finding.

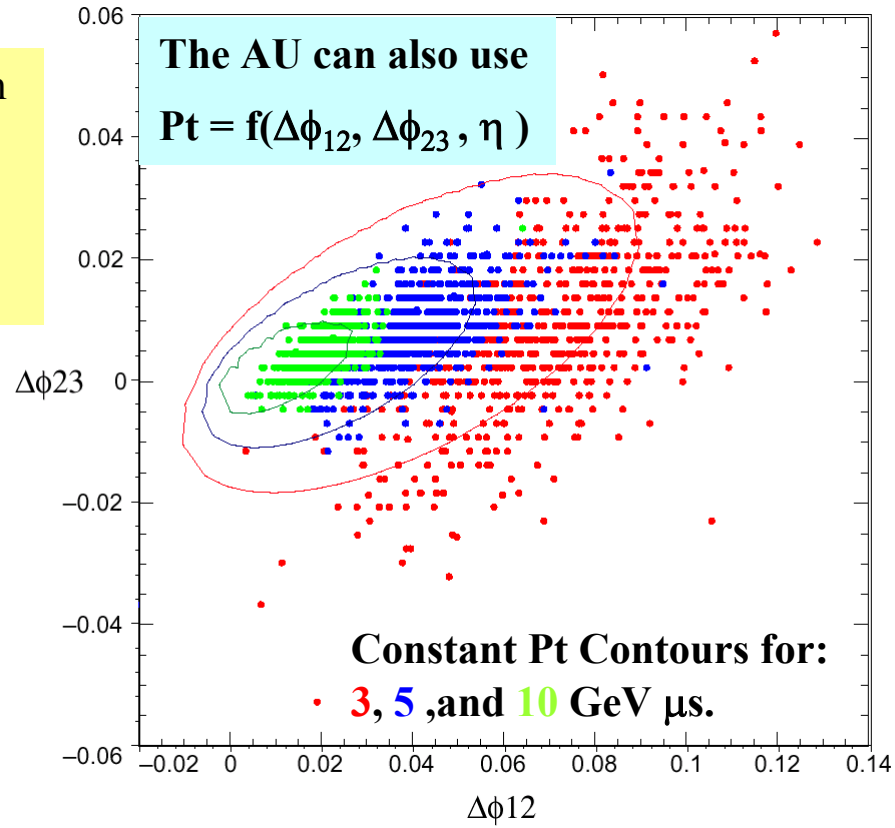
Pt Assignment Unit



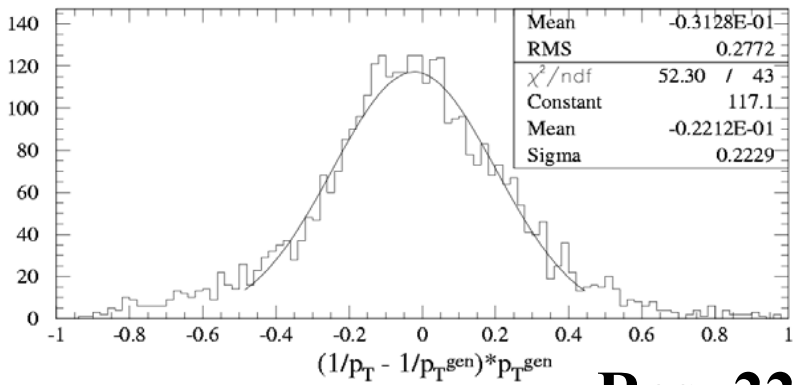
LUT Contents Derived from Functional Relation:

$Pt = f(\Delta\phi_{AB}, \eta)$

e.g. $Pt = A[\eta]/\Delta\phi_{AB}$



Residual Plot



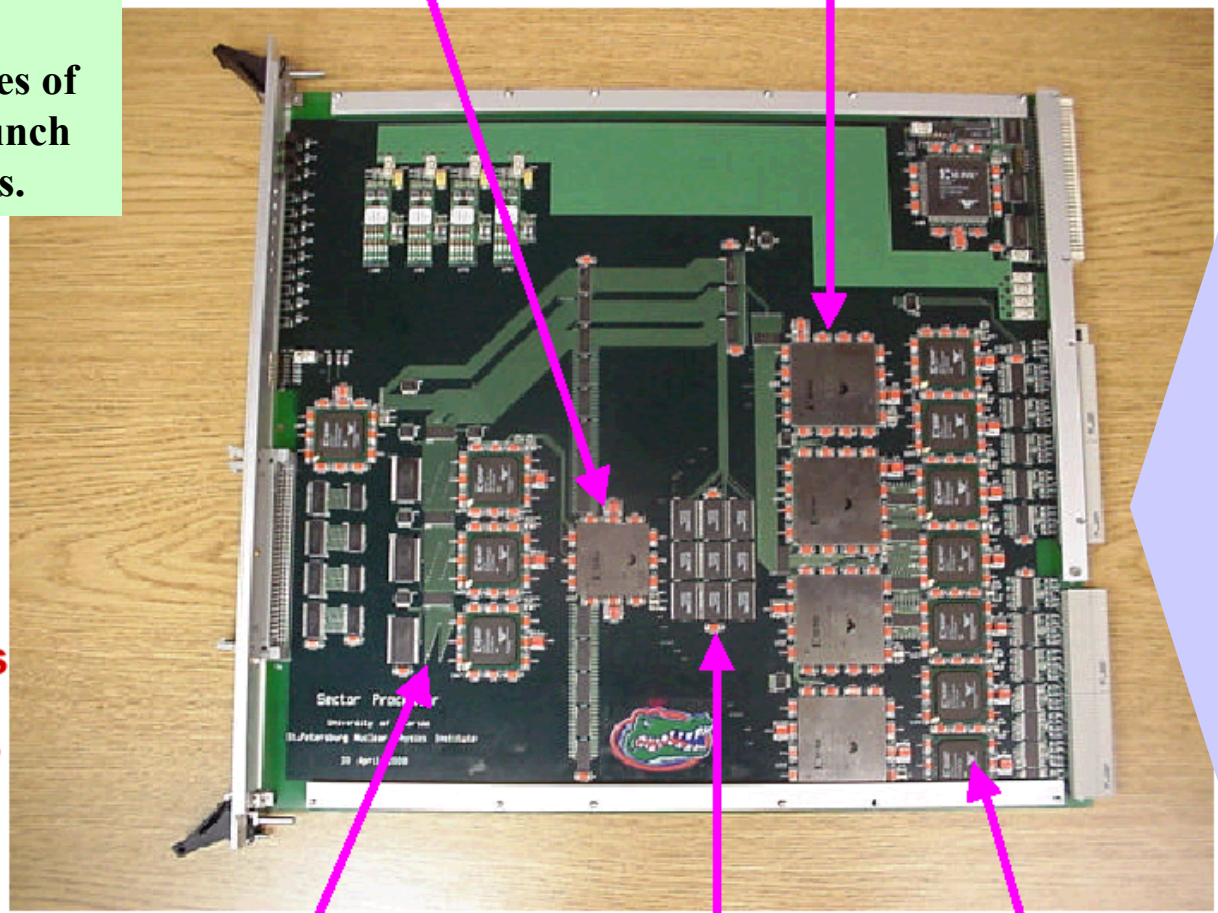
Res=22%

SP2000 Prototype Design

- **Performs 1 Billion Operations/Sec.**
- **Finishes analyses of data from p-p bunch collision in 375 ns.**

Final Selection Unit
XCV150BG352

Extrapolation Units
XCV400BG560



12 layers

10K vias

17 FPGAs

12 SRAMs

25 buffers

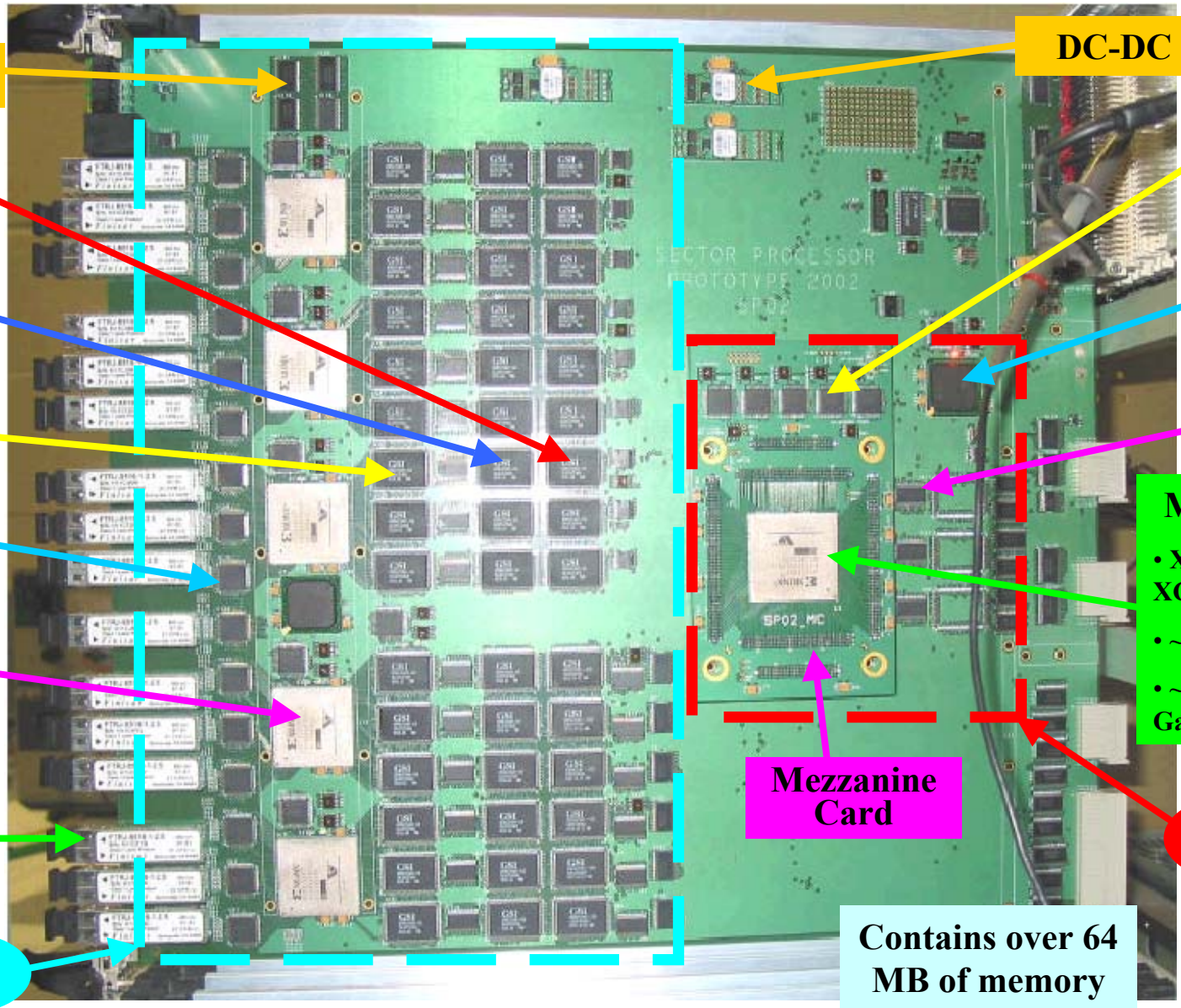
3GB/s from 3 Sector Receiver Cards

Assignment Units
XCV50BG256 &
2M x 8 SRAM

Track Assemblers
256k x 16 SRAM

Bunch Crossing Analyzer
XCV50BG256

SP2002: 3 SR's and 1 SP Merged onto 1 Board



EEPROM

Phi Global LUT

Eta Global LUT

Phi Local LUT

TLK2501 Transceiver

Front FPGA

Optical Transceiver

•15 x 1.6 Gbit/s Links

3 SRs

DC-DC Converter

EEPROM

VME/ CCB FPGA

PT LUT

Main FPGA

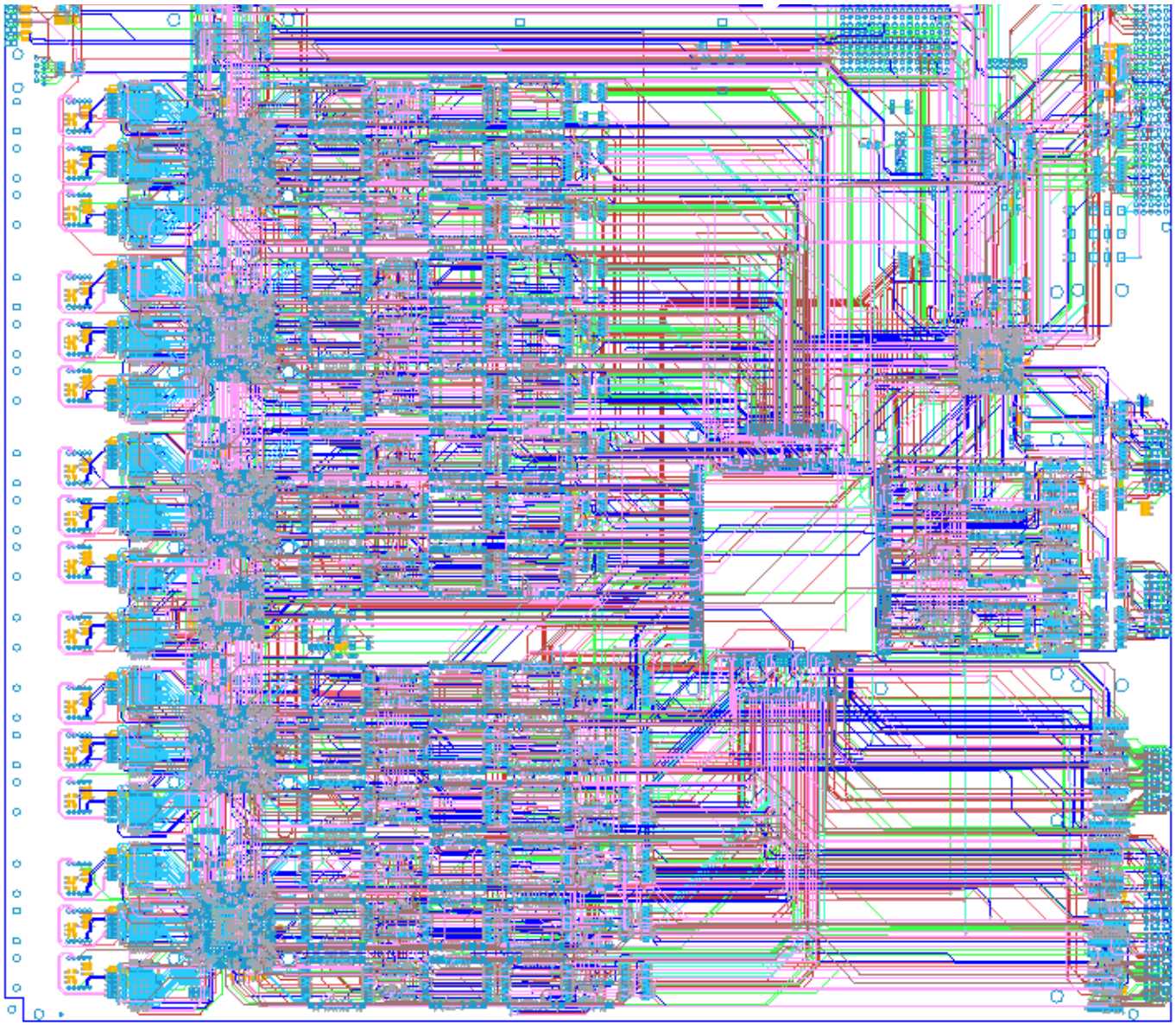
- Xilinx Virtex-2 XC2V4000
- ~800 User I/O
- ~4 Million Logic Gates

Mezzanine Card

SP

Contains over 64 MB of memory (51 SRAMs)

SP2002: 16 Layers



Verilog++

- SP logic became too complex to rely on schematic-based Firmware.
- A class library has been developed at UF that allows one to write both the simulation code and firmware in C++, and then translate this code into Verilog HDL. Thus, our code serves a dual purpose: when compiled one way we get a simulation, and when we compile the other way we get a Verilog output. This guarantees a bit-for-bit compatible simulation!
  - This Verilog code can then be synthesized by our FPGA vendor tools and is used as our SP Firmware. This allows us to verify the SP logic through C++ debugging tools such as MS Visual C++. We can also run this code as a part of the CMS simulation and reconstruction framework - thus allowing us to use usual analysis tools for verification (e.g. ROOT).
- We can thus maintain a line-by-line correspondence between simulation logic and Firmware logic. *Our current Firmware is to be used with a Xilinx Virtex-2 series FPGA.* Example of Verilog shown below:

C++:

```
always (negedge (vtckp))
begin
If(ConfigReg(0) == 1)
begin
   EastWaddr = 0;
   WestWaddr = 0;

end
```

Generated Verilog:

```
always @(negedge vtckp)
begin
   if (ConfigReg[0] == 1)
   begin
      EastWaddr = 0;
      WestWaddr = 0;
   end
```

Test Results and Future Plans

- **SP2000 was a Success**

Tests Completed:

- **Downloaded Firmware to FPGAs**
- **Validated VME Interface**
- **Validated on-board databus (common to Front FPGA)**

Plans:

- **Test Optical Link Connection to Peripheral Electronics.**
- **Test SR Memories**
- **Test SP Track-Finding Logic**
- **Cosmic Ray and Possibly Beam Test**

Conclusions

- We have successfully built and tested a prototype trigger which, utilizing 3-D track-finding algorithms, identifies muons in the CSC muon system of CMS, and reports their Pt and angular coordinates to the Global Muon Trigger.
- Receives 3 GB/s of input data and has an expected latency of 250 ns.
- SP2000 successfully tested
- SP2002 has been fabricated. Firmware is being finalized.
- SP2002 Tests well underway.