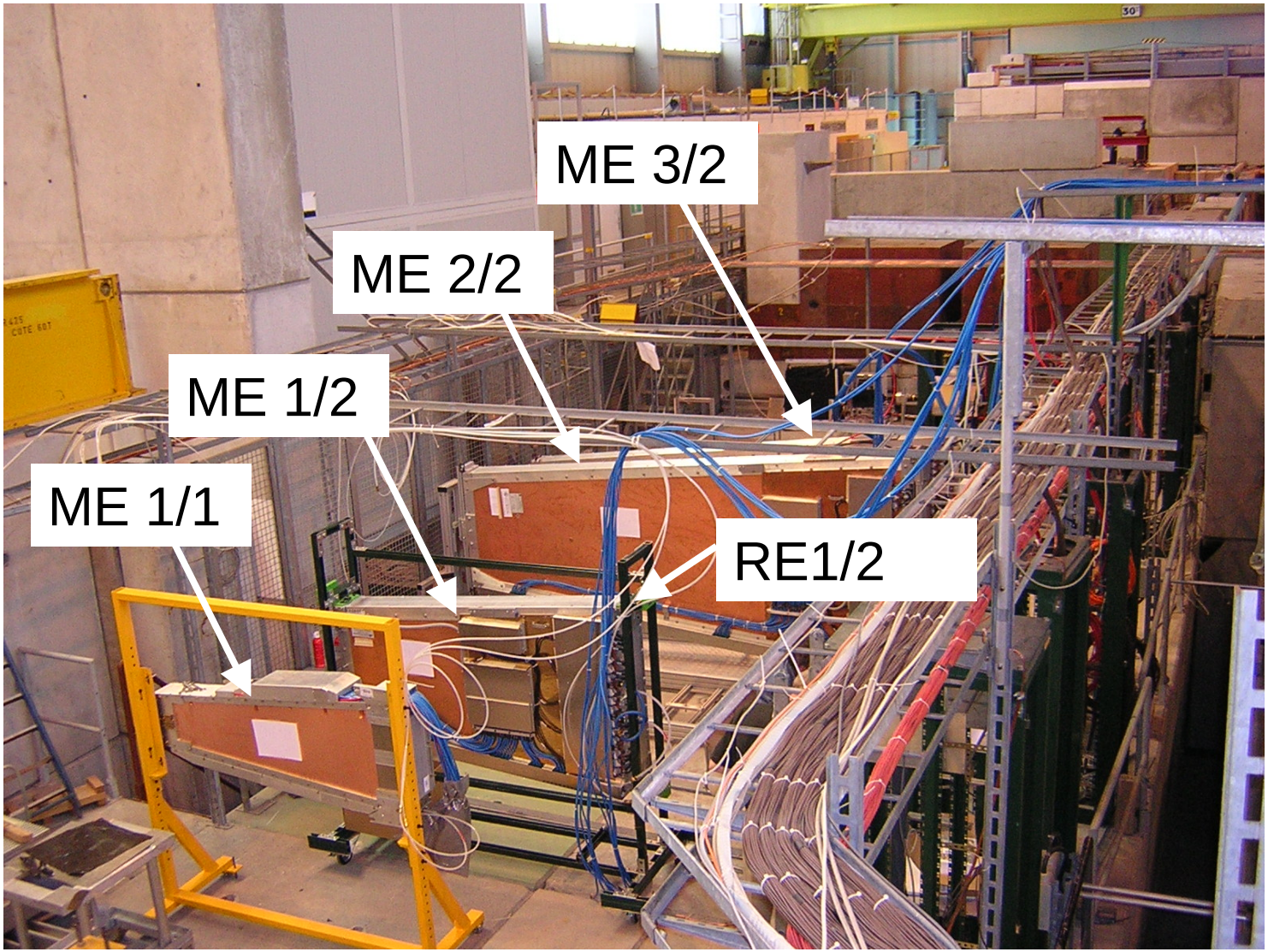
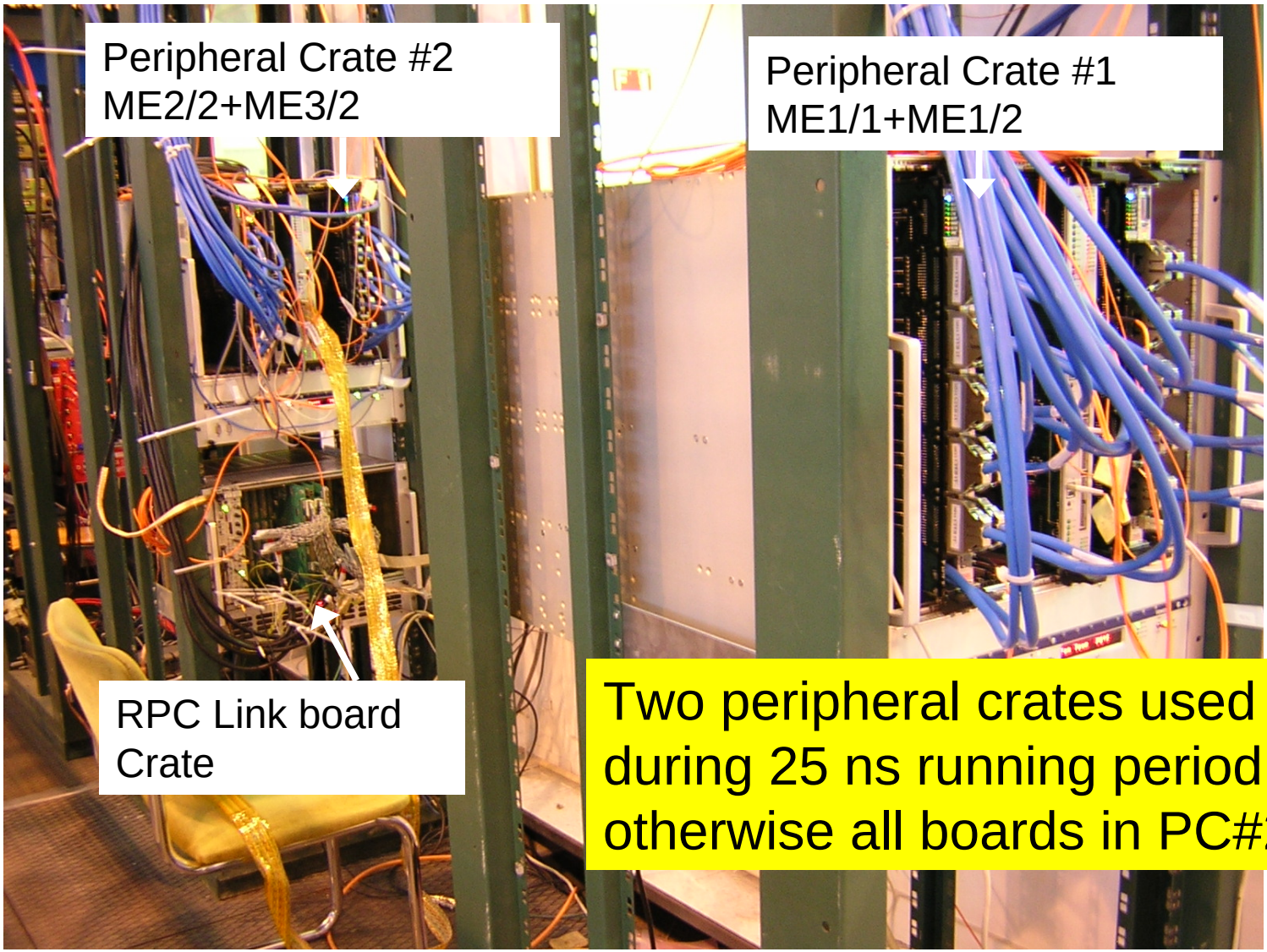
Track-Finder Test Beam Results

Darin Acosta

2004 CSC Beam Test (Muon Slice Test)



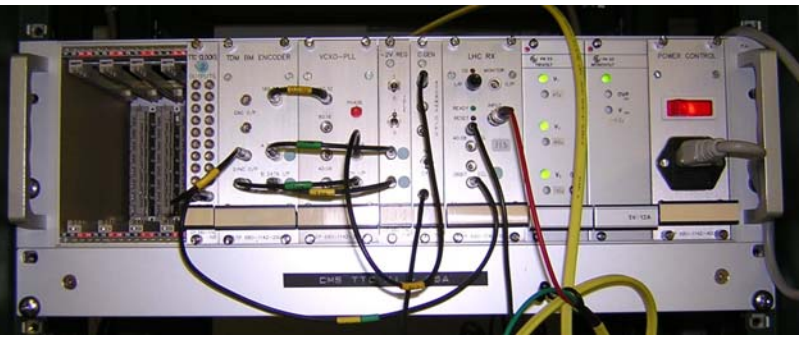
Peripheral Electronics Configuration



Two peripheral crates used only during 25 ns running period, otherwise all boards in PC#2

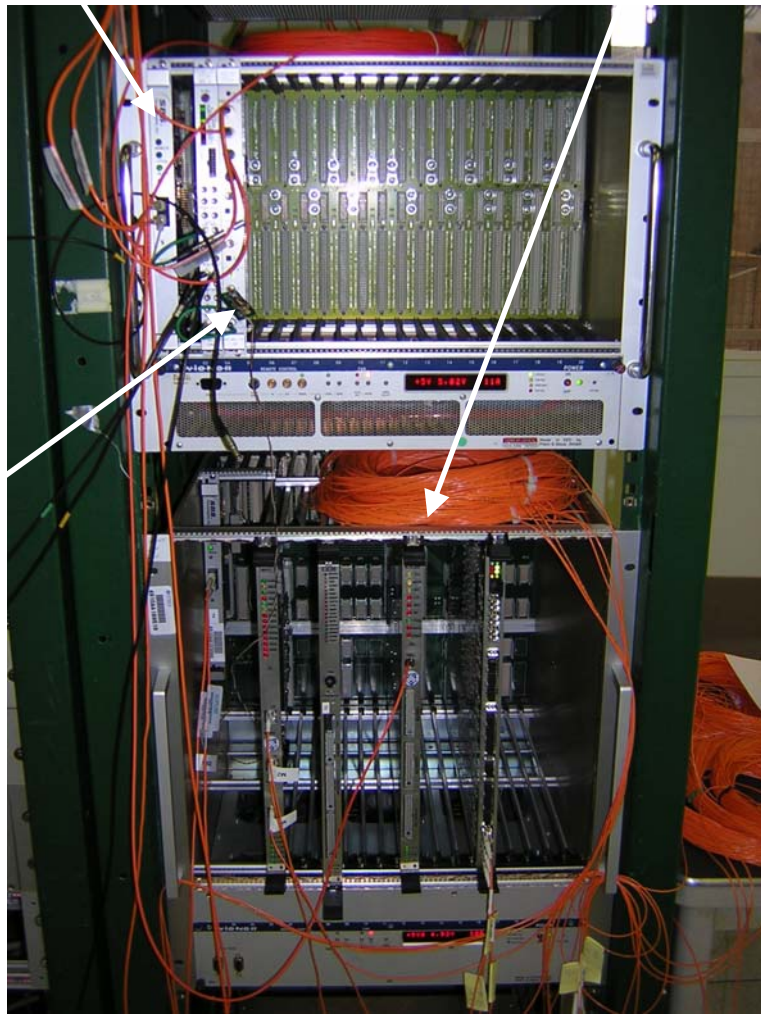
Track-Finder, TTC & Trigger Electronics

TTCmi crate
(machine interface for clock & orbit)



TTCvi crate

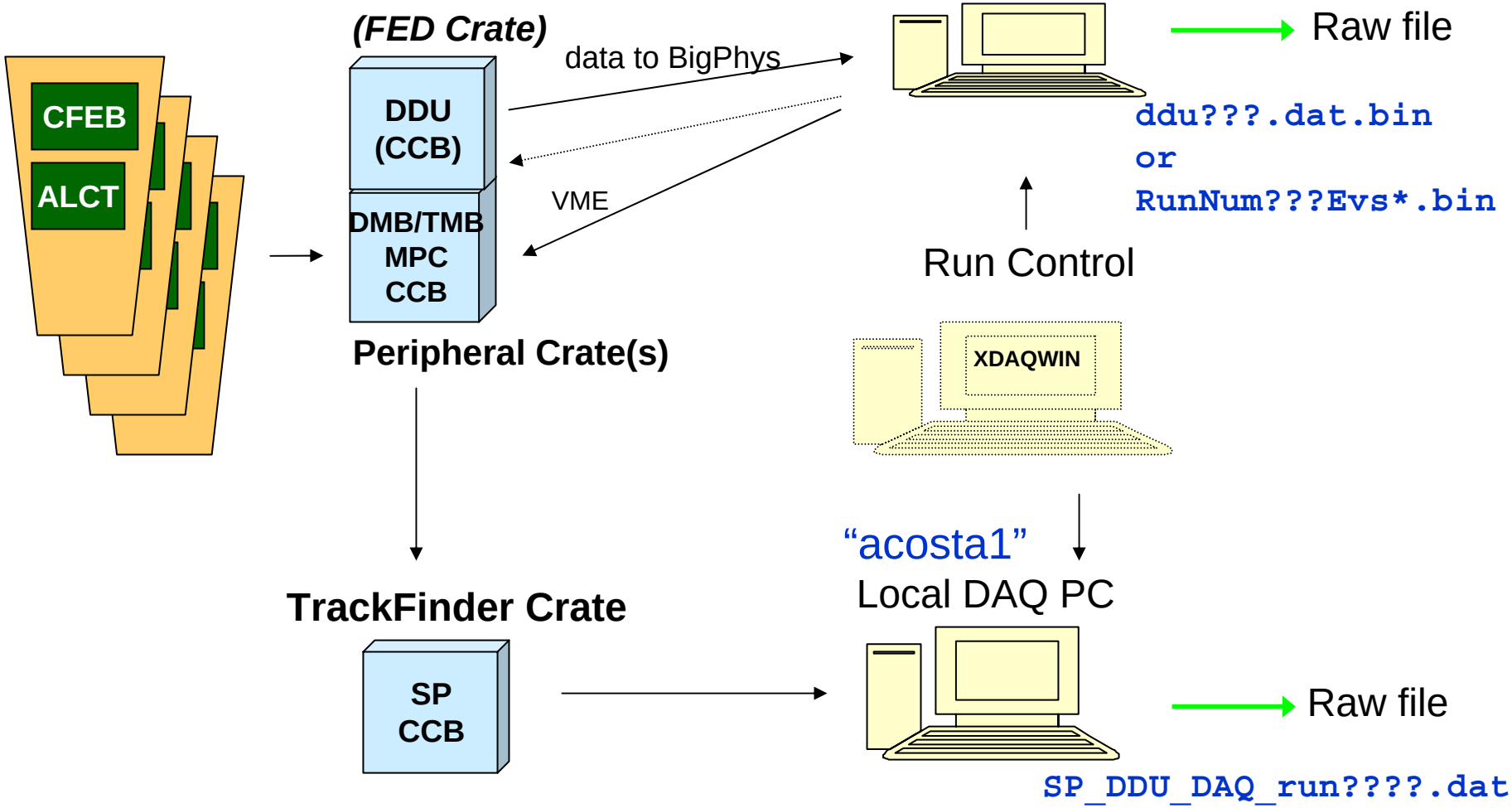
Level-1
Track-Finder crate



- **Machine clock and orbit signals only available during 25 ns run**
  - **We used Lev's XO for asynch period**
- **TTC configuration**
  - **Lindsey set up sending of spill start/stop signals in TTC asynchronous mode**
  - **Lev & Mike set up synchronous TTC signals partway through 25 ns period**

Test Beam 2004 DAQ Configuration

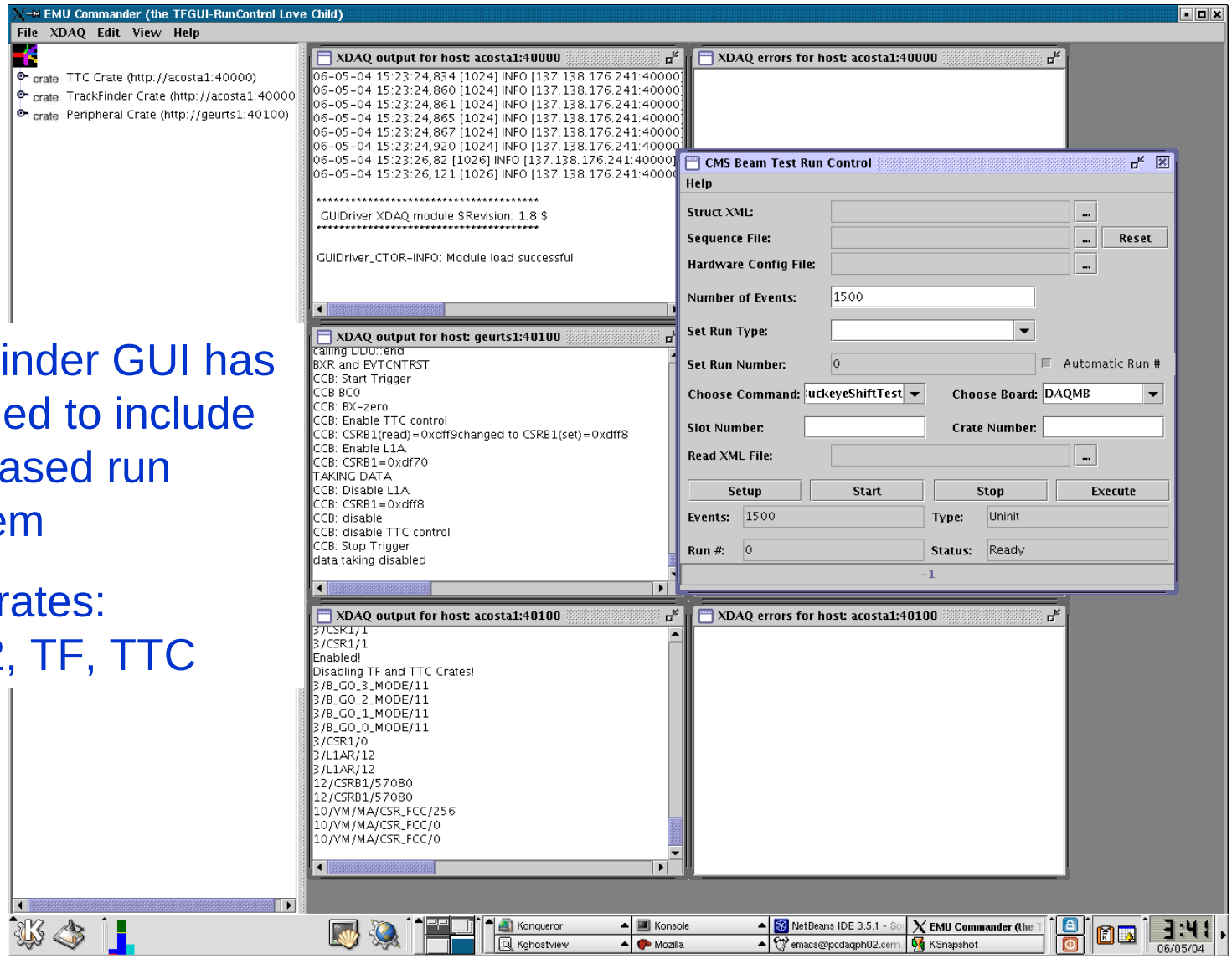
Configuration commands distributed via XDAQ.
Event-building tested



The Integrated EMU GUI

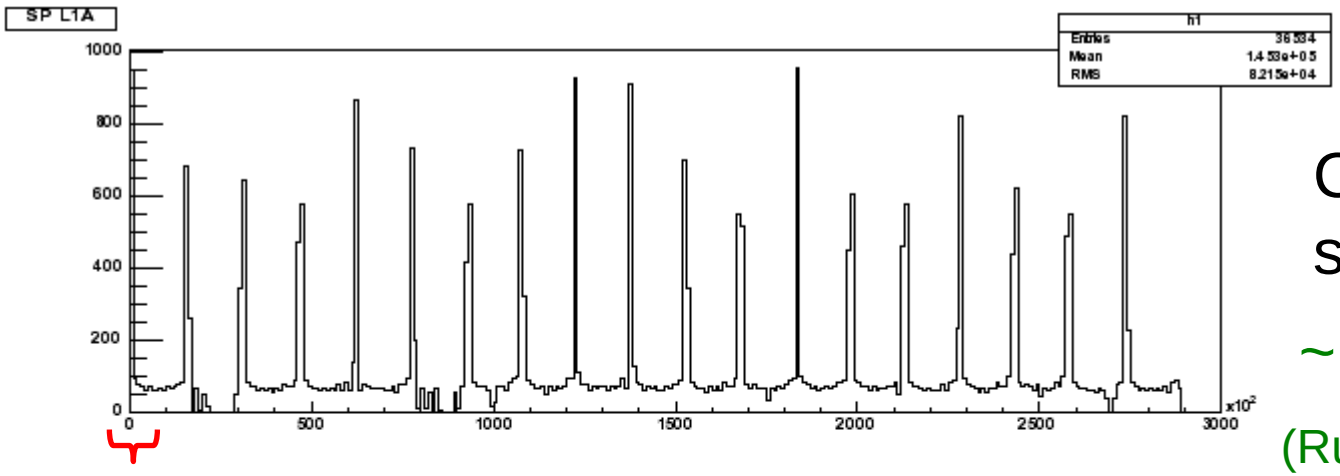
The Track-Finder GUI has been extended to include the XDAQ-based run control system

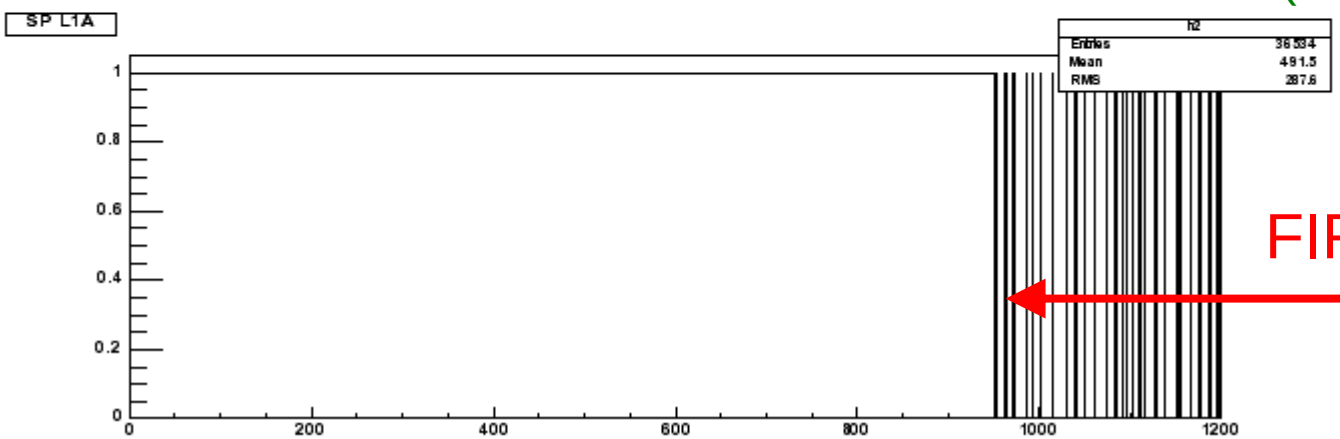
Controls 4 crates:
PC#1, PC#2, TF, TTC



SP DAQ

- **The Track-Finder DAQ FIFO fills up because of slow VME readout (but complete record @ start of each spill)**





Can count spills in run!

~10% caught

(Run 380, muons)

FIFO full

Full CSC Track-Finder DAQ Data Format

- **Full (i.e. final) DAQ output format of CSC TF specified**
  - **http://www.phys.ufl.edu/~acosta/cms/trigger.html**
- **CSC Track-Finder logs all input and output data for several BX around L1A (typically 7 bx)**
  - **Zero suppression capability (valid pattern)**
  - **Includes MS winner bits**
- **Implemented in firmware, and tested at beam test**
- **Data unpacking software written**
  - **"Puffs" into ORCA objects, but not yet installed into ORCA**

Table 4: SP02 DAQ Data Format

SP02 DAQ Data Format

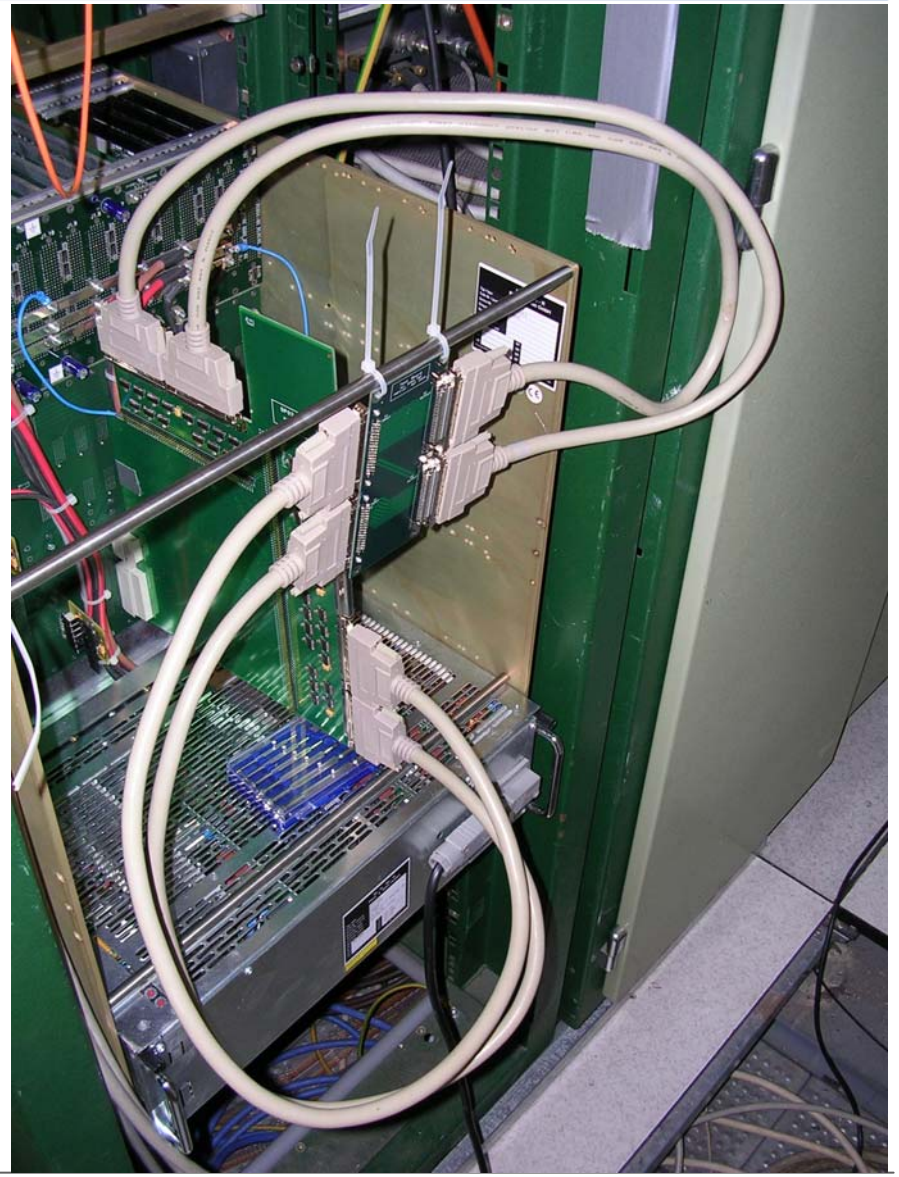
Data Word	Description	Comment for Zero Supression bit = 1	Data bits D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Event Header																		
HD0	Event Configuration Word	Always present	0xF				PT_LUT		ME Active	FRONT_FPGA Active					Zero Supr.	#_of_BX		
HD1	BC	Always present	0xF				Bunch Counter											
HD2	EC_LSB	Always present	0xF				Event Counter LSB											
HD3	EC_MSB	Always present	0xF				Event Counter MSB											
FRONT_Data_Block[1] for (BX = Bunch_Counter_Value)																		
FAB0	Muon Valid Pattern bits for Zero Suppression	if (#_of_BX) > 0 and at least one Active FRONT_FPGA	0	ME4C	ME4B	ME4A	ME3C	ME3B	ME3A	ME2C	ME2B	ME2A	ME1F	ME1E	ME1D	ME1C	ME1B	ME1A
FAB1	Synch Error bits (as they come from MPC)		0	ME4C	ME4B	ME4A	ME3C	ME3B	ME3A	ME2C	ME2B	ME2A	ME1F	ME1E	ME1D	ME1C	ME1B	ME1A
FAB2	track stub	if (#_of_BX) > 0, (F1_Active) = 1 and VP[ME1A] = 1	ME1A Frame 1 data															
FAB3	track stub		ME1A Frame 2 data															
FAB4	track stub	if (#_of_BX) > 0, (F1_Active) = 1 and VP[ME1B] = 1	ME1B Frame 1 data															
FAB5	track stub		ME1B Frame 2 data															
FAB6	track stub	if (#_of_BX) > 0, (F1_Active) = 1 and VP[ME1C] = 1	ME1C Frame 1 data															
FAB7	track stub		ME1C Frame 2 data															
FAB8	track stub	if (#_of_BX) > 0, (F2_Active) = 1 and VP[ME1D] = 1	ME1D Frame 1 data															
FAB9	track stub		ME1D Frame 2 data															
FAB10	track stub	if (#_of_BX) > 0, (F2_Active) = 1 and VP[ME1E] = 1	ME1E Frame 1 data															
FAB11	track stub		ME1E Frame 2 data															
FAB12	track stub	if (#_of_BX) > 0, (F2_Active) = 1 and VP[ME1F] = 1	ME1F Frame 1 data															
FAB13	track stub		ME1F Frame 2 data															
FAB14	track stub	if (#_of_BX) > 0, (F3_Active) = 1 and VP[ME2A] = 1	ME2A Frame 1 data															
FAB15	track stub		ME2A Frame 2 data															
FAB16	track stub	if (#_of_BX) > 0, (F3_Active) = 1 and VP[ME2B] = 1	ME2B Frame 1 data															
FAB17	track stub		ME2B Frame 2 data															
FAB18	track stub	if (#_of_BX) > 0, (F3_Active) = 1 and VP[ME2C] = 1	ME2C Frame 1 data															
FAB19	track stub		ME2C Frame 2 data															
FAB20	track stub	if (#_of_BX) > 0, (F4_Active) = 1 and VP[ME3A] = 1	ME3A Frame 1 data															
FAB21	track stub		ME3A Frame 2 data															
FAB22	track stub	if (#_of_BX) > 0, (F4_Active) = 1 and VP[ME3B] = 1	ME3B Frame 1 data															
FAB23	track stub		ME3B Frame 2 data															
FAB24	track stub	if (#_of_BX) > 0, (F4_Active) = 1 and VP[ME3C] = 1	ME3C Frame 1 data															
FAB25	track stub		ME3C Frame 2 data															
FAB26	track stub	if (#_of_BX) > 0, (F5_Active) = 1 and VP[ME4A] = 1	ME4A Frame 1 data															
FAB27	track stub		ME4A Frame 2 data															
FAB28	track stub	if (#_of_BX) > 0, (F5_Active) = 1 and VP[ME4B] = 1	ME4B Frame 1 data															
FAB29	track stub		ME4B Frame 2 data															
FAB30	track stub	if (#_of_BX) > 0, (F5_Active) = 1 and VP[ME4C] = 1	ME4C Frame 1 data															
FAB31	track stub		ME4C Frame 2 data															

SP_Data_Block[1] for (BX = Bunch_Counter_Value)

SPB0	Modified Synch Error bits (as SP gets it)	if (#_of_BX) > 0	0	ME4C	ME4B	ME4A	ME3C	ME3B	ME3A	ME2C	ME2B	ME2A	ME1F	ME1E	ME1D	ME1C	ME1B	ME1A
SPB1	MB non-zero Quality and Track Mode bits		0	0	MB1D	MB1A	MODE[3]				MODE[2]				MODE[1]			
SPB2	track stub	if (#_of_BX) > 0, (MB_Active) = 1 and Quality[MB1A] > 0	MB1A Frame 1 data															
SPB3	track stub		MB1A Frame 2 data															
SPB4	track stub	if (#_of_BX) > 0, (MB_Active) = 1 and Quality[MB1D] > 0	MB1D Frame 1 data															
SPB5	track stub		MB1D Frame 2 data															
SPB6	1st track data	if MODE[1] > 0	MS[1] Frame 1 data															
SPB7	1st track data		MS[1] Frame 2 data															
SPB8	1st track ids's		MS[1] Frame 3 data															
SPB8a	PT data	if MODE[1] > 0 and PT_LUT = 1	MS[1] Frame 4 Data															
SPB10	2nd track data	if MODE[2] > 0	MS[2] Frame 1 data															
SPB10	2nd track data		MS[2] Frame 2 data															
SPB11	2nd track ids's		MS[2] Frame 3 data															
SPB11a	PT data	if MODE[1] > 0 and PT_LUT = 2	MS[2] Frame 4 Data															
SPB12	3rd track data	if MODE[3] > 0	MS[3] Frame 1 data															
SPB13	3rd track data		MS[3] Frame 2 data															
SPB14	3rd track ids's		MS[3] Frame 3 data															
SPB14a	PT data	if MODE[1] > 0 and PT_LUT = 3	MS[3] Frame 4 data															
...																		
...																		
FRONT_Data_Block[#_of_BX] for (BX = Bunch_Counter_Value + #_of_BX - 1)																		
SP_Data_Block[#_of_BX] for (BX = Bunch_Counter_Value + #_of_BX - 1)																		

DT/CSC Transition Card Test

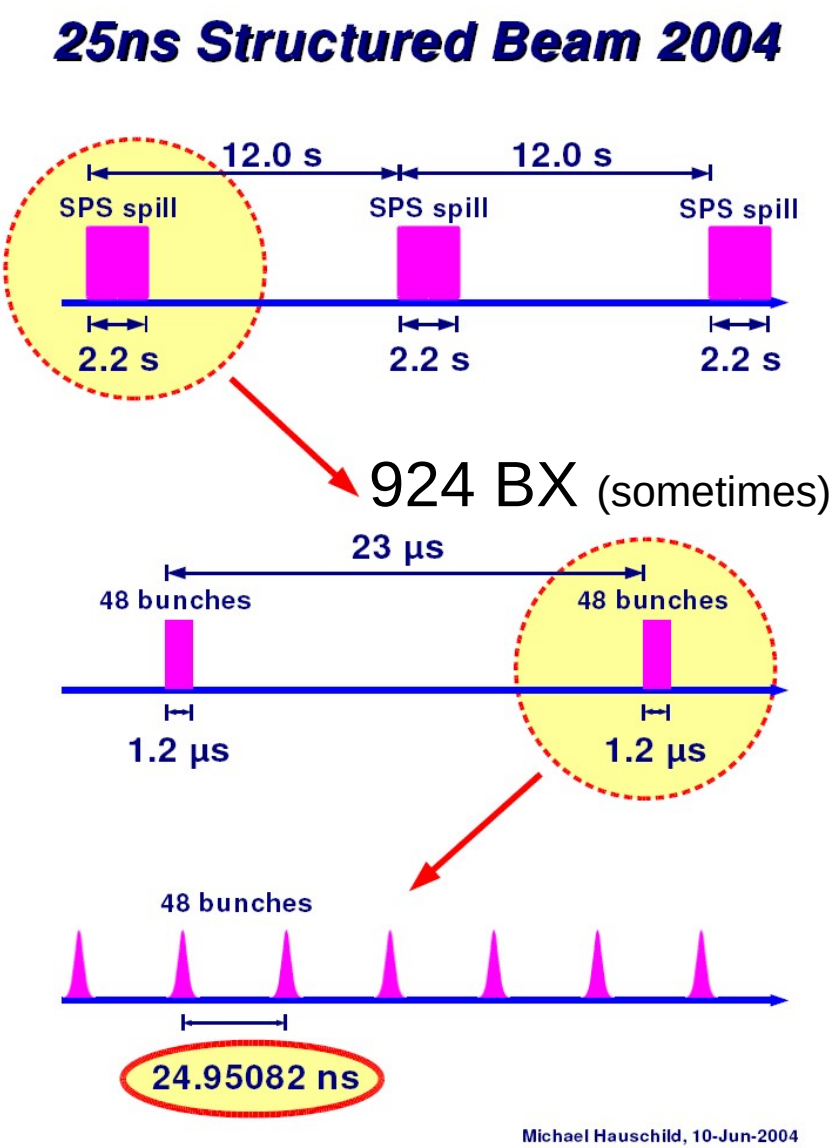
- **While we were waiting for beam to start at CERN, we managed to test a new DT/CSC transition card for the Track-Finder**
  - **New design solves connector space problem**
  - **Tester board allows loopback test without DT Track-Finder**
  - **Data pumped from input FIFO to output FIFO on SP**
- **Data test succeeded, except for 1 broken backplane pin**
- **Next step:**
  - **Second integration test with DT TF (Oct.'04 or later)**



Configuration During Asynch Period

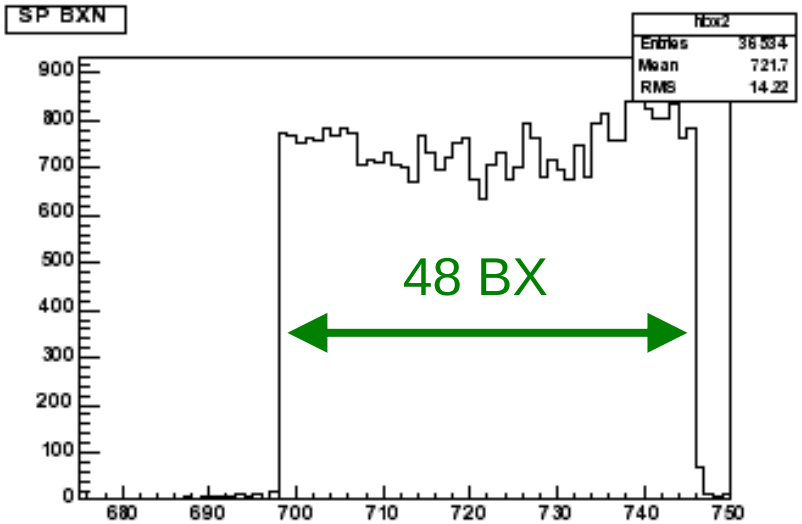
- **Single peripheral crate configuration for all four TMB's + DMB's (+ DDU)**
- **CCB2004 in FPGA mode**
- **Scintillator-based L1A**
- **Muon beam only**
- **Most runs were ALCT studies varying chamber angles and ALCT parameters**
  - **Early runs recorded only by Track-Finder**

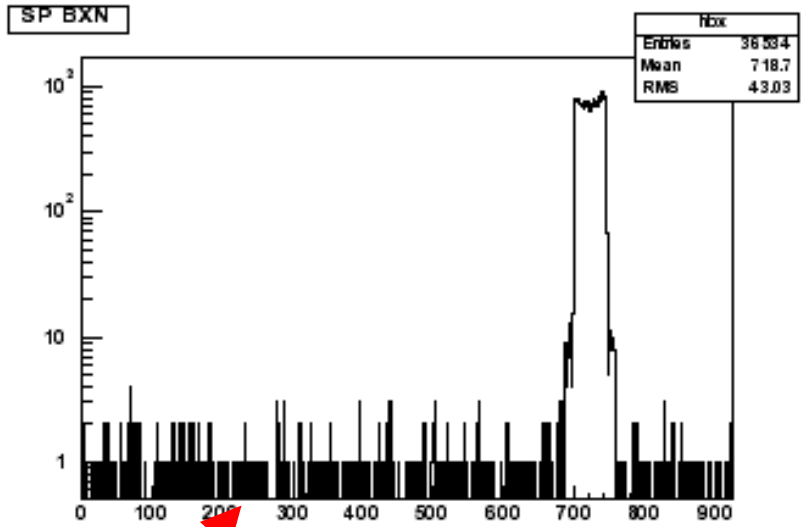
25 ns Structured Beam

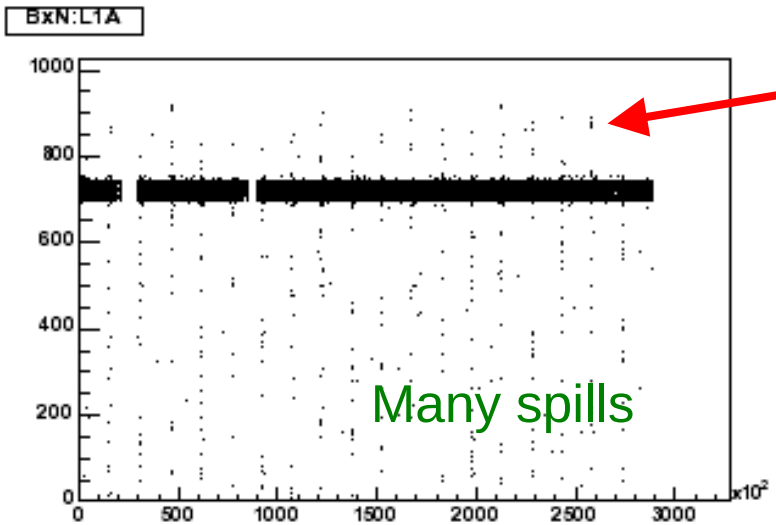


- **LHC-like bunch structure during synchronous running**
- **Trigger rates at X5A during spill**
  - **Muons: 3–10 kHz**
  - **Pions: >100 kHz**
- **CSC readout system is designed for a L1A*LCT rate at LHC design luminosity of order 5 kHz**

Sector Processor BX Distribution







Some random triggers, mostly @ spill start

- **BX counter blindly resets every time BC0 arrives**
- **See Lev's talk for details**

Run 380, muons

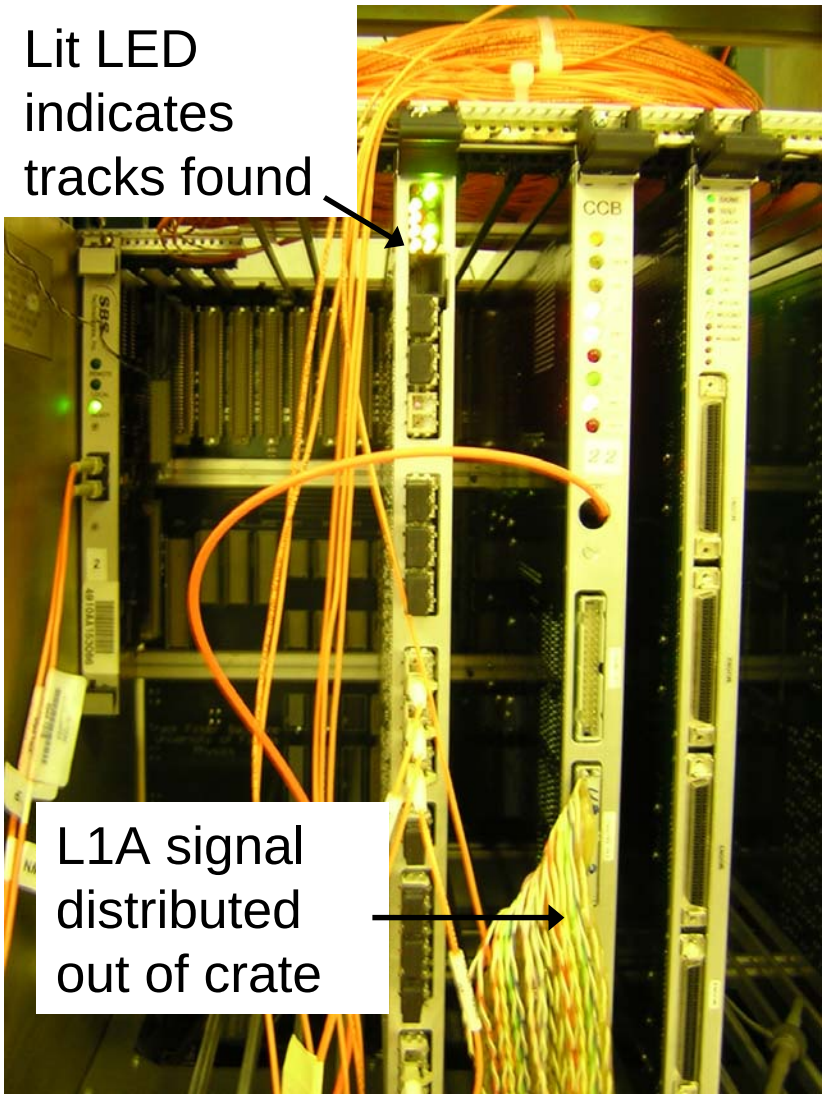
Configuration During 25 ns Period

- **Went to 2 Peripheral Crate setup**
  - **PC #1: ME1/1 + ME1/2 (with RAT)**
  - **PC #2: ME2/2 + ME3/2**
- **TMB logic updated ⇒ New data format!**
  - **Accommodates RPC data, fixes stale data bug**
  - **Breaks RootEventDisplay?**
- **Went to discrete logic mode on CCB (runs > 293)**
  - **No programmable L1A delay (done in CCB2001 for TF L1A)**
- **Went to Track-Finder trigger (runs > 291)**

Track-Finder Trigger

- **Aligned chambers in SR LUTs, but some features:**
  - **Same LUTs used for all links**
    - **CSC id was used to determine appropriate offset to apply**
  - **Could not use ORCA tables, because TMB quality codes from hardware do not match ORCA!**
  - **Set ϕ to be strip id (lose some precision)**
    - **Did not correct di-strip patterns (factor 4 discrepancy), nor scaled strip/WG size to global coordinate system**
- **Generally triggered on ME2/2 and ME3/2**
  - **Various cable mappings vary ME1-ME2-ME3-ME4 order**
  - **Accidentally had η offset in ME1**
  - **Can trigger on 1 chamber with ghost segment on second link**
- **Never tried "transparent" mode of MPC (routing of specific MPC inputs to MPC outputs)**
- **Sensitive to entire beam profile $\otimes$ CSC coverage:**
  - **Muon trigger rate increases from ~6500/spill to ~17000/spill**
  - **Pion trigger rate decreases from 240K/spill to 175K/spill (effect of η offset problem?)**

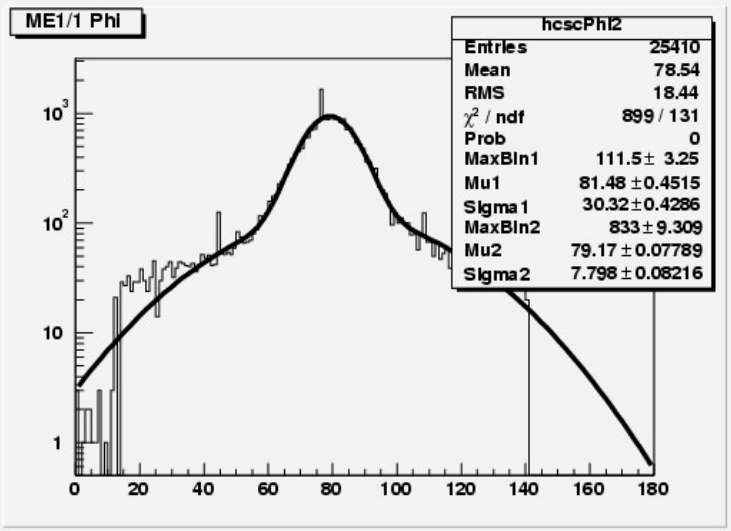
Track-Finder Tests

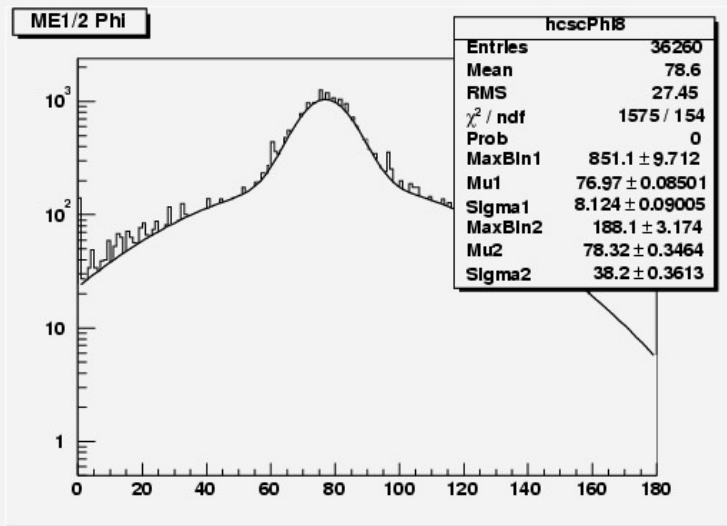


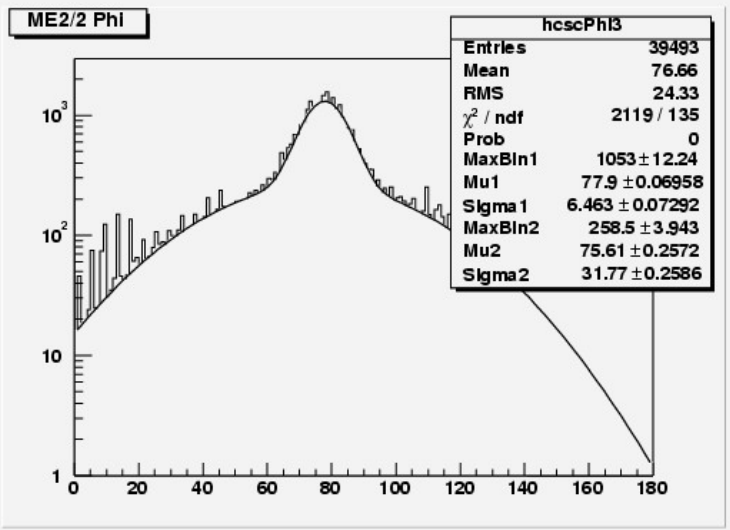
- First time we tested with full Track-Finding logic to identify tracks in data
- Full DAQ logging of inputs and outputs for offline comparisons
  - Can compare with data sent by Peripheral Crates as well as internal TF logic
- L1A generation a major synchronization accomplishment for trigger
  - Data must be aligned spatially and temporally
  - Very useful for slice tests

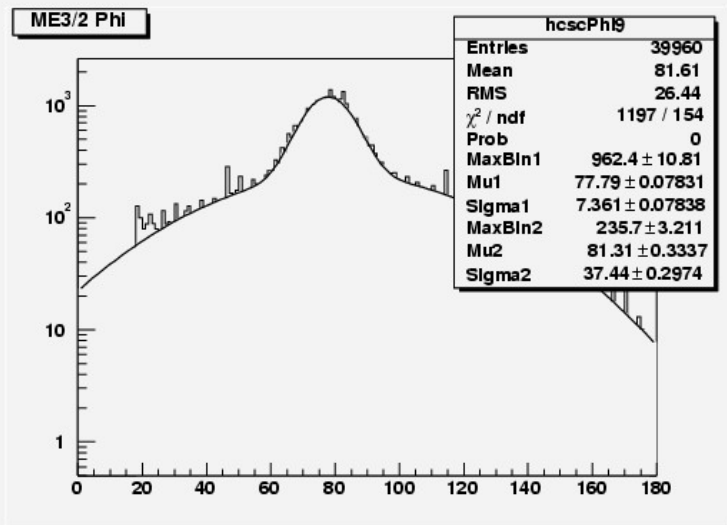
Spatial Alignment in Phi of TF Data

Run 380





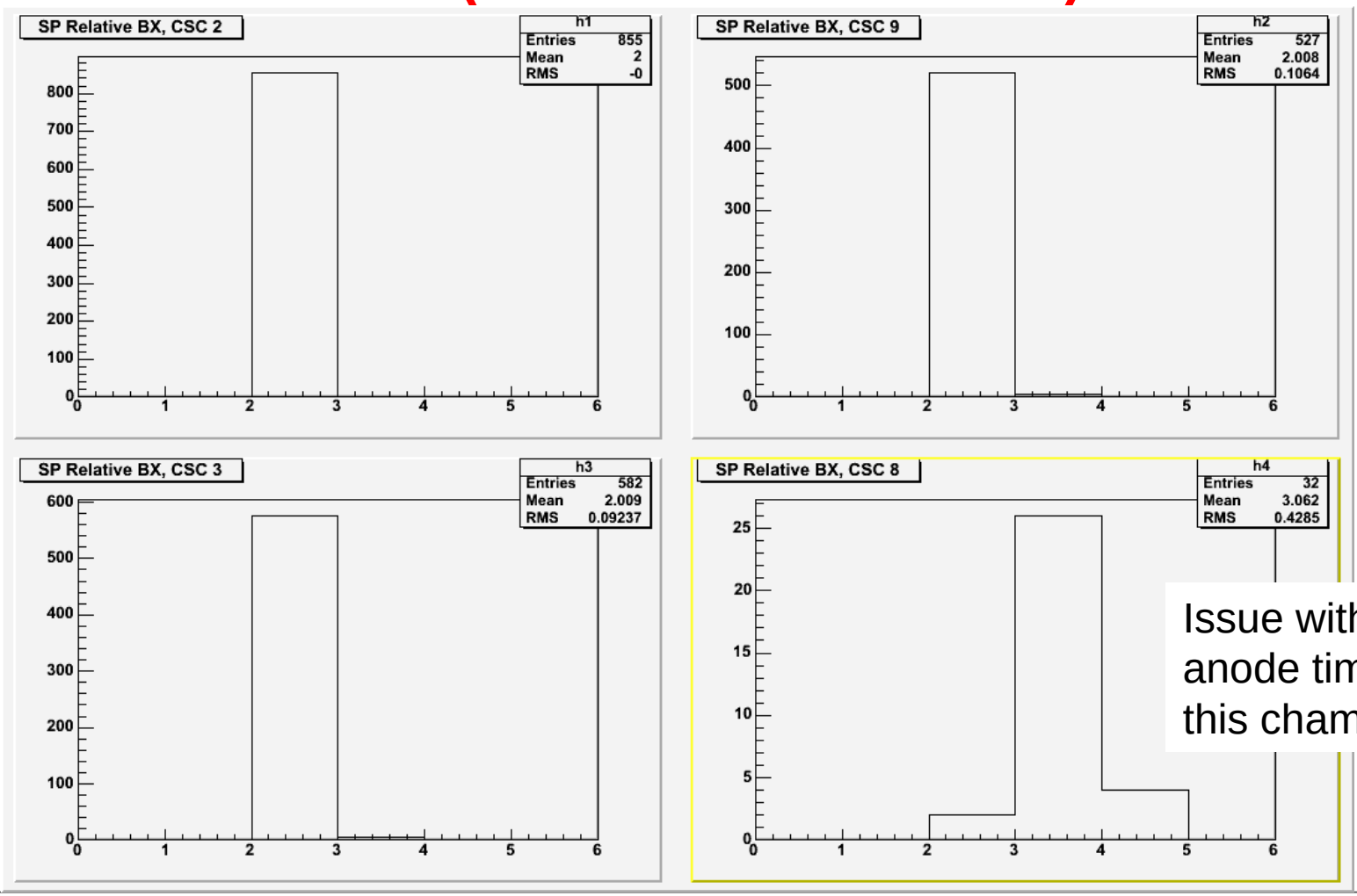




½-strip units. Need to convert to global coordinate system

Time Alignment of CSC data in Track-Finder

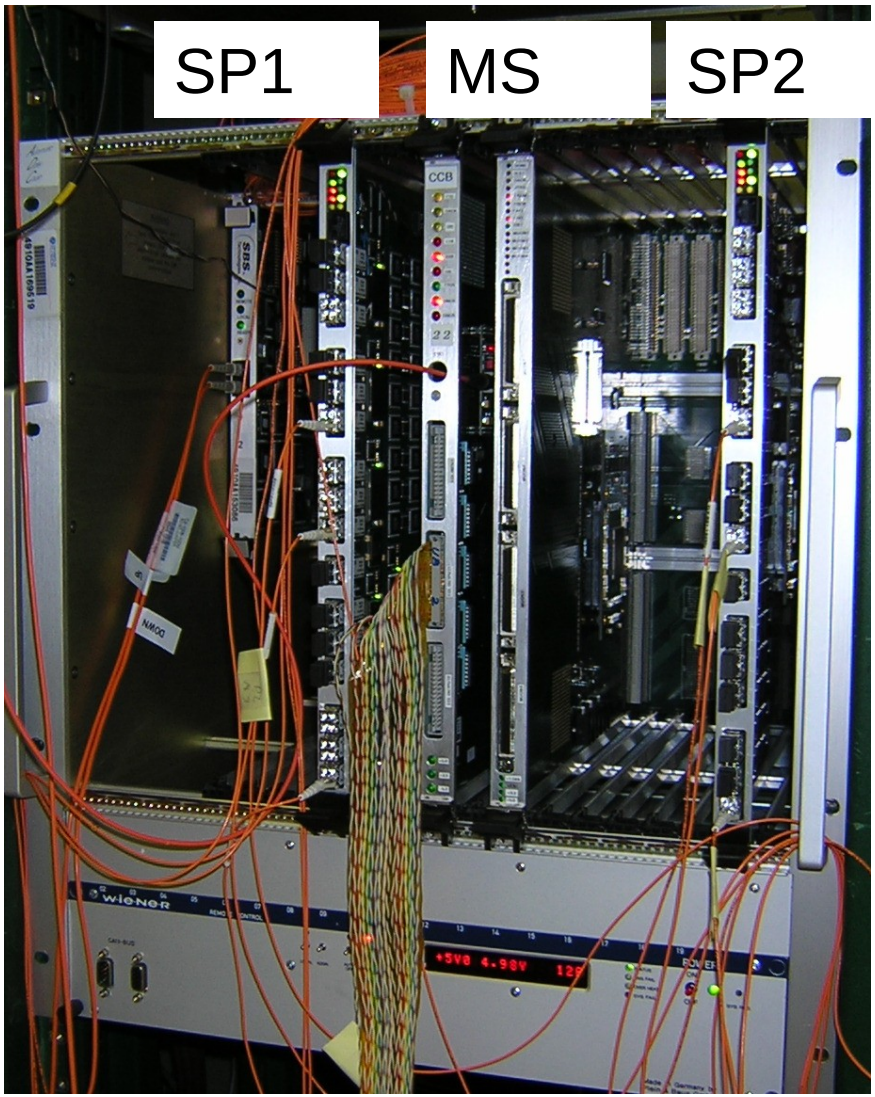
- **Able to get all trigger data from multiple chambers and crates on same BX (at least for some runs):**



Issue with anode timing for this chamber

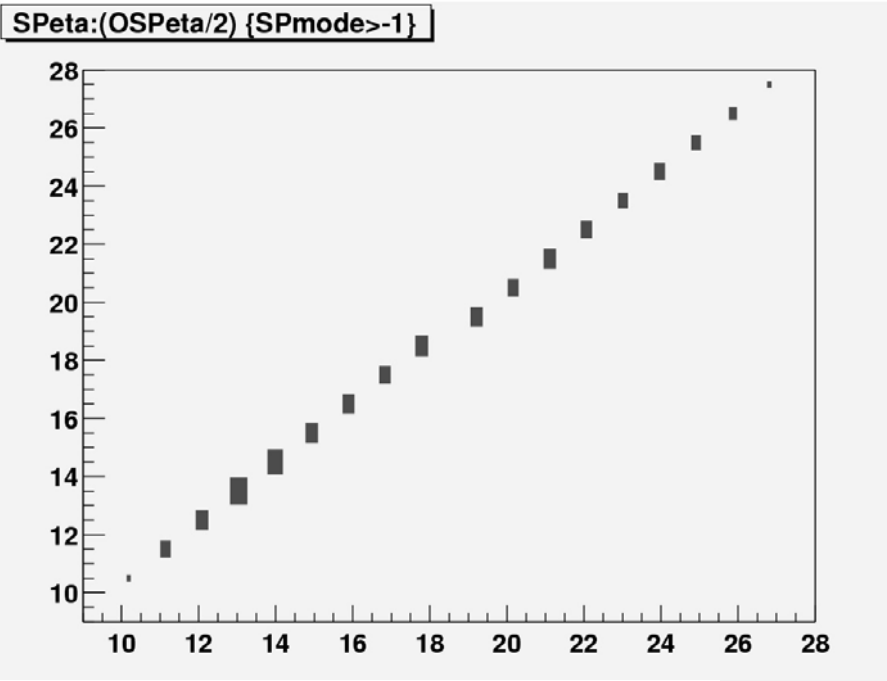
Run 293

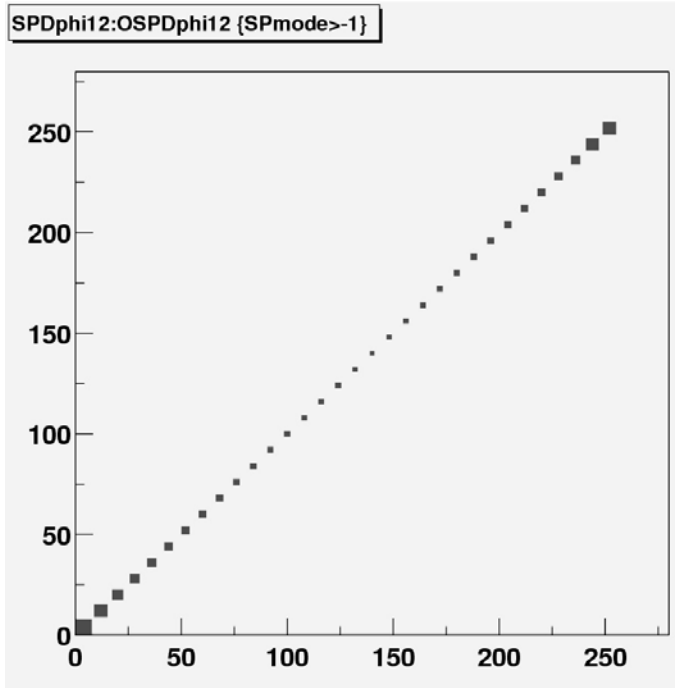
Track-Finder Crate Tests Cont'd



- First test of multiple peripheral crates to TF crate
  - Synchronization test
- Various clocking solutions tried to test robustness of optical links
  - MPC used QPLL 80 MHz clock on backplane for all 25 ns runs
- First test of multiple Sector Processors to one Muon Sorter
  - Detailed offline checks of exchanged data should follow to validate boards

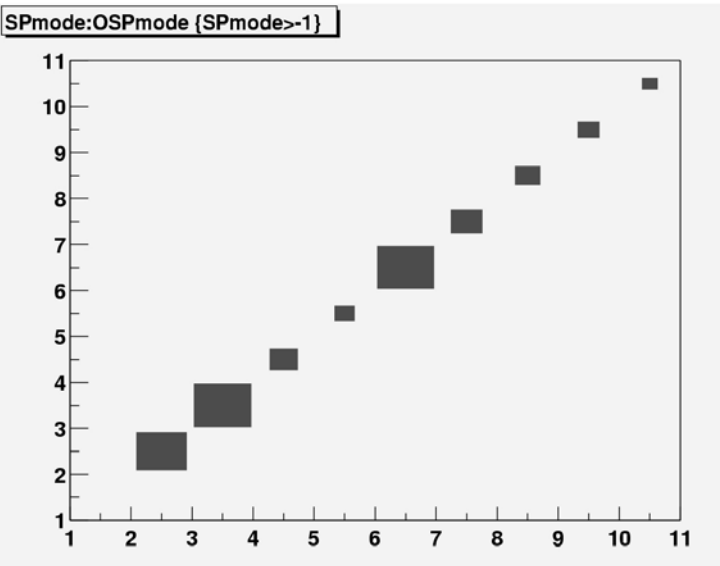
SP: ORCA vs. Hardware Check





Run 366, Scurlock

64K events



- **Correlation of track η, $\Delta\phi$ between 2 stations, and track type agrees perfectly between hardware and ORCA simulation**

Further SP Functionality Checks

- REU student Nick Park ran on additional runs to check the agreement between simulation and hardware
- Again perfect agreement:
  - Run 379: 14K
  - Run 380: 36K
  - Run 381: 32K
- So in total, ~150K events checked

TMB→ MPC → SP Check

- **In order to directly check the integrity of the data transmission between MPC and SP optical links, compare the TMB data logged through the DDU with that recorded by the SP**
  - **Note: no link errors were observed on the error counters during beam test when we were checking**
- **Procedure:**
  - **Open both DDU and SP data files, scroll until L1A match**
  - **Assign a relative BX to each LCT recorded by the TMB by using the difference between the ALCT 5-bit BX (BX when LCT was found) and the ALCT 12-bit BX % 32 (BX corresponding to L1A)**
  - **Run this train of BX through the MPC simulation to get the MPC LCT results for each BX**
  - **Compare with SP data for a train of 7 BX**
- **Question: how best to assign BX without ALCT data?**

MPC → SP Results

- Asynchronous period, muon runs, ME2/2 + ME3/2 only
- Run 169
  - 5 mismatches in 3987 events (0.1%) (then unpacking software crashes)
    - Mostly TMB ME3/2 data missing (often 4-5 BX early)
- Run 170
  - 15 mismatches in 12052 events (0.1%)
    - Mostly TMB ME3/2 data missing (often 4-5 BX early)
- Run 168
  - 1.5% mismatches
- Runs 171, 172, 173,…
  - 2.2% mismatches
    - Missing ME2/2 and ME3/2 TMB data
- Adding in ME1/2:
  - 16–19% mismatches (mostly missing ALCT data)

MPC → SP Results

- **Synchronous period, muon runs, ME2/2 + ME3/2 only**
  - **Recall that we switched to QPLL 80 MHz backplane clock on MPC**
- **Run 368**
  - **4 mismatches in 1102 events (0.4%)** **(then unpacking software crashes)**
- **Run 369**
  - **13 mismatches in 1715 events (0.8%)** **(then unpacking software crashes)**
- **Run 374**
  - **290 mismatches in 20000 (1.5%)**

- **Most mismatches due to bit flips on ME3/2 data**
- **Comparing only ME2/2 data yields mismatch rate of ~0.3%**

➔ Of these, most cases are when SP is missing data

Conclusions on Mismatches

- **ME3/2 mismatches are probably NOT due to link errors**
  - **For the synchronous runs runs, most mismatches due to bit flips on ME3/2 data (e.g. 9244 → 924c).**
    - **Why just ME3/2 singled out when MPC sorts data and rearranges LCT to link mapping?**
    - **50% of the time it is the same bit, so how can that happen for random errors on a serial link?**
  - **Some bit flips occur on events with two LCTs/chamber**
    - **In separate studies, these are usually not real di-muons, but rather ghost segments with identical strip id**
    - **The SP data showed strip equality, TMB did not**

- **Likely to be an issue with DAQ path for TMB**

MPC Validation

- Can check MPC winner bits recorded by TMB in DDU data with that expected by MPC simulation (all TMBs)
- Use same code developed for TMB→MPC→SP check to place LCTs on correct BX
  - Run 168: 193 mismatches in 79408 events (0.25%)
  - Run 169: 129 mismatches in 58139 events (0.22%)
    - TMB1: 63
    - TMB3: 51
    - TMB8: 15
  - Run 170: 141 mismatches in 65227 events (0.22%)
    - TMB1: 69
    - TMB3: 53
    - TMB8: 19
  - Run 374: 66 mismatches in 31872 events (0.21%)
- Most mismatches are due to BX mis-assignment
  - HW winner bits agree with data recorded by SP

MS → SP Tests

- Muon Sorter installed during synchronous period
- For runs ≥372, should be reporting winner bits
  - Interesting side effect is that if one SP in the crate does not have Pt LUT loaded, prevents correct winner bits to be reported to another SP
- Check of run 380, 11775 events, SP as trigger
  - Track 0 winner bit: set for all but 1 event
    - An event where 2 muons were found, each on a different BX (verified by simulation)
    - MS id bits = 1 for first one, =2 for second (even though it is first on the output links)
  - Track 1 winner bit: set whenever 2 muons found (20 events)
  - No occurrences of 3 track events
    - Hard to get 3 tracks in one BX, given just 2 LCTs/chamber

Sector Processor Conclusions

- Fully operational SP tested with full data format
- Agreement between the recorded TMB data and SP data can be at the level of 99.7%, but worse for some chambers and runs
  - Same level of agreement as obtained from the Sep.'03 beam test
- Agreement between the output of the SP with a simulation based on the logged inputs is 100%
- The SP in conjunction with a specially modified CCB was able to self-trigger the experiment (including RPC)
- Require updated SR LUTs from ORCA to match the actual TMB quality codes from hardware
- Muon Sorter winner bits appear to be properly recorded
- New DT/CSC transition card works

General Conclusions

- **Lots of details should be fixed for next time around**
  - **Get TMB quality codes to match in ORCA**
  - **Derive appropriate LUTs from ORCA to get full precision and appropriate scaling from one chamber to next**
  - **Clean up configuration (remove η offset)**
  - **Use "MPC Transparent" mode**
  - **Possibly place TF trigger in "OR" with scintillator**
- **Logging of TMB data should be checked.**
  - **Seem to have data corruption problems that prevent 100% agreement with SP. Depends on TMB and run number. Timing issue?**
- **Logging of data through DDU, and unpacking software, ran into various problems**