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A PROTOTYPE TRACK-FINDING PROCESSOR FOR THE LEVEL-1 TRIGGER OF THE CMS ENDCAP MUON SYSTEM

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We report on the development and performance of a novel track-finding processor for the Level-1 trigger of the CMS endcap muon system. The processor links track segments identified in the cathode-strip chambers of the endcap muon system into complete three-dimensional tracks. It then measures the momentum of the best track candidates from the sagitta measured between three muon chambers in the endcap fringe field. The processor is pipelined at 40 MHz, and has an overall latency of 400 ns. The logic for the prototype is implemented in high-density FPGAs and SRAM memory. It receives approximately 3 gigabytes of data every second from a custom backplane operating at 280 MHz. Test results of the prototype are consistent with expectation.

1. CSC Level-1 Trigger and Track-Finding Architecture

This paper reports on the development and performance of a track-finding processor for the Level-1 trigger of the CMS (Compact Muon Solenoid) endcap muon system.[1] The endcap muon system consists of four stations at each end of the CMS detector. Each station is composed of Cathode Strip Chambers (CSC) of trapezoidal shape arranged to form a disk.[2] The trigger region of the CSC Level-1 Trigger is divided into 60° sectors in azimuth for both endcaps (a total of twelve sectors). Each sector covers the pseudo-rapidity region $0.9 < \eta < 2.4$. Track-finding in each sector is performed by a Sector Processor (SP), which is a 9U VME card housed in a crate in the counting house. The pattern of charge deposition in the six layers of the CSC chambers by a traversing charged particle are identified by the front end electronics boards to form track segments.[3] The information of the track segments in a sector are collected by several boards and ultimately received by a SP at a rate of 3 GB/s through a custom backplane which operates at 280 MHz. The SP performs three-dimensional track-finding by matching the track segments in both ϕ and η. It measures the track parameters of the three best muons and transmits the results to a sorting processor. The sorting processor selects the four best muons out of the 36 muon candidates send by the twelve SPs, and reports them to the Level-1 Global Muon Trigger.

The goal of the CSC Track-Finder is to identify muon candidates efficiently at

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as low a P_T threshold as possible, and yet to keep the single muon rate down at the level < 1 kHz per unit rapidity at the full LHC (Large Hardon Collider) luminosity. The logic of the track-finding algorithm should also be programmable so that the experiment can adapt to different background conditions and collision rates.

2. Sector Processor

The block diagram of the SP is shown on the left of Figure 1. The main components on this card are Bunch Crossing Analyzer (BXA), Extrapolation Unit (EU), Track Assembler Unit (TAU), Final Selection Unit (FSU), and Assignment Unit (AU). The data received by the SP from the custom backplane are deserialized and synchronized with the local clock. These data are then processed by the units mentioned above at a rate of 40 MHz. Most of the logics are implemented in Field Programmable Gate Arrays (FPGAs) and Random Access Memory (RAM). The overall latency of this prototype SP is 400 ns.

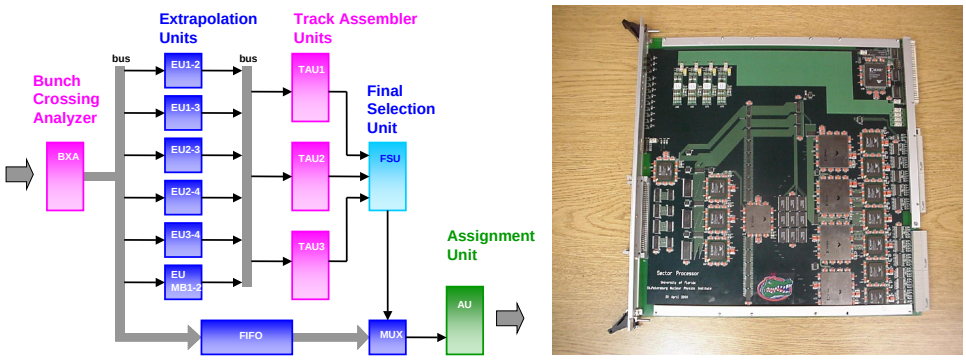

Fig. 1. Left figure: Block diagram of the logic for one Sector Processor of the Track-Finder. Right figure: Photograph of the Sector Processor prototype.

The data of the track segments received by the SP is accumulated by the BXA for a couple of bunch crossings. This enables the SP to analyze track segments received in different bunch crossings caused by the intrinsic timing spread of the track segment formation. An EU links track segments in two CSC stations in three dimensions by performing tests to check if the track segments are compatible with a muon coming from the nominal collision point with a curvature that is consistent with the bending induced by the magnetic field. To minimize the latency in the SP, all individual extrapolations are performed in parallel. These require a total of 87 EUs implemented in four Xilinx XCV400BG560 Virtex FPGAs.[4] About 100 billion operations are performed in the EUs per second.

The results from the EUs are examined by the TAU to determine if any of the track segment pairs come from the same muon track. Nine link units, which are static RAM memories, are implemented to use the extrapolation results to assemble the best track patterns. The qualities of the assembled tracks and the indices of the track segments used in making the track are sent to the FSU. The nine tracks

assembled by the TAU are examined by FSU to cancel redundant tracks and to select the three best distinct tracks. The FSU first compares the qualities of these tracks and the indices of the track segments that form these tracks. The comparison results are used to determine if some of the tracks are from a single muon, based on whether the number of common track segments exceed a preset threshold. Finally, three best distinct tracks are identified and are reported to the AU.

The last task of the Track-Finder, which is executed in the AU, is to measure the track parameters of the three muon candidates selected by the FSU. These parameters include the ϕ and η coordinates of the muon, P_T, sign and the overall quality of the track. The P_T is determined from the sagitta measured between two or three stations in the endcap fringe field. Simulation results show that for low P_T tracks, the accuracy in the P_T measurement is $\sim 30\%$ from two-station measurement, and with the first station (station closest to the nominal collision point) included. However this accuracy can be improved to $\sim 20\%$ using three-station measurement, and with the first station included.[5] This accuracy will accomplish a single muon trigger rate of < 1 kHz per unit rapidity at the full LHC luminosity.

3. Construction and Test of the CSC Sector Processor Prototype

A SP prototype, shown on the right of Figure 1, was designed and built at the University of Florida. It is a twelve-layer 9Ux400 mm VME board. There are 17 FPGSs (in ball grid array), 12 SRAMs, and ten thousands vias on the board. The prototype had undergone series of tests and its entire functionality had been verified. Logic tests on each of the main components were done by sending test patterns, which resemble the track segments from muon tracks in the endcap muon system, through each component. The output from these components were then compared to the results from the CSC Track-Finder simulation. Test patterns from 200 thousand single muon tracks and from 60 thousand triple muon tracks were sent through the hardware at 40 MHz, and results from the hardware output were similar to the results from the simulation. Transmission of track segment data from receiver boards to the SP prototype via the custom backplane had also been tested successfully. The receiver boards, which sit in the same crate as the SP, receive track segment data from the front end electronics via optical links.

References

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