The Track-Finding Processor for the Level-1 Trigger of the CMS Endcap Muon System

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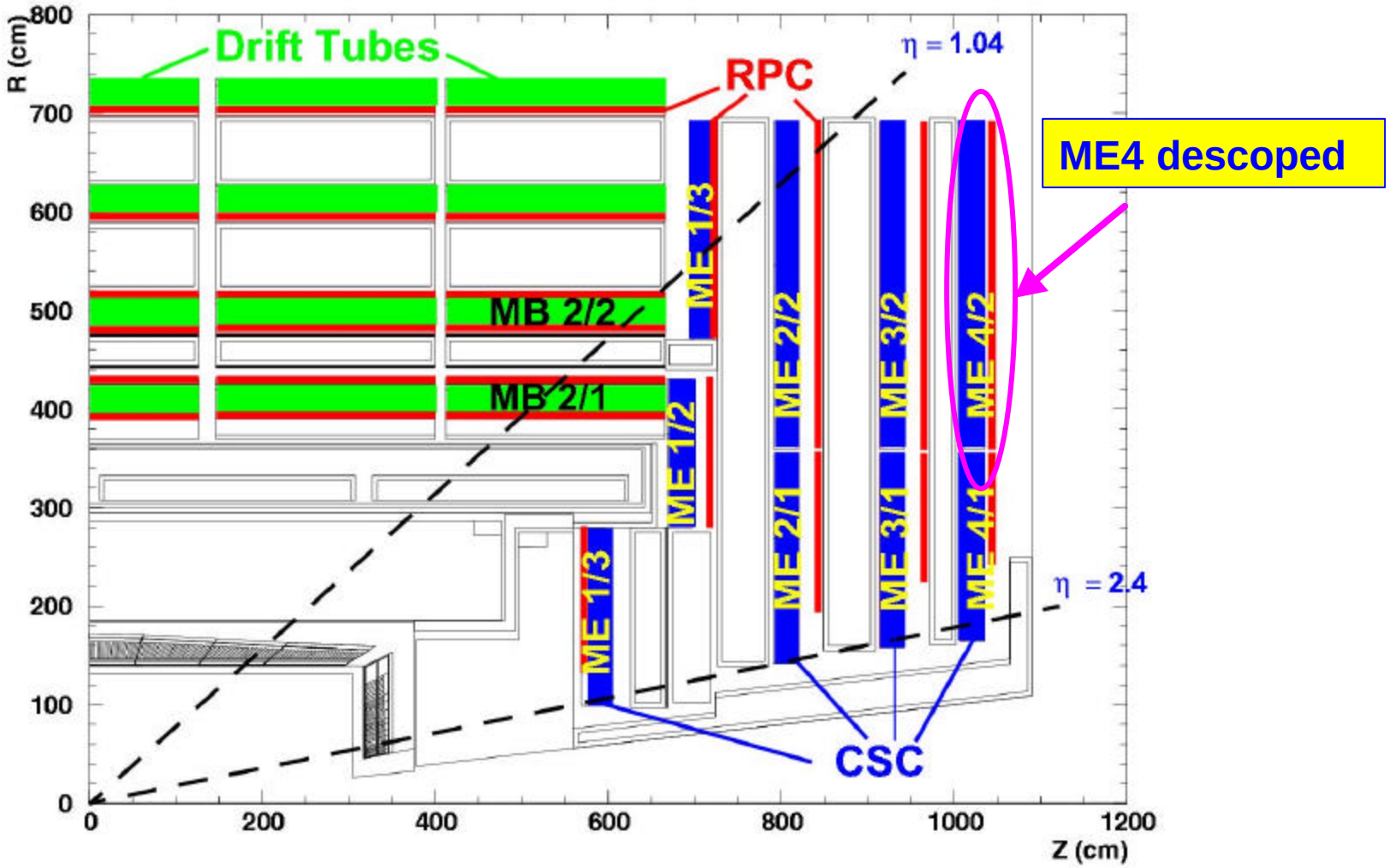
Geometric Coverage



Trigger Regions in j

Track-Finding performed in independent 60° sectors

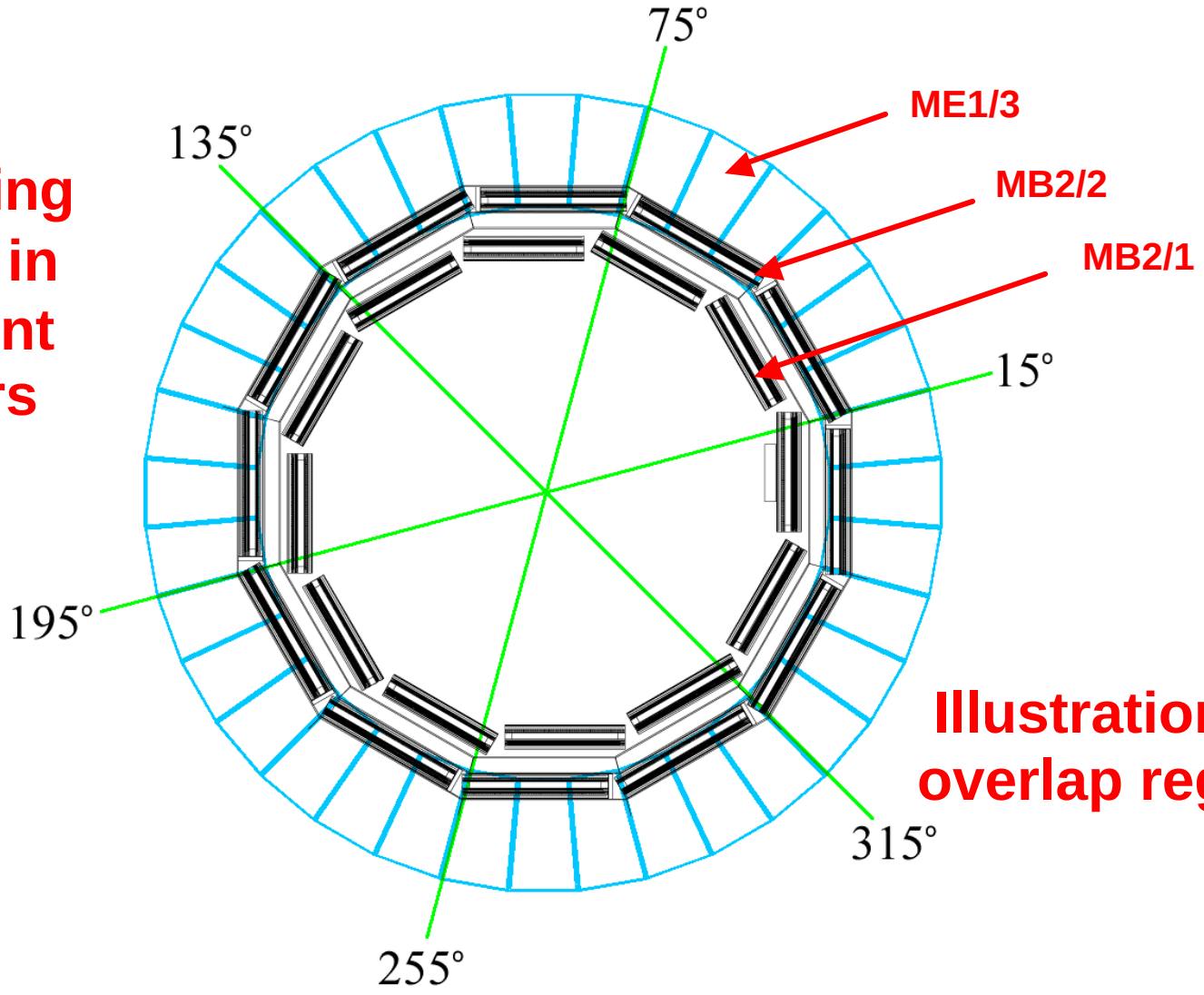


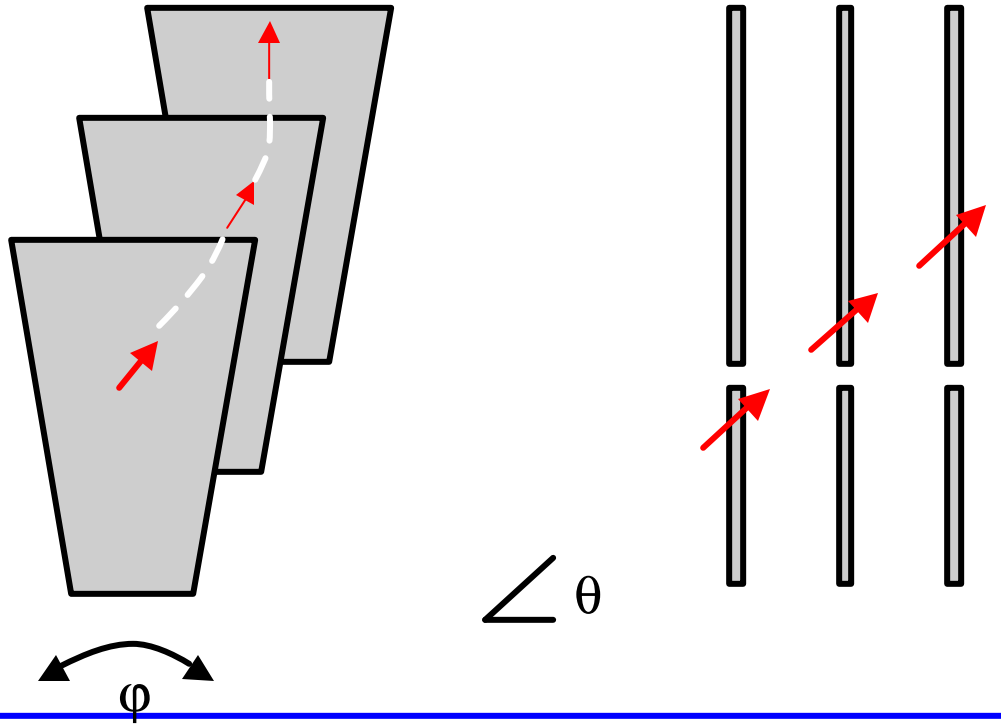
Illustration of overlap region

Muon Track-Finding

Perform 3D track-finding from trigger primitives

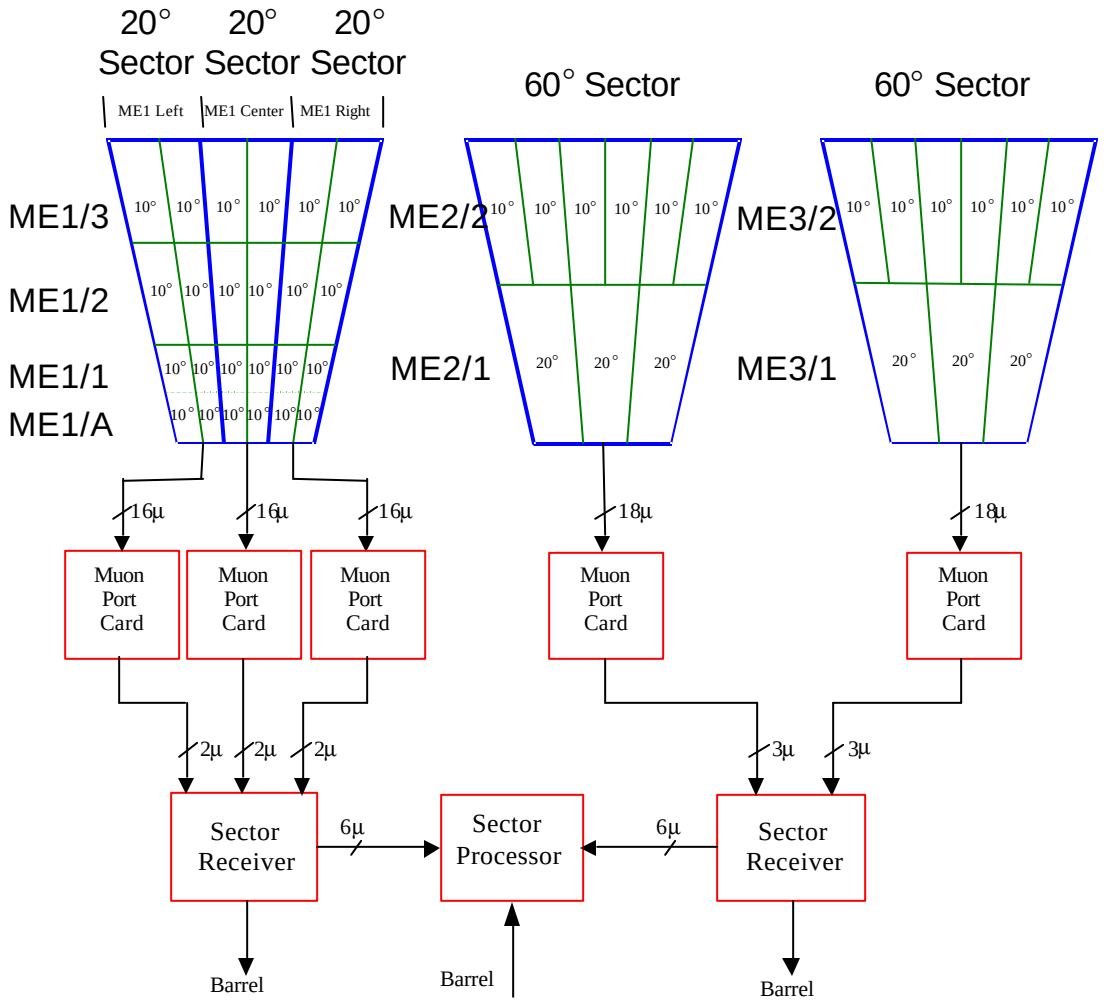
Measure P_T, ϕ, and η

Transmit highest P_T candidates to Global L1



Sector Partitioning

30° or 20° subsectors in ME1



60° sectors in ME2 —ME4

2 or 3 MPC

6 m / SR

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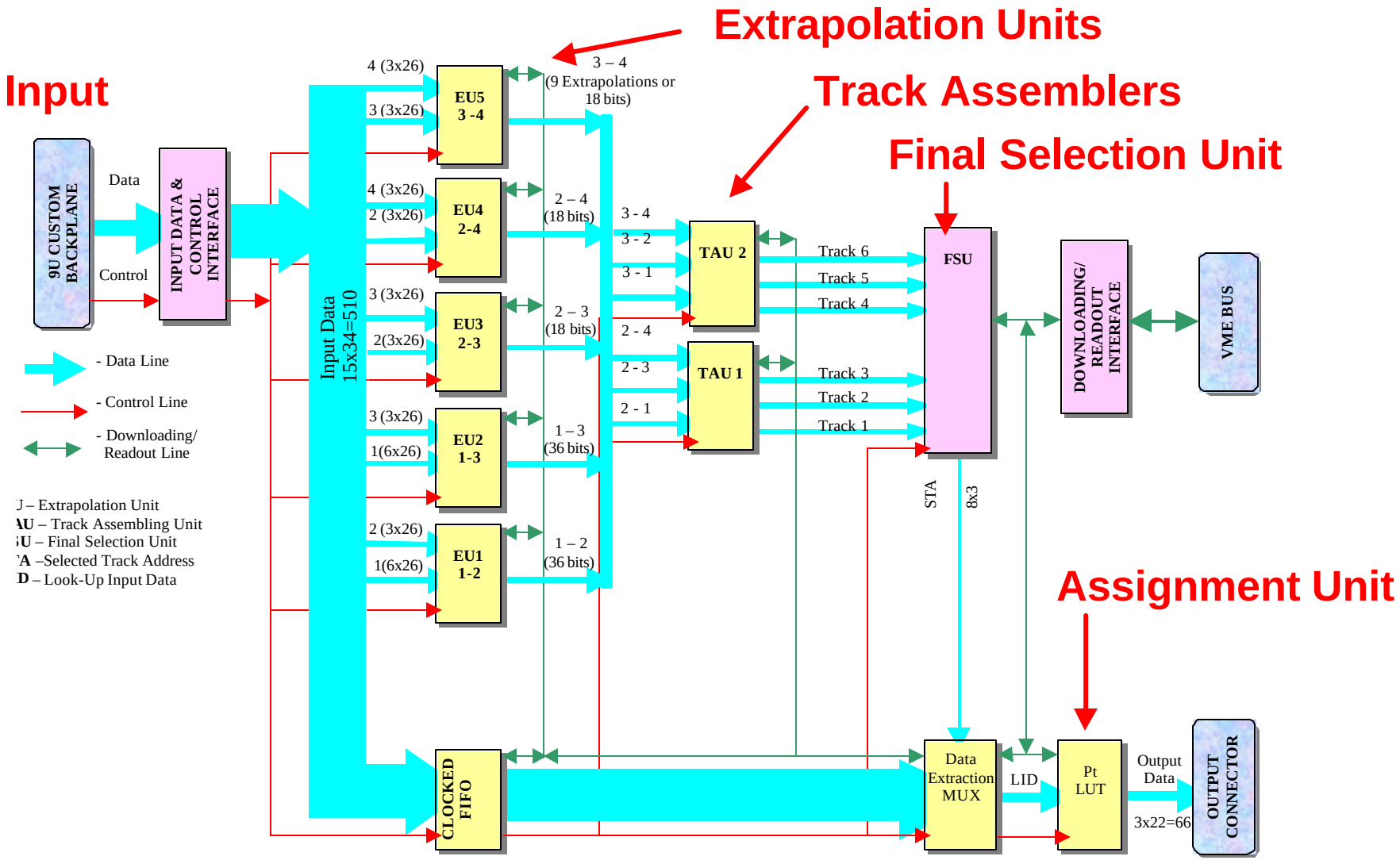
Sector Processor Functionality

- Identify and measure muons from ~ 600 bits every 25ns (3 GB/s)
- Perform all possible station-to-station extrapolations in parallel
  - Simultaneously search roads in η and ϕ
- Assemble 3- and 4-station tracks from 2-station extrapolations
- Cancel redundant short tracks if track is 3 or 4 stations in length
- Select the three best candidates
- Calculate P_T, η, ϕ and send to CSC muon sorter

Sector Processor Block Diagram



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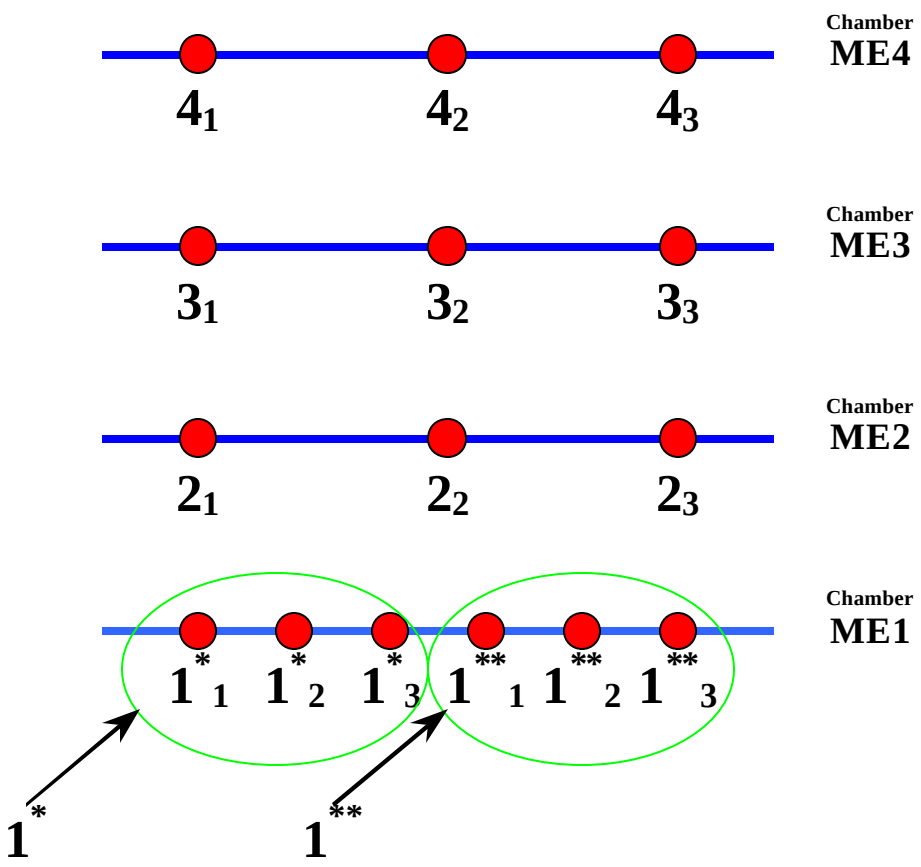
Sector Processor Logic



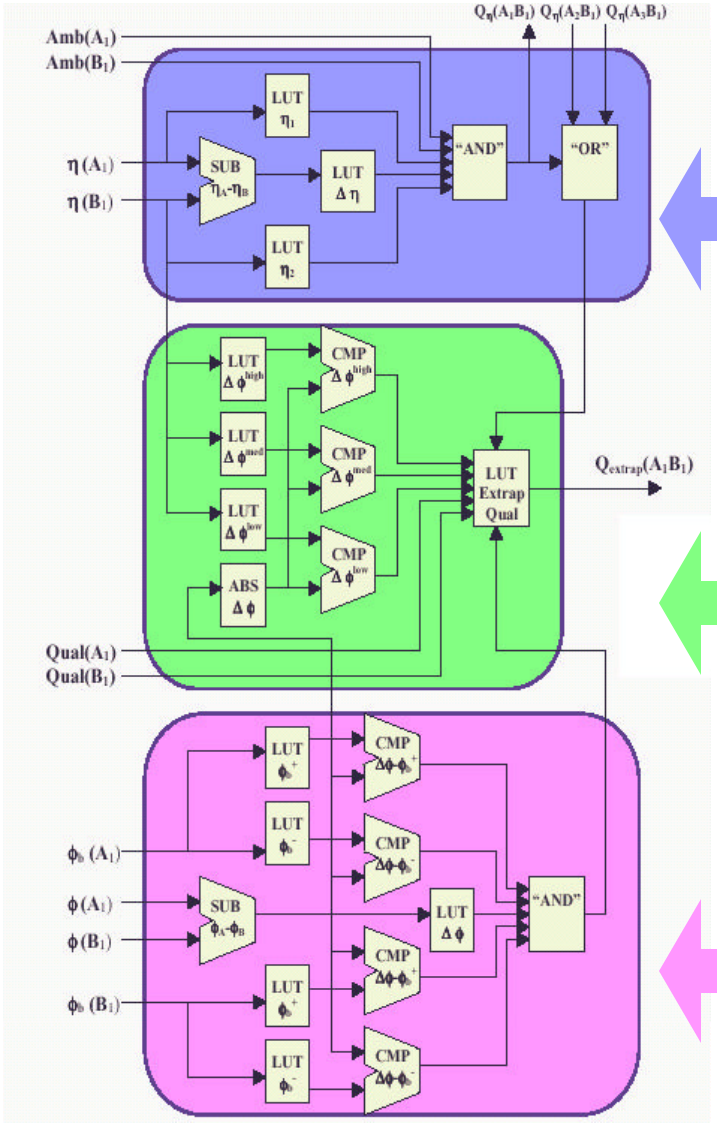
➔ **Perform all combinations of extrapolations in parallel:**

1_i « 2_k, 1_i « 3_k, 2_i « 3_k 2_i « 4_k, 3_i « 4_k

But not 1_i « 4_k

➔ **Track Assembler takes best 2 or 3 extrapolations per reference segment**

Extrapolation Unit



h Road Finder:

- Check if track segment is in allowed trigger region in η.
- Check if Δη and η bend angle are consistent with a track originating at the collision vertex.

Quality Assignment Unit:

- Assigns final quality of extrapolation by looking at output from η and φ road finders and the track segment quality.

f Road Finder:

- Check if Δφ is consistent with φ bend angle ϕ_b measured at each station.
- Check if Δφ in allowed range for each η window.

Track Assembler Unit

Functions:

- Determines if any track segment pairs belong to the same muon
- Combines those segments and assigns a code to denote which muon stations are involved
- Outputs a quality word for the best track for each hit in the key stations (2 and 3)

Final Selection Unit

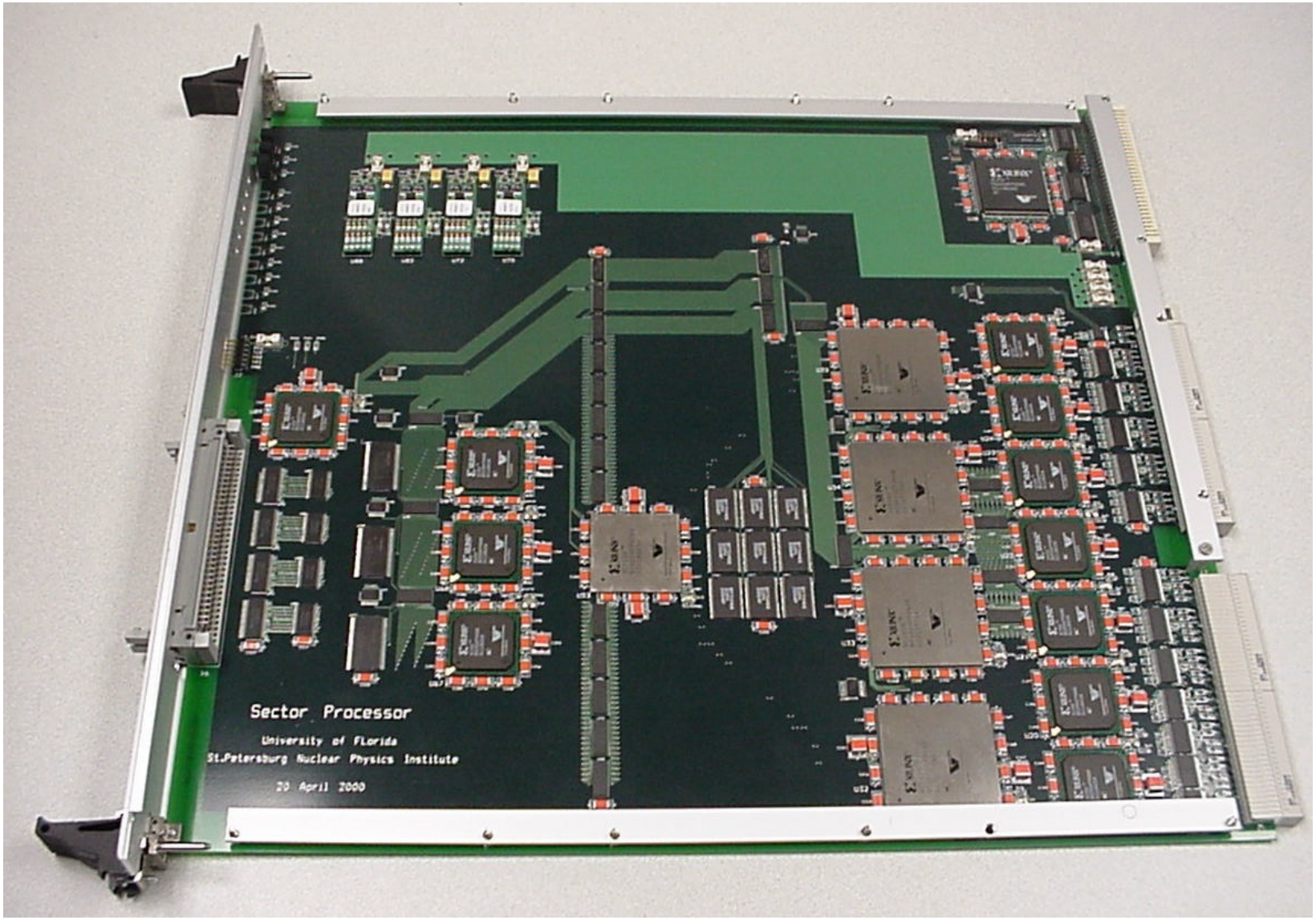
Functions:

- Select three best out of nine tracks presented by Track Assemblers
- Cancel redundant tracks (parts of the longer track)

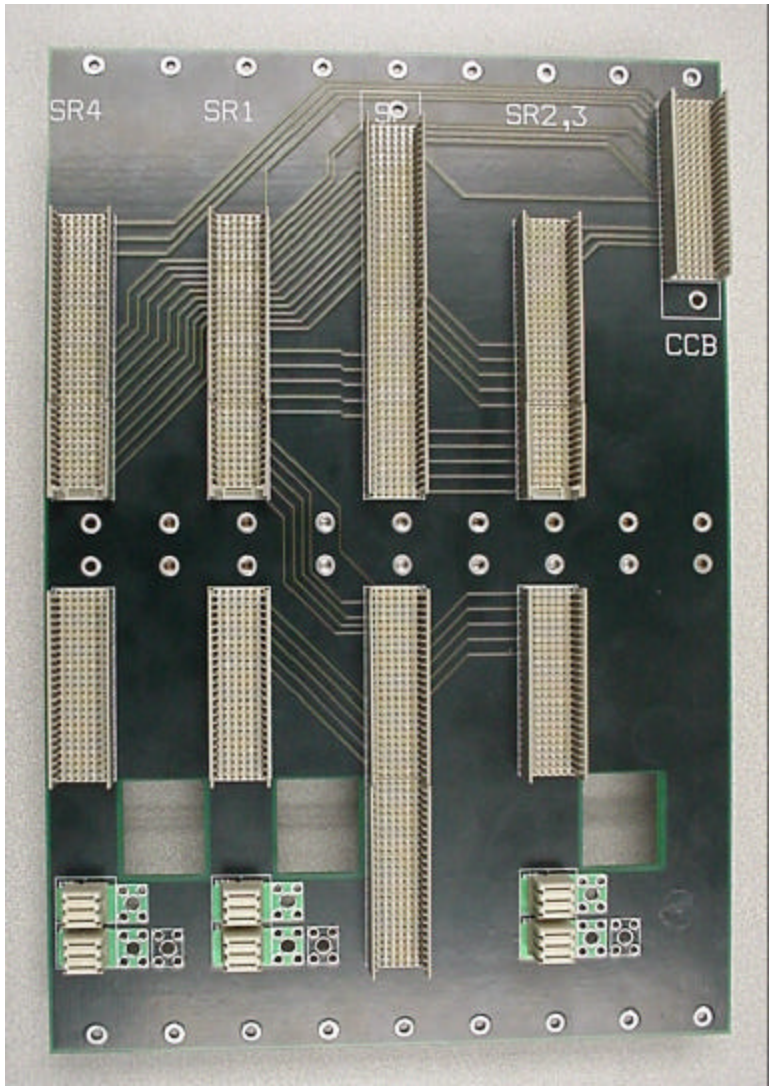
Pt Assignment Unit

- **Calculates P_T, ϕ, η of the three best muons selected by Final Selection Unit.**

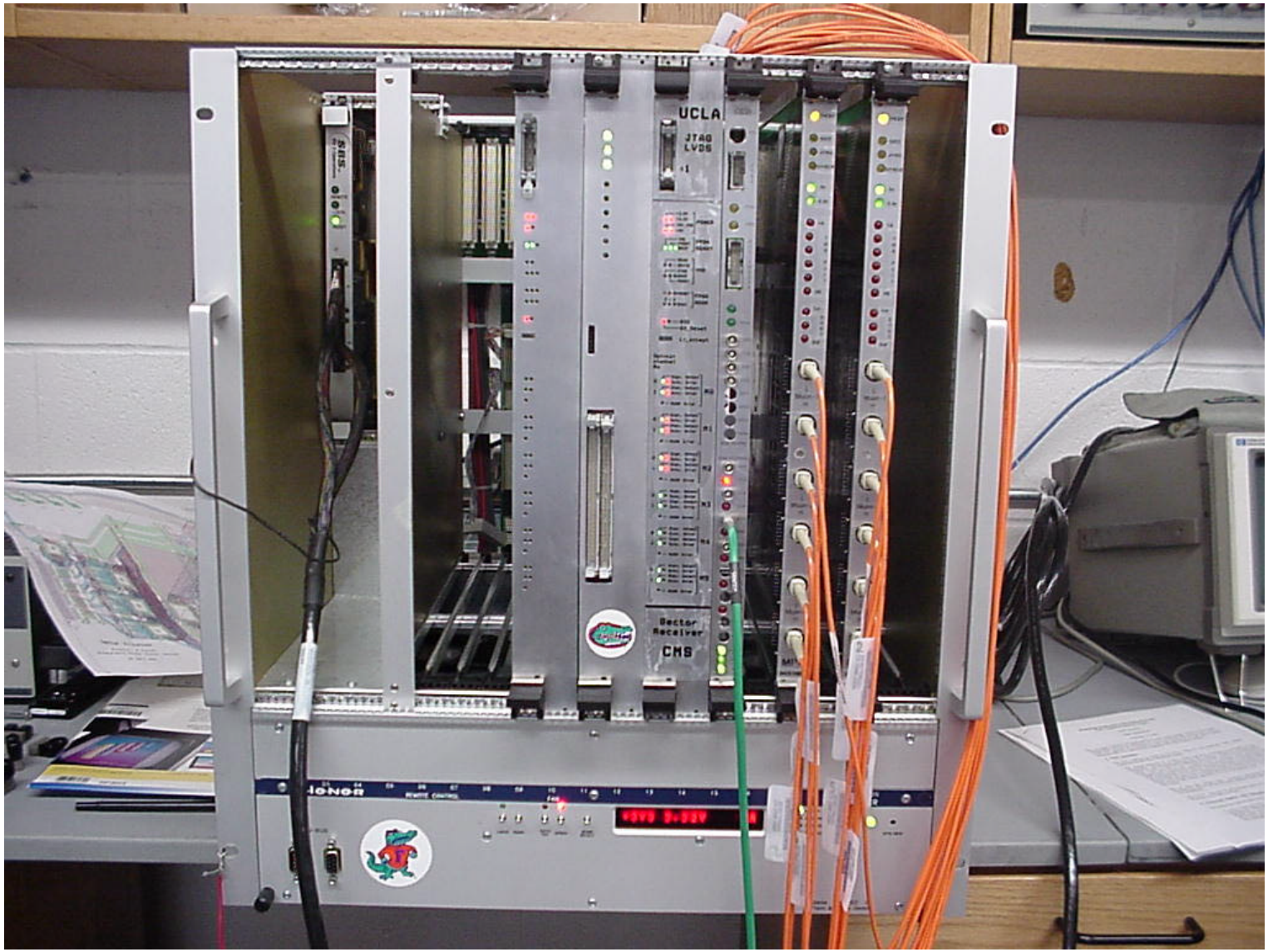
First Prototype



Custom LVDS Backplane



Test crate



First Prototype Results

- Track-Finder algorithm implemented in 15 Xilinx Virtex FPGAs, ranging from XCV50 to XCV400
- One XCV50 for VME interface
- One XCV50 for output FIFO
- Latency 15 clocks
- Output compared with C++ model, using simulated input data as well as random numbers, transmitted via custom backplane
- 100% matching demonstrated

Test software

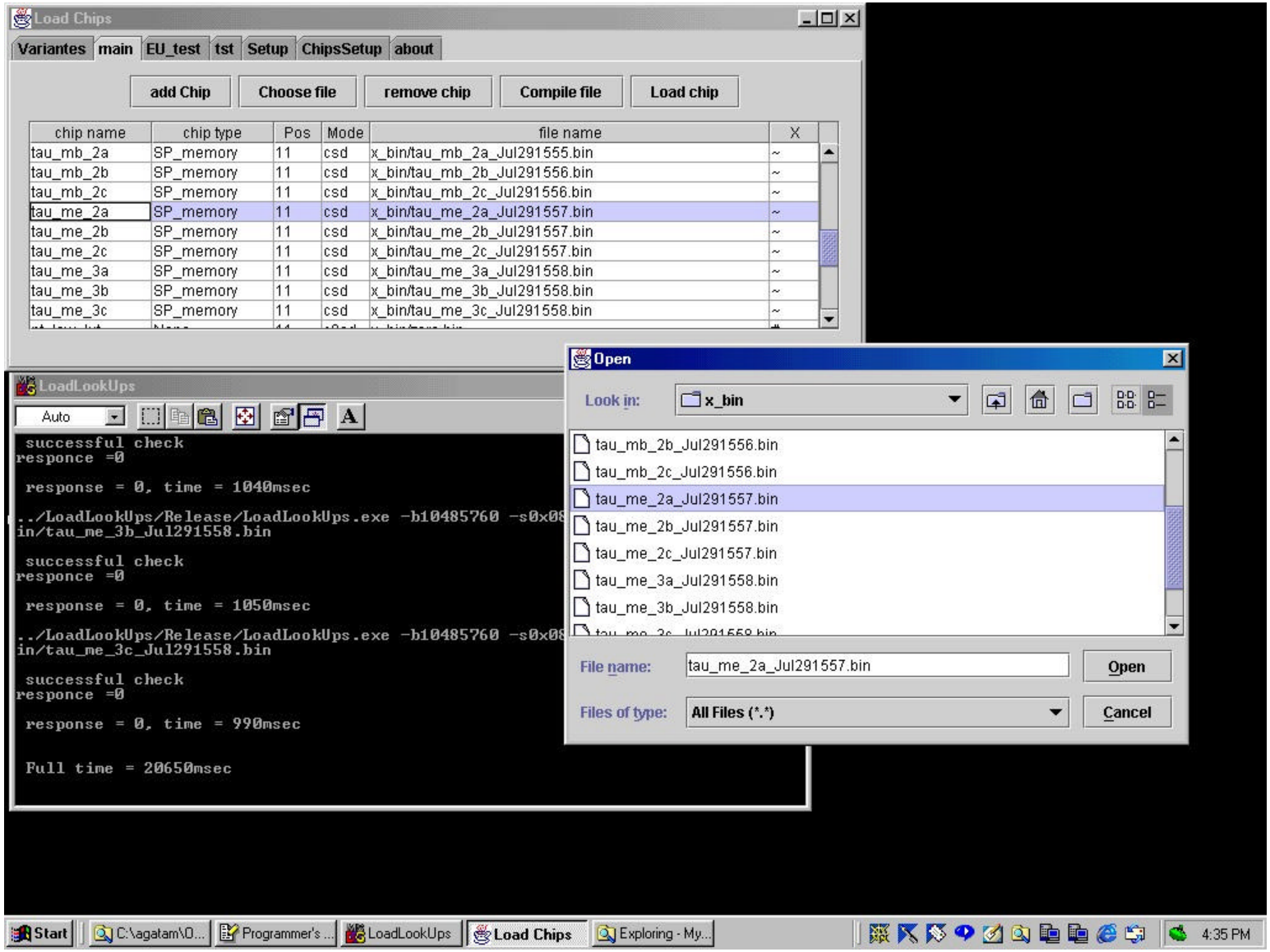
Written:

- Standalone version of the C++ model for Windows
- Module for the comparison of the C++ model with the board's output
- JTAG configuration routine, controlling the fast VME-to-JTAG module of the board
- Lookup configuration routine, used to write and check the on-board lookup memory
- Board Configuration Database with a Graphical User Interface (GUI), that keeps track of many configuration variants and provides a one-click selection of any one of them. Each variant contains the complete information for FPGA and lookup memory configuration. Can be used for multiple boards.

To simplify possible porting:

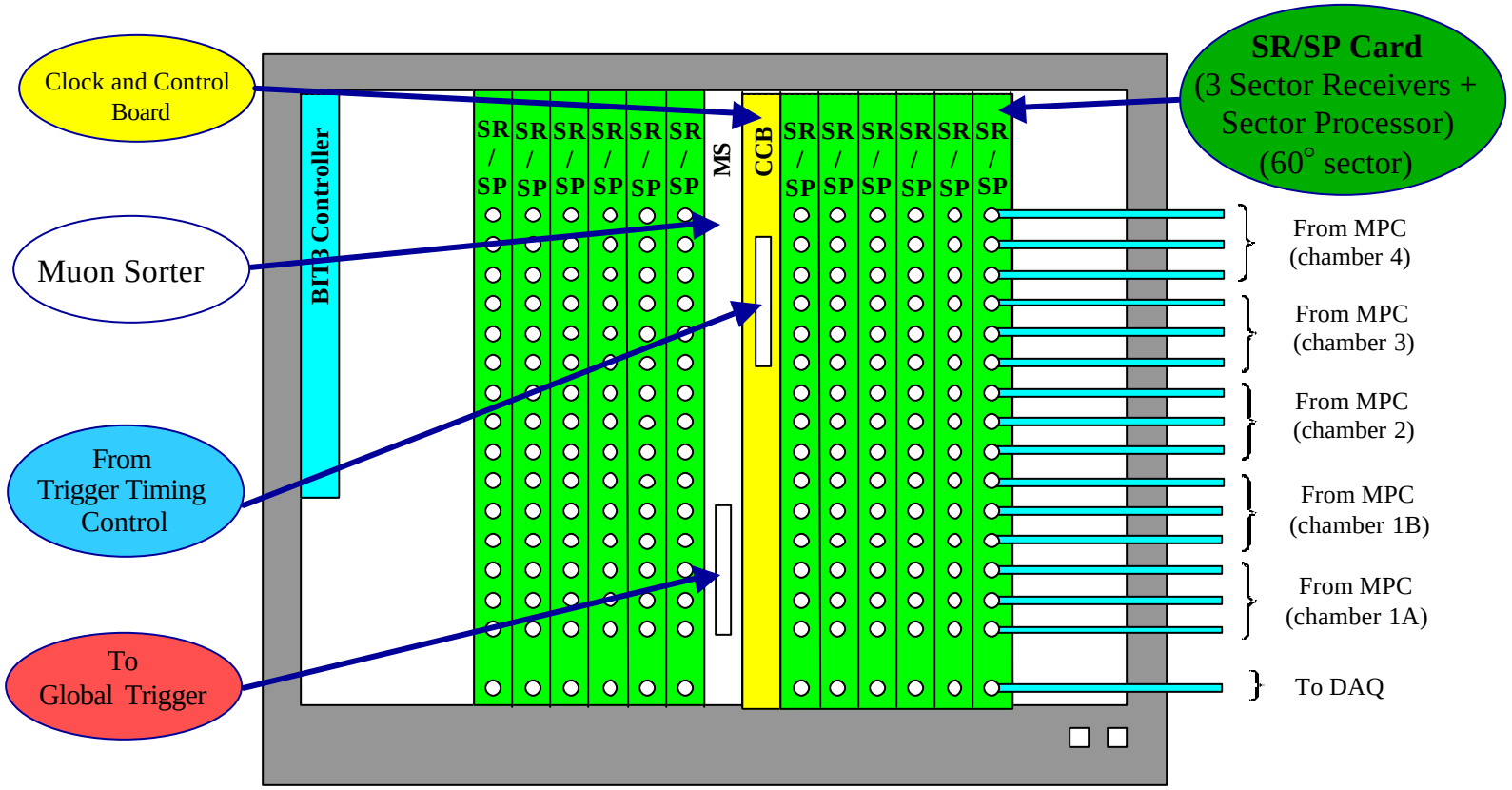
- All software is written in portable C or C++
- GUI is written in JAVA

Test Software Screenshot



Single Crate Solution

Track-Finder crate (1.6 Gbits/s optical links)

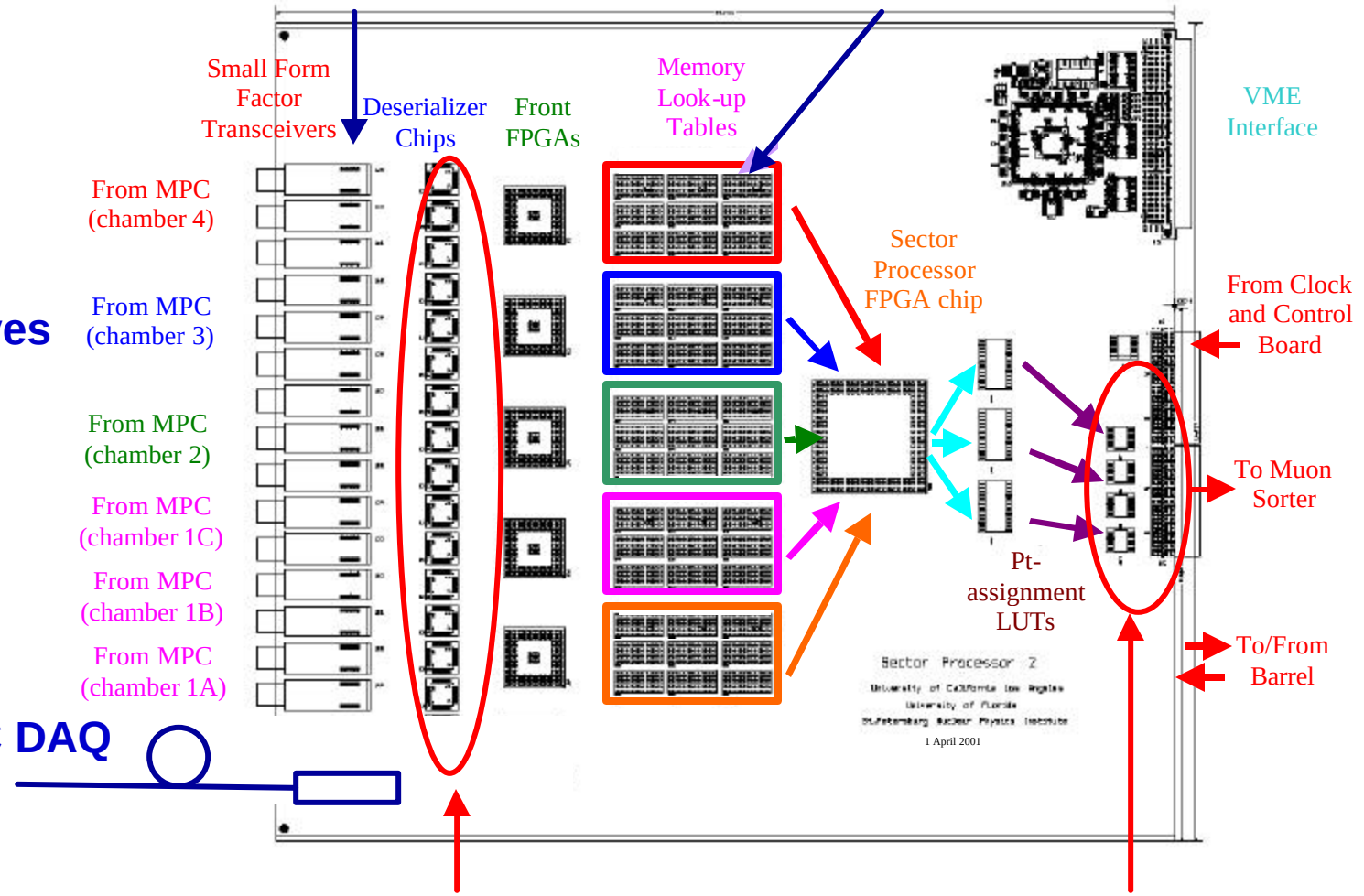


- **Power consumption: ~ 500W per crate**
- **15 optical connections per SR/SP card**
- **Custom backplane for SR/SPs < > CCB/MS connection**

Merged SR/SP

15 trigger links, 1 DAQ

45 SRAM



From trigger primitives

To CSC DAQ

Input: 528 bits/sector/b.x.

Output: 60 bits/sector/b.x.

Salient Features

Bi-Directional Optical Links

- ➔ Since we have both transmitters and receivers in the optical connection, this allows the option to send data as well as receive
- ➔ Makes testing much easier
  - One board sends data to other, or even itself through links

SP chip on a mezzanine board

- ➔ Decouples board development from FPGA technology
- ➔ Makes upgrades easier

DT fan-out on transition board

- ➔ Deliver all possibly needed signals to backplane connector
- ➔ Settle transmission technology, connector type, connector count on transition board at a later date

SR/SP Inputs

➔ **Muon Port Cards deliver 15 track stubs each BX via optical**

Sent on first frame

Signal	Bits / stub	Bits / 3 stubs (1 MPC)	Bits / 15 stubs (ME1–ME4)	Description
½ Strip *	8	24	120	½ strip label
CLCT pattern *	4	12	75	Pattern number without 4/6, 5/6, 6/6
L/R bend *	1	3	15	Sign bit for pattern
Quality *	3	9	45	Computed by TMB
Wire group	7	21	105	Wire group label
Accelerator m	1	3	15	Straight wire pattern
CSC i.d.	4	12	60	Chamber label in subsector
BXN	2	6	30	2 LSB of BXN
Valid pattern	1	3	15	Must be set for above to apply
Spare	1	3	15	
Total:	32	96	480	(240 bits at 80 MHz)

Reduced from 5

Needed for frame info

➔**DT Track-Finder delivers 2 track stubs each BX via LVDS**

Signal	Bits / stub	Bits / 2 stubs (MB1: 60°)	Description
f	12	24	Azimuth coordinate
f_b	5	10	ϕ bend angle
Quality	3	6	Computed by TMB
BXN	2	4	2 LSB of BXN
Synch/Calib	1	2	DT Special Mode
Muon Flag	1	2	2nd muon of previous BX
Total:	24	48	

SR/SP Outputs

➔ **6 track stubs are delivered to DT Track-Finder each BX (delivered at 40 MHz to transition board)**

Signal	Bits / stub	Bits / 2 stubs (ME1: 20°)	Bits / 6 stubs (ME1: 60°)	Bits / 6 stubs @ 80 MHz	Description
f	12	24	72	36	Azimuth coordinate
h	1	2	6	3	DT/CSC region flag
Quality	3	6	18	9	Computed by TMB
BXN	–	2	6	3	2 LSB of BXN
	16	34	**102**	**51**	**Total**

➔ **3 muons per SP are delivered to Muon Sorter via GTLP backplane**

Sent on first frame

Signal	Bits / m	Bits / 3 m (1 SP)	Bits / 36 m (12 SP)	Description
f	5	15	180	Azimuth coordinate
h	5	15	180	Pseudorapidity
Rank *	7	21	252	5 bits p_T + 2 bits quality
Sign *	1	3	36	
BXN *	–	2	24	2 LSB of BXN
Error *	–	1	12	
Spare *	1	3	12	
Total:	19	60	**720**	**(360 bits at 80 MHz)**

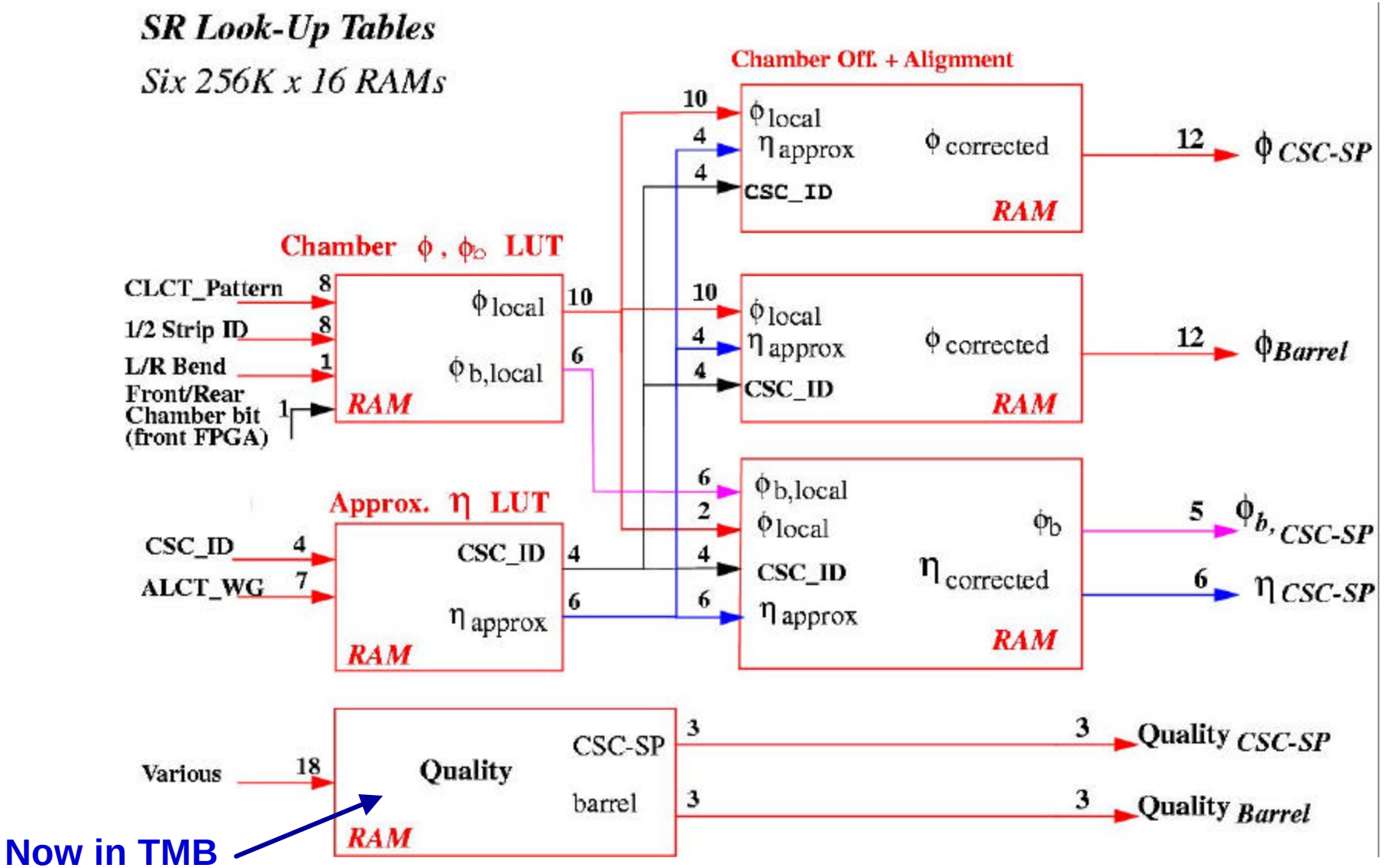
SR/SP Internal Dataflow

➔ **Data delivered from SR to SP**

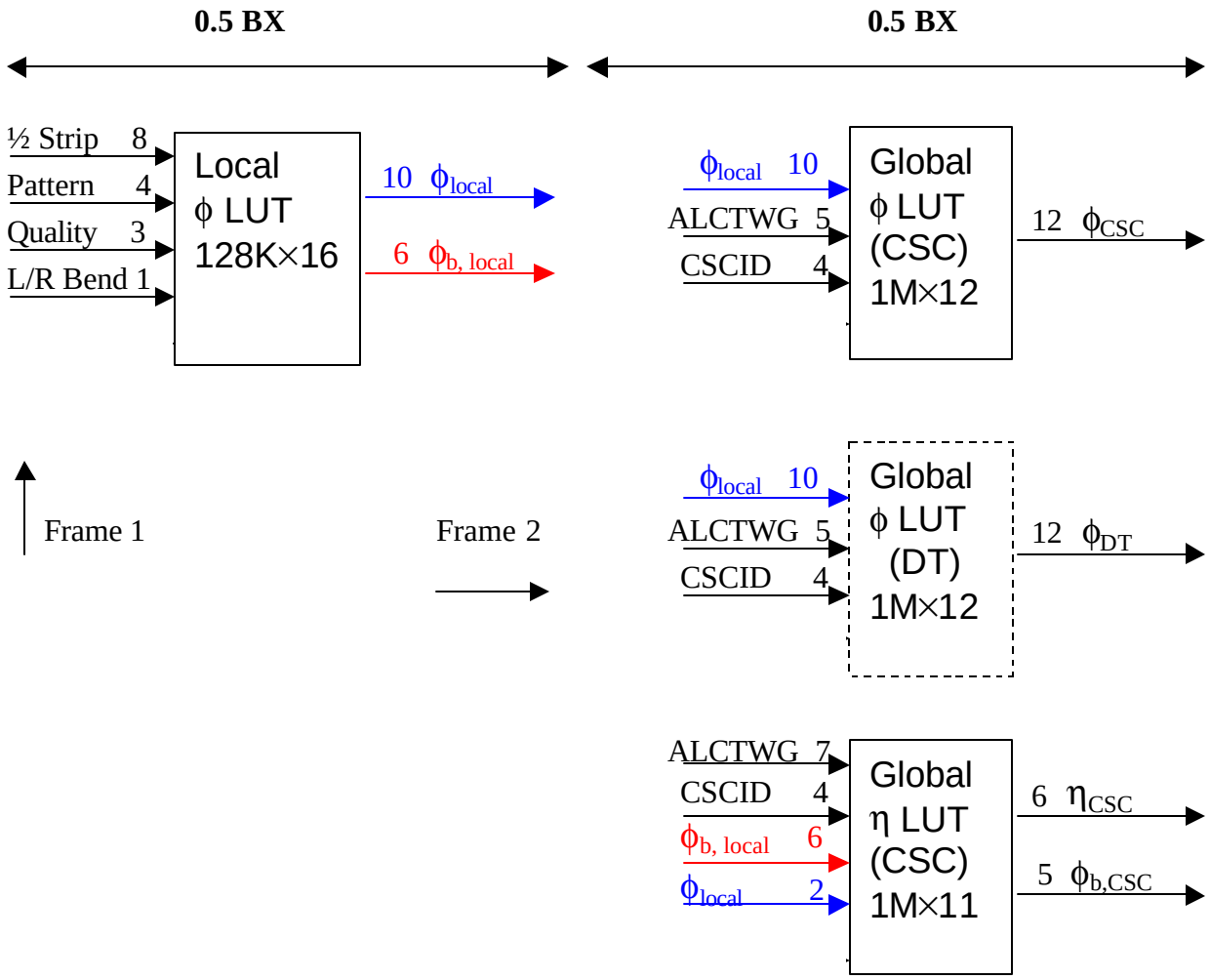
Signal	Bits / stub	Bits / 6 stubs (ME1)	Bits / 15 stubs (ME1–ME4)	Description
f	12	72	180	Azimuth coordinate
f_b	5	30	75	ϕ bend angle
h	6	36	90	Pseudorapidity
Accelerator m	1	6	15	η bend angle
Front/Rear *	1	6	6	ME1 chamber stagger
CSC ghost *	–	4	4	2 stubs in same ME1 CSC
Quality	3	18	45	Computed by TMB
Total:	28	172	**415**	~~(sent at 80 MHz)~~

ME1 only

Old SR Memory Scheme



New SR Memory Scheme



Discussion of SR Memory (1)

Data Frames:

- Data arrives off links @ 80 MHz
- The proposed framing scheme implies no latency loss
  - First LUT operates on first frame only (but must reduce CLCT pattern label by 1 bit)
- This frame definition must be applied in the TMB where the data is generated and first serialized (i.e. before MPC) to avoid latency penalty

Memories:

- LUT for DT only applies to ME1
- Chip count is 3 per stub, down from 6 originally
- Increased memory size to 0.5M (okay for synch. SRAM)

Discussion of SR Memory (2)

One memory set per stub:

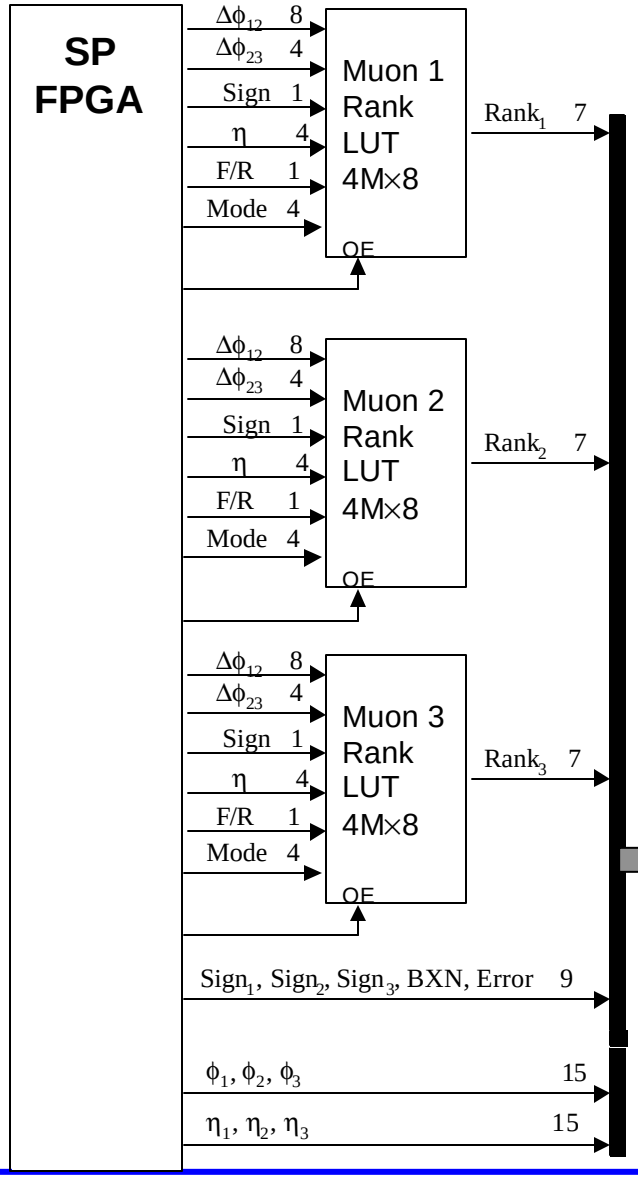
- ➔ 15´3 = 45 chips
- ➔ 1 BX latency
- ➔ 415 signals to SP

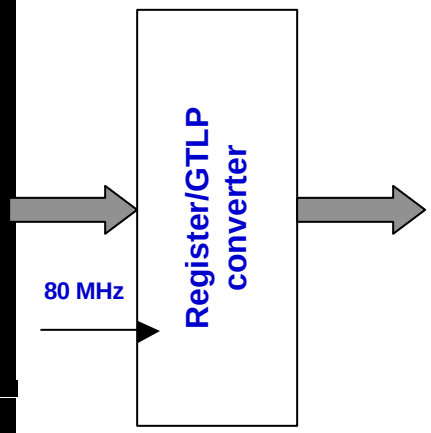
First SR had 36 chips and 1 BX latency

Memory choices:

- ➔ synch SRAM clocked at 160 MHz (tested to this frequency)
- ➔ Flow Through SRAM clocked at 80 MHz

Pt Assignment Memory Scheme





- Must serialize to fit data on backplane
- No latency penalty for serialization if Rank sent first to Muon Sorter
- SP FPGA contains tri-state buffers and generates enable for memories

Frame 1

80 MHz

To GTLP Backplane

Frame 2

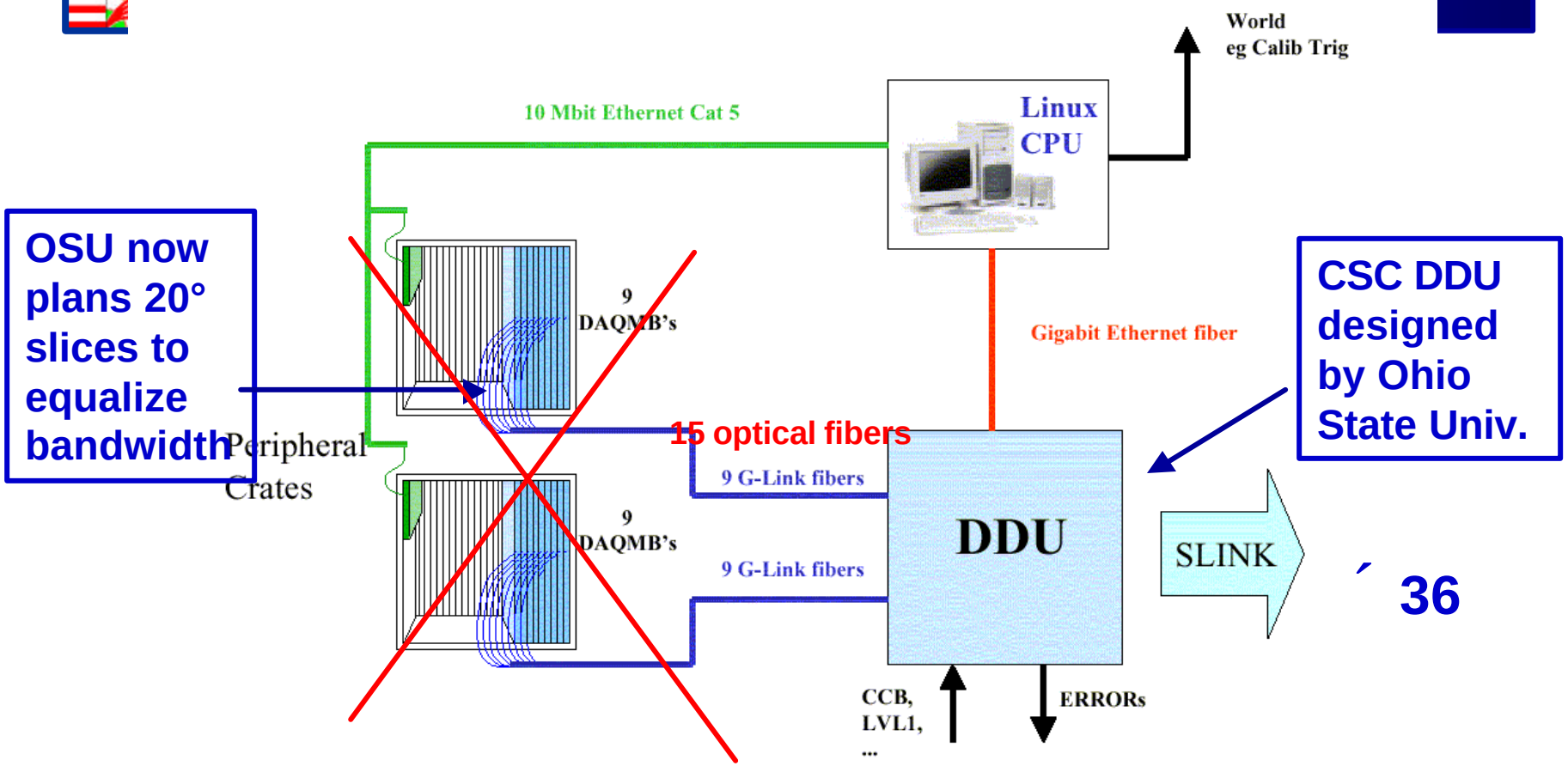
CSC TF DAQ Plans

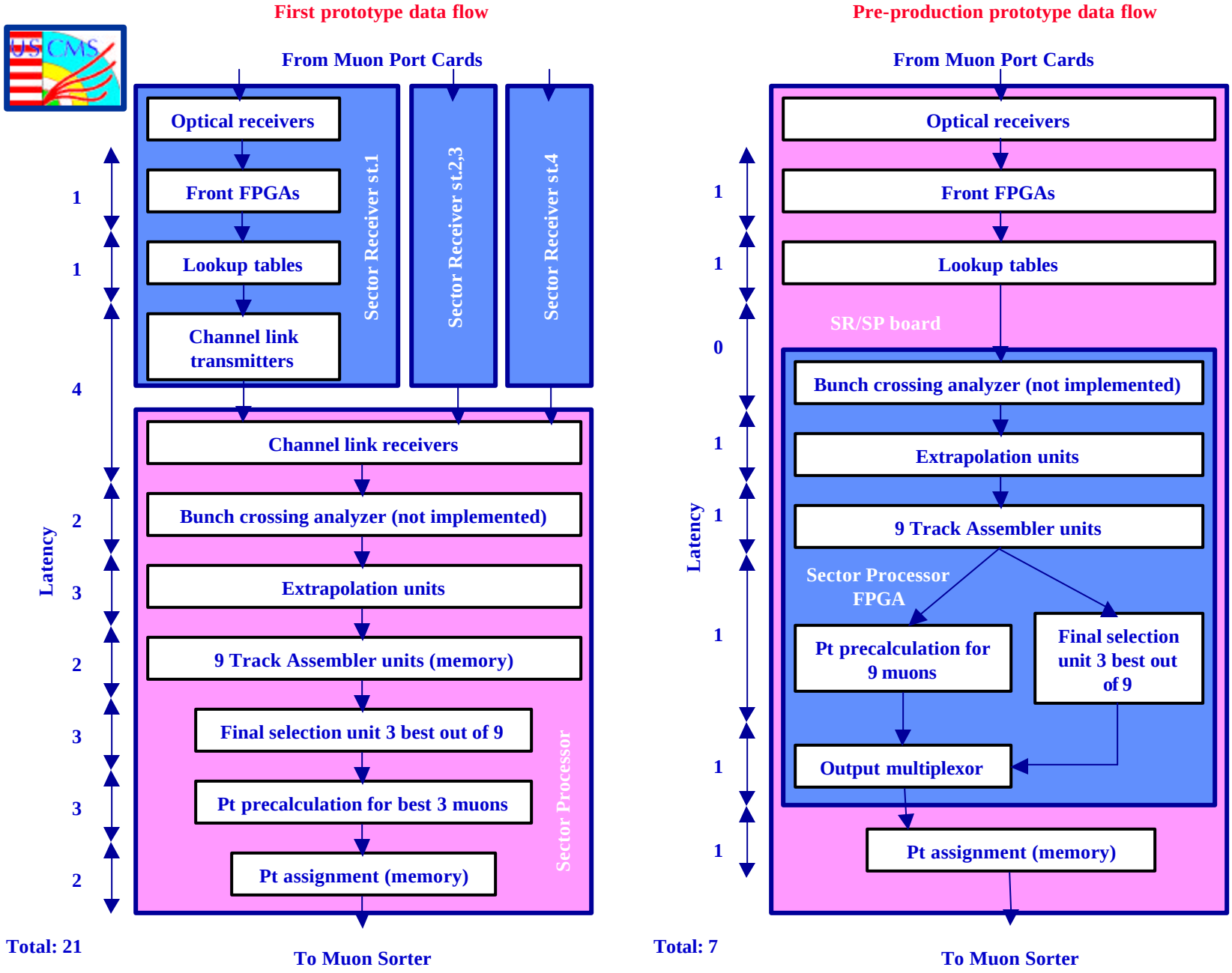
Send input of SR and output of SP to DAQ stream for diagnostics

Track-Finder DAQ acts as additional DDU for EMU system

- ➔ Plan to use existing DDU design by OSU
  - OSU has decided to use T.I. Chip for serialization
  - 12 SP fiber connections fits well into 15 planned for DDU

Mirror CSC DAQ Path




First prototype data flow
From Muon Port Cards
Optical receivers
Front FPGAs
Lookup tables
Channel link transmitters
Sector Receiver st.1
Sector Receiver st.2,3
Sector Receiver st.4
Channel link receivers
Bunch crossing analyzer (not implemented)
Extrapolation units
9 Track Assembler units (memory)
Final selection unit 3 best out of 9
Pt precalculation for best 3 muons
Pt assignment (memory)
Sector Processor
Latency
1
1
4
2
3
2
3
3
2
Total: 21
To Muon Sorter
Pre-production prototype data flow
From Muon Port Cards
Optical receivers
Front FPGAs
Lookup tables
SR/SP board
Bunch crossing analyzer (not implemented)
Extrapolation units
9 Track Assembler units
Sector Processor FPGA
Pt precalculation for 9 muons
Final selection unit 3 best out of 9
Output multiplexor
Pt assignment (memory)
Latency
1
1
0
1
1
1
1
1
Total: 7
To Muon Sorter

Pre-Production Prototype

Done:

- SP algorithm is rewritten in Verilog HDL
- New C++ model line-by-line corresponds to Verilog HDL code
- If Verilog HDL code is written properly, C++ conversion is very simple and straightforward
- New C++ model matches the functionality of the original C++ model
- SP-Verilog has been extensively simulated and is working in exact correspondence to functionality of the first prototype and both C++ models
- Simulated latency for Sector Processor Algorithm: 5 clocks (15 in the first prototype)
- Board development underway

Plans:

- Replacing the original C++ model with the new one in ORCA
- Adding new features into the SP-Verilog code and C++ model simultaneously, keeping them in strict line-by-line correspondence

SP Algorithm Modifications

- Extrapolation and Final Selection units are reworked, and now each of them is completed in only one clock.

- The Track Assembler Units in the first prototype were implemented as external lookup tables (static memory). For the second prototype, they are implemented as FPGA logic. This saved I/O pins on the FPGA and one clock of the latency.

- The preliminary calculations for the PT assignment are done in parallel with final selection for all 9 muons, so when three best out of nine muons are selected, the pre-calculated values are immediately sent to the external PT assignment lookup tables.

Acknowledgements

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We also would like to acknowledge the efforts of R. Cousins, J. Hauser, J. Mumford, V. Sedov, B. Tannenbaum, who developed the first Sector Receiver prototype, and the efforts of M. Matveev and P. Padley, who developed the Muon Port Card and Clock and Control Board, which were used in the tests.