TRACK-FINDER CRATE:
TESTS UPDATE AND OTHER ISSUES…

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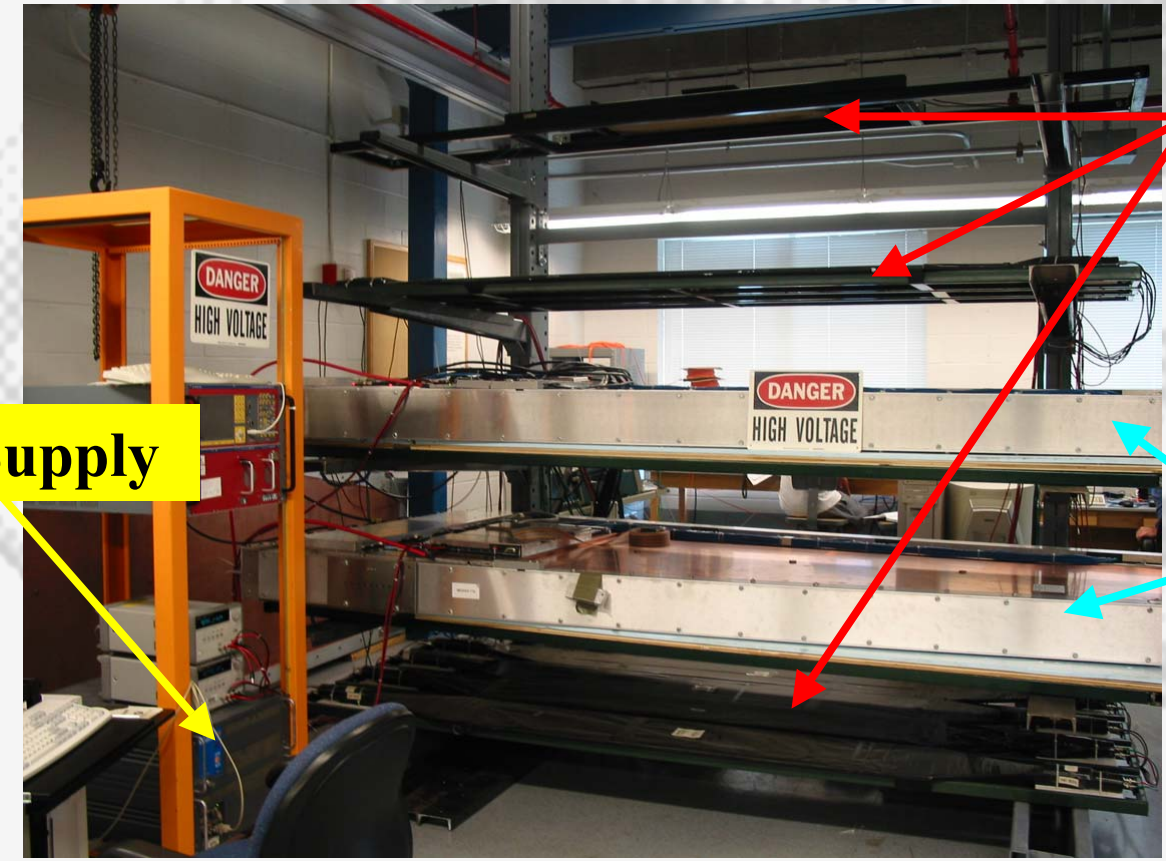
FLORIDA COSMIC STAND: DETECTORS

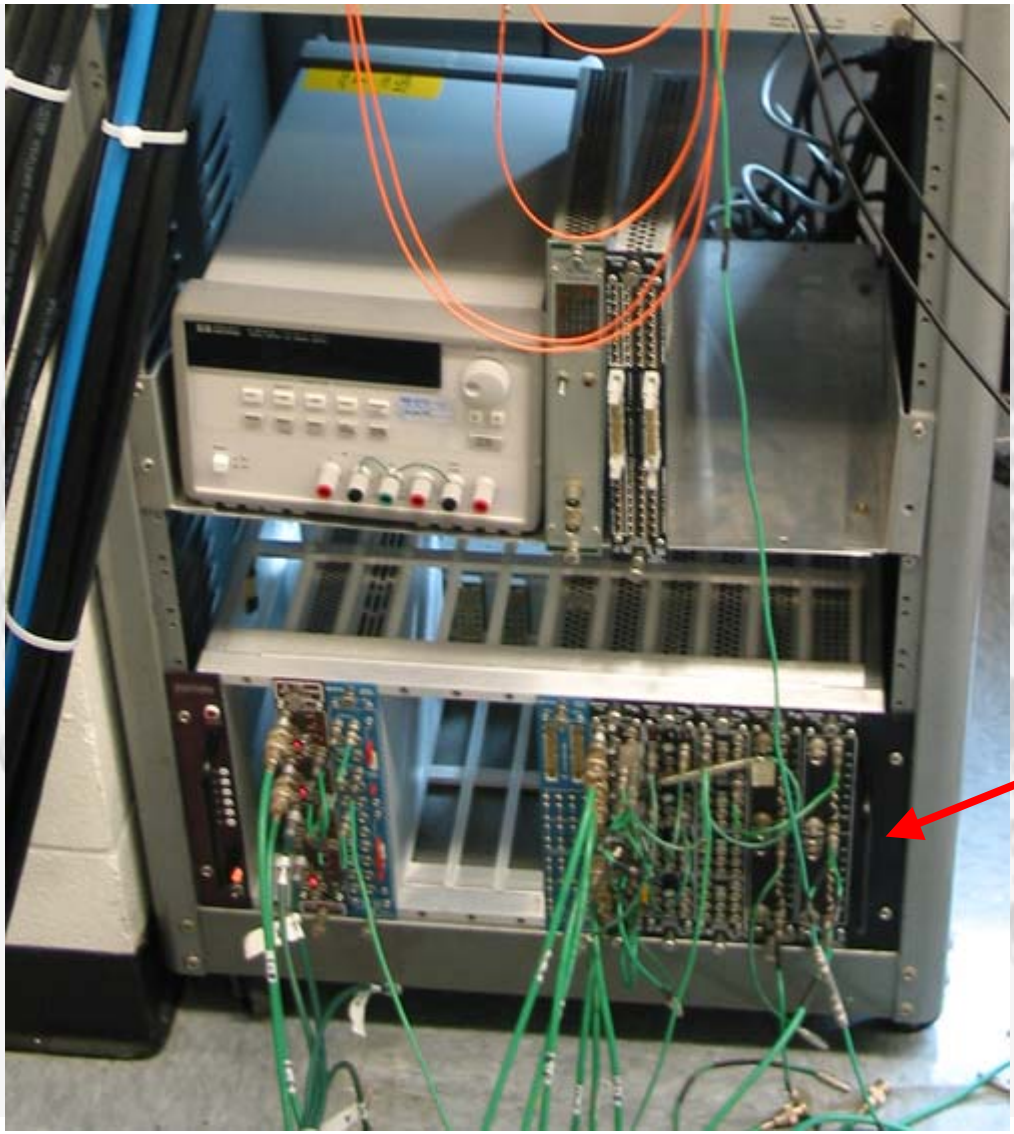


Scintillator Panels

HV Supply

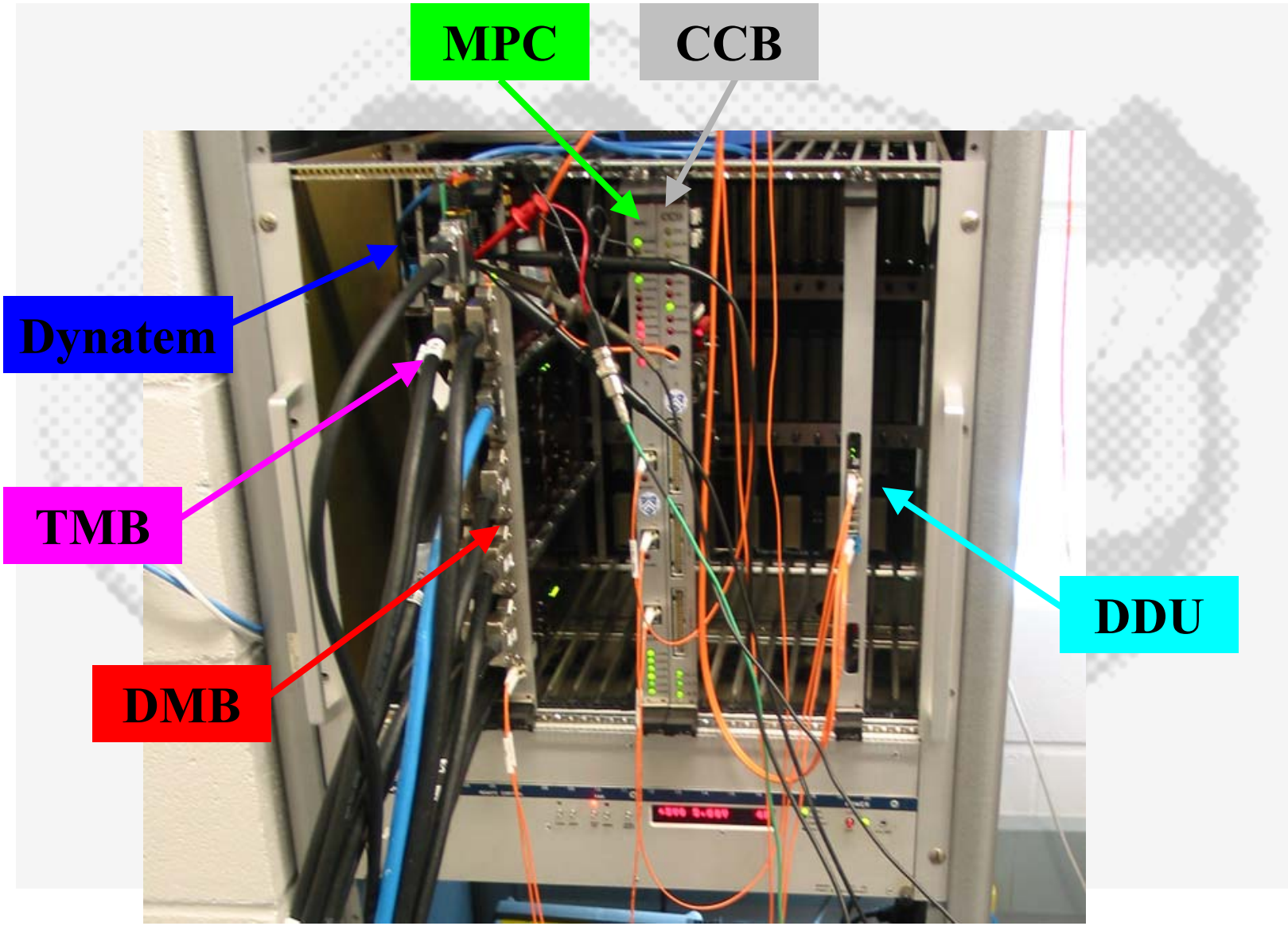
CSCs

FLORIDA COSMIC STAND: TRIGGER LOGIC

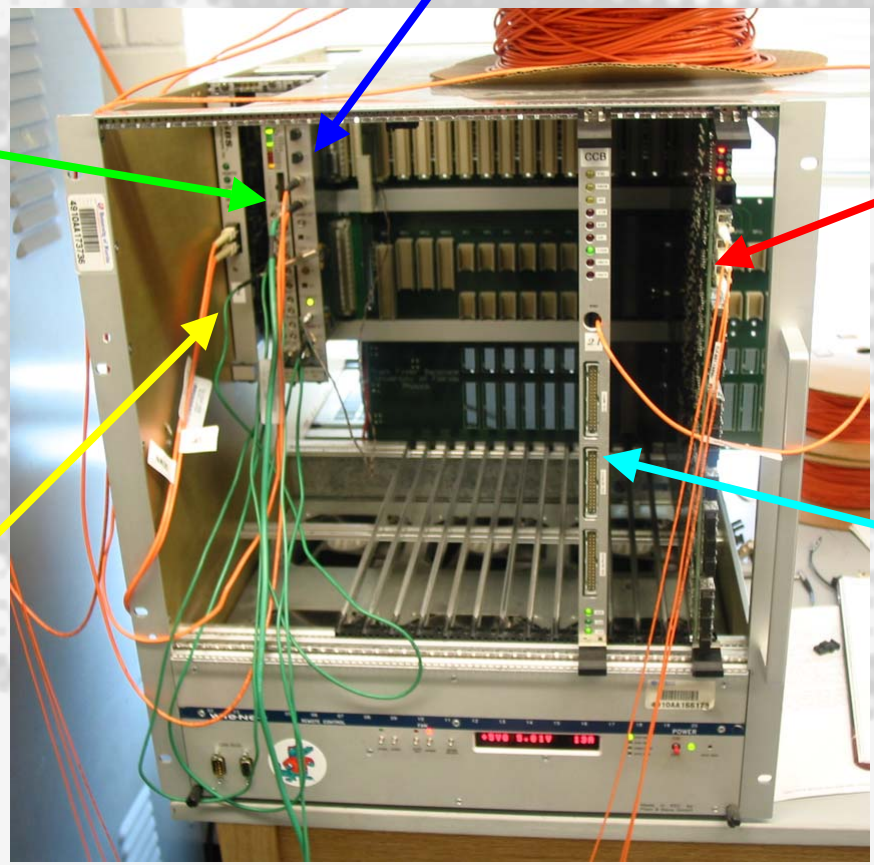


NIM Crate Modules Provide Trigger Logic

FLORIDA COSMIC STAND: PERIPHERAL CRATE



FLORIDA COSMIC STAND: TRACK-FINDER CRATE

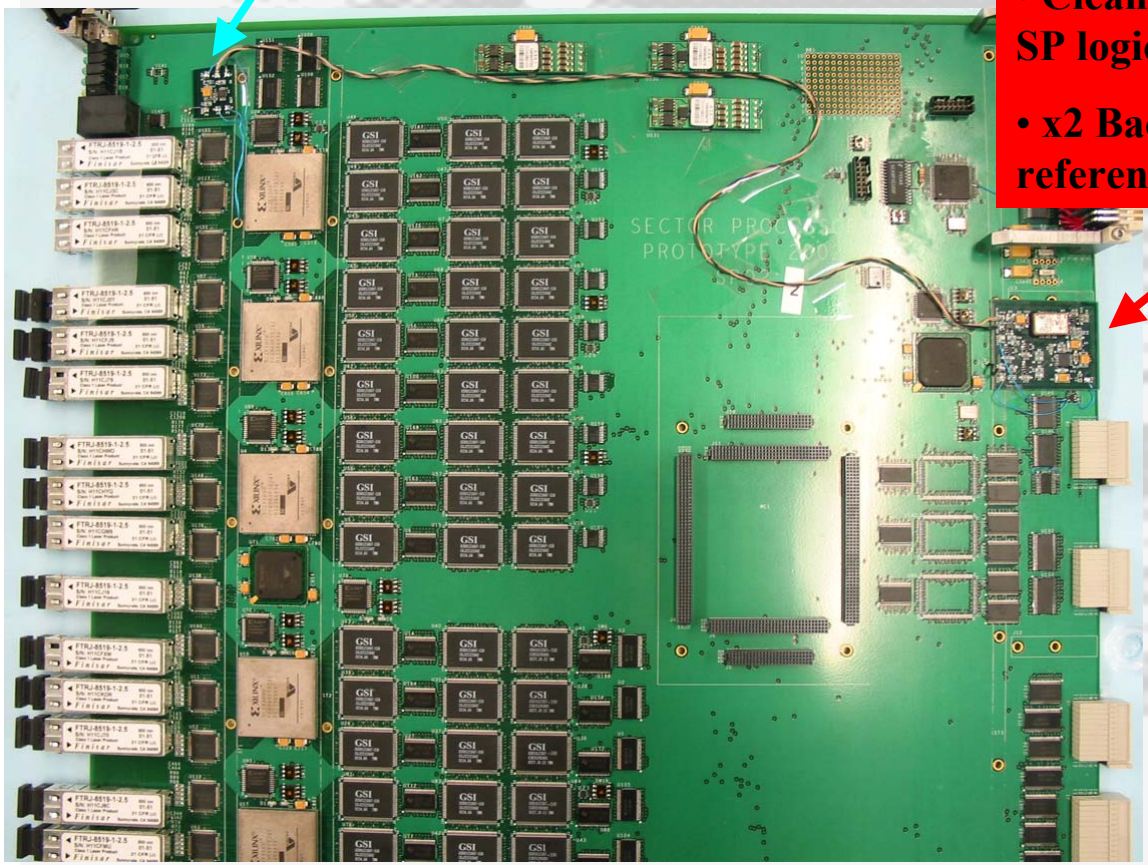


MODERATLY HAPPY SLICE-TEST PEOPLE

- **Peripheral Crate Controller Software well underway**
- **PCC SW Successfully Configures Peripheral Crate Hardware**
- **Able to read DDU data.**
- **Now working on Track Finder Crate Interface**

SECTOR PROCESSOR CLOCK PATCH (Synchronous Option)

LVDS Repeater Delivers Multiplied Clock to Front FPGAs to Drive TLK2501 clock input



Voltage Controlled Crystal Oscillator PLL Patch

- **Low jitter Output**
- **Cleans Backplane clock to Drive SP logic**
- **x2 BackPlane Clock supplies reference to TLK2501**

SECTOR PROCESSOR CLOCK PATCH: RESULTS

- SP (TFC)→SP (TFC) Loopback PRBS Test. 3 Links on Front FPGA 5:
  - Using Patched CCB clock and 100m fibers.
  - **No Errors after 5 hours.**
- MPC (TFC)→TF (TFC) PRBS Test. 3 Links on Front FPGA 5:
  - Using Patched CCB clock and 100m fibers.
  - **No Errors after 24 hours.**

SECTOR PROCESSOR CLOCK PATCH: RESULTS

TTC uses 40 MHz Clock. So, Driving TTCvx with 40.0787 MHz XO Patch:

- MPC (TFC) → SP (TFC) PRBS. 3 links on Front FPGA 5.
  - **No Errors after 32 Hours.**
- MPC (PC) → SP (TFC) PRBS. 3 links on Front FPGA 5 with L1A rate @ 100kHz.
  - **No Errors after 14 Hours.**

SECTOR PROCESSOR CLOCK PATCH: RESULTS

Asynchronous Option: Drive GTX_CLK Pin on TLK2501 Directly or Through Front FPGA with 80.1574 MHz XO **as Reference**. Received clock is recovered.

- SP (TFC)→SP (TFC) Loopback PRBS Test. 3 Links on Front FPGA 5:
  - Using TTCvx Patch Clock.
  - **No Errors after 5 hours.**

OTHER SP TESTS…

- **Working on Test Routine in CFEB Control Environment which Loads MPC Input FIFO with Random LCT Patterns to Send to SP.**
  - **TTC issues inject test pattern command to MPC and SP. This causes MPC to transmit and SP to receive.**
  - **Output files are the compared.**
- **Dynatem seems to be limitation for Sending test data to MPC.**
  - **Takes ~15s to load input FIFO with 256 BXs of LCTs.**
  - **Takes ~5s to read output FIFO.**
  - **So, we can only read/write ~3 cycles of 256 LCTs/minute or ~1M LCTs/Day.**
  - **Need ~10 years to check all possible patterns.**

OTHER SP TESTS…

- **Will also try to integrate Greg's routine to test TMB → MPC → SP communication – winner bits.**
- **Having problems getting LCT data from MPC timed into SP Links. Synchronization procedure requires BCO to be received by SP and MPC. The MPC LCT data carries a BCO flag to the SP Front FPGA which uses this flag to mark the current BXN. This measures the offset between backplane commands and LCT data.**
  - **Need LCT with VP=1 in step with BCO. But this is not possible with Cosmics.**
- **Not clear data was being transmitted to SP.**
- **Other problems:**
  - **Holger on vacation until 28th, Darin injured, Lev in Russia, no Peripheral Crate hardware experts at Florida.**

SEPTEMBER TEST BEAM

- Another opportunity to test MPC→SP communication.
  - Now have clock solution ⇒ Links will work!
- Interface with Drift Tube Track-Finder Hardware
- Help Rick with Event Builder Software
- Setting up Peripheral Crate is a concern – NOT Plug and Play!
  - **A. Tumanov spent many hours on phone with OSU and UCLA to finally read out DDU data on his final night in Gainesville**
- **The final problem was internal TMB timing registers set deep in cfeb_control software. This required TMB measurements to be made at Florida. These results were relayed to Martin at Fermlab who then interpreted them, and provided the solution.**

Peripheral Crate HW Experts at Test Beam?

PERIPHERAL CRATE CONFIGURATION SOLUTION!

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