CSC Track-Finder HW/SW Update

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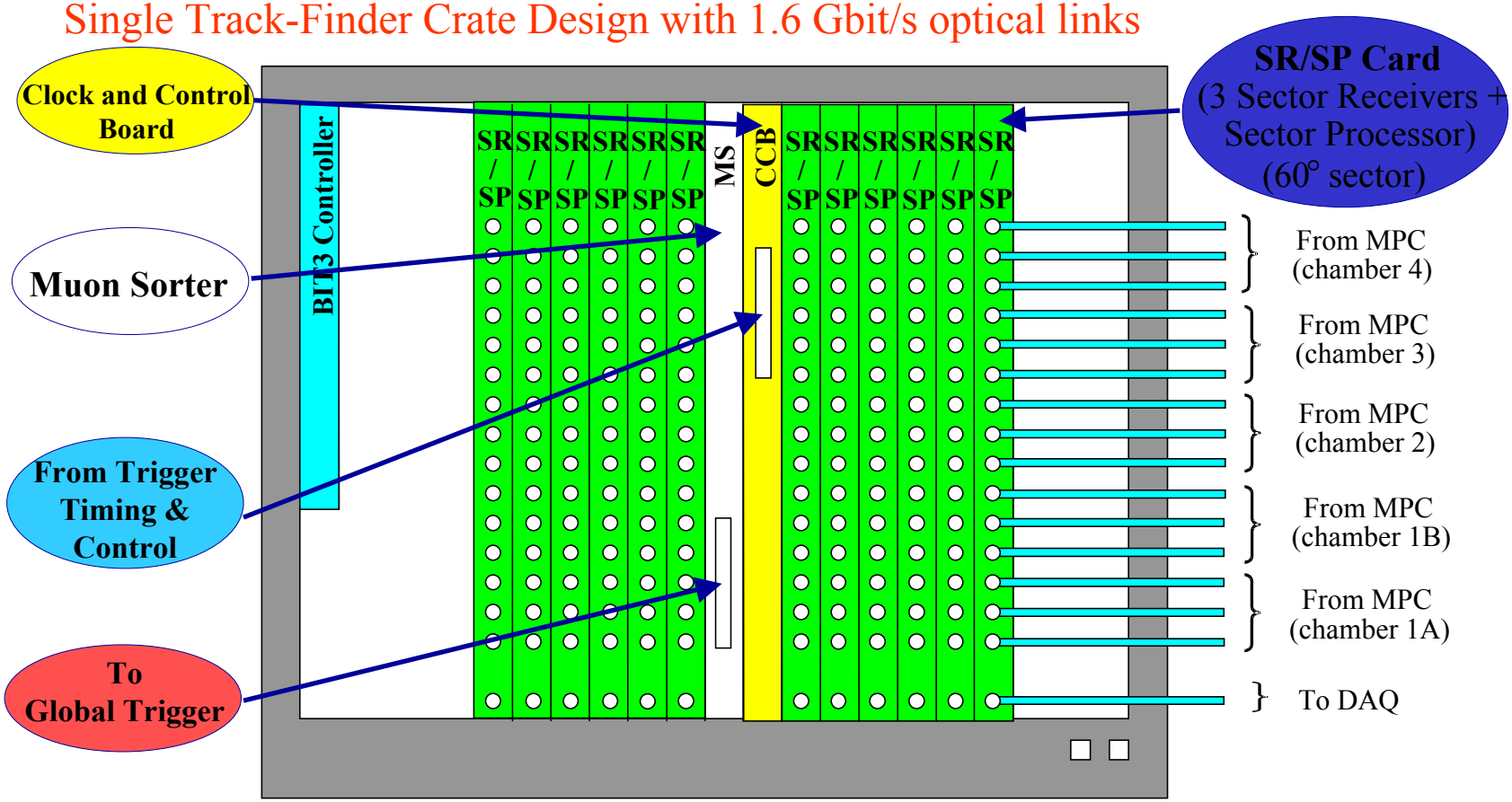
New Track-Finder Crate Design

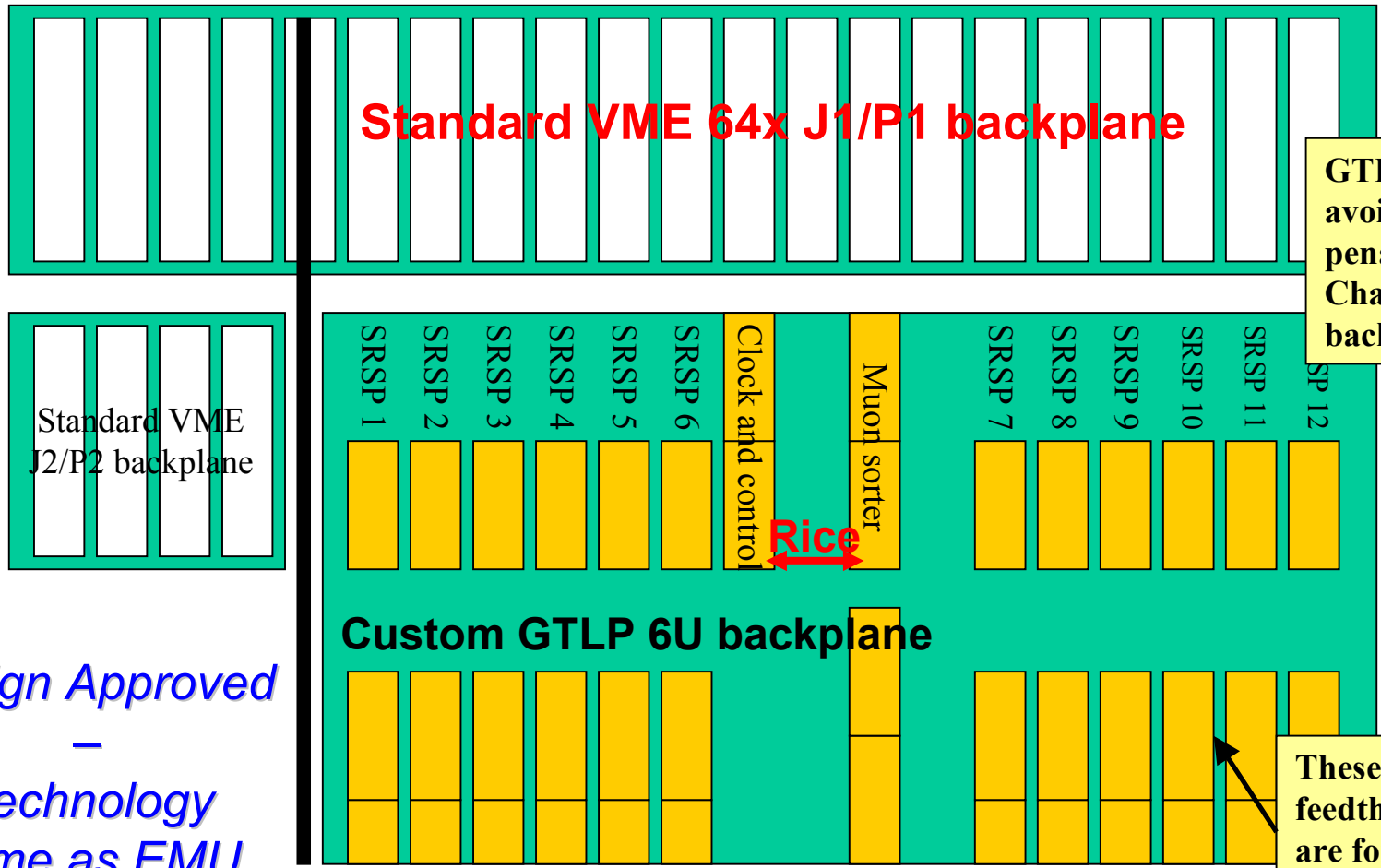
- Single Track-Finder Crate Design with 1.6 Gbit/s optical links



- Reduces SR/SP processing time from 21 bx (old design) to 7 bx
- Crate Power Consumption ~ 1000 W
- 16 Optical connections per SR/SP card
- Custom Backplane for SR/SP ⇔ CCB and MS connection

CSC Track Finder Backplane

Florida



GTLP backplane avoids latency penalty of previous Channel-Link backplane (~3BX)

Design Approved – Technology same as EMU peripheral crates

These SRSP feedthru connectors are for DT information exchange via transition board

DT-CSC Interface Specified

- **DT/CSC transition board pinout specified**
- **Connector pinout to DT/CSC transition board defined**
- **Would like to specify DT/CSC cable pinout**
- **CMS IN 2002/040 released**

Signal	Bits/stub	Bits/3 stubs	Bits/6 stubs	Description
ϕ	12	36	72	Azimuth coordinate
η	1	3	6	DT/CSC region flag
Quality	3	9	18	stub quality
BXN	–	2	4	2 LSB of BXN
BC0	–	1	2	bunch crossing 0
Clock	–	1	2	clock for data
Total:	16	52	104	

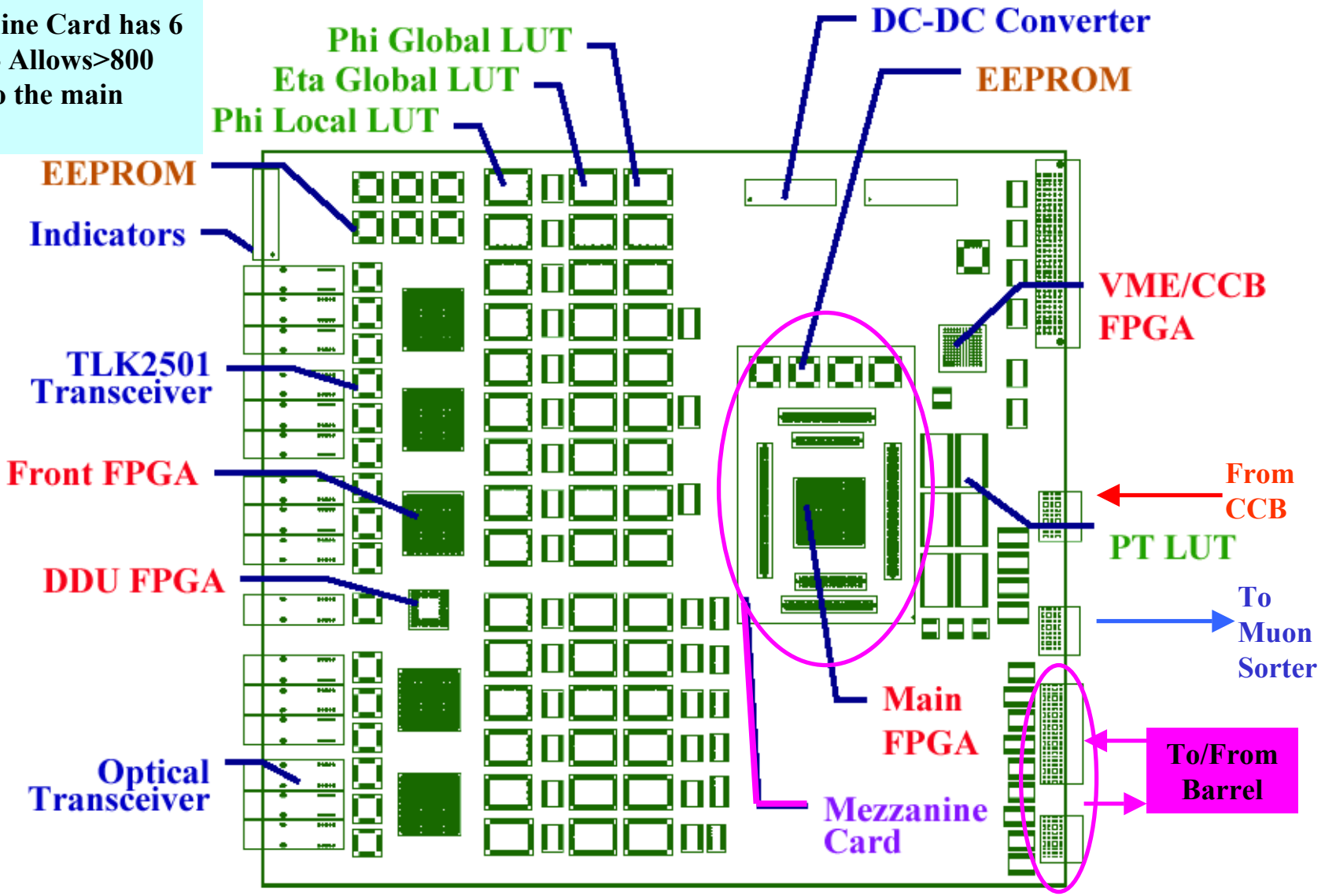
CSC TF→ DT TF

DT TF→ CSC TF

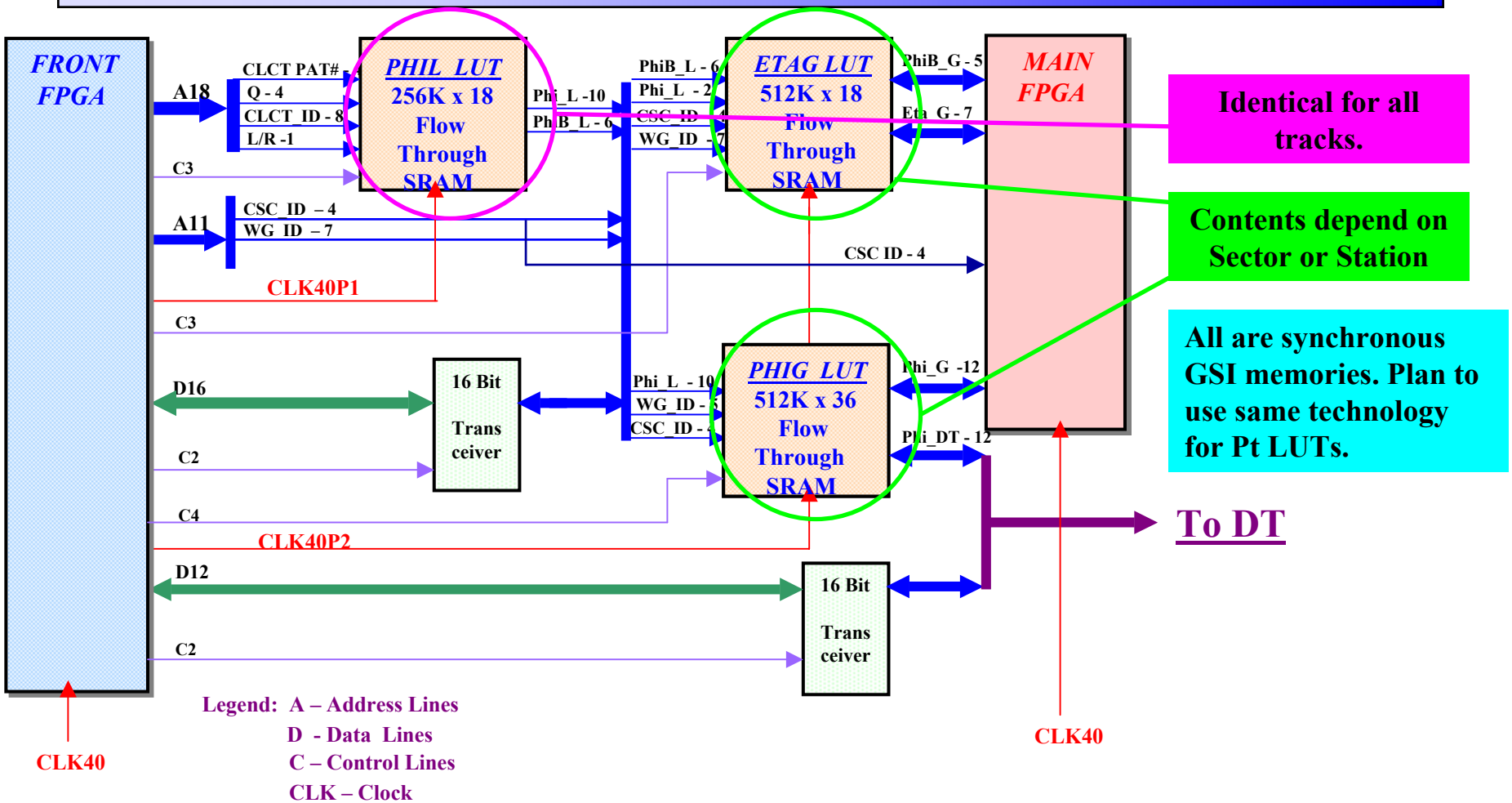
Signal	Bits/stub	Bits/2 stubs	Description
ϕ	12	24	Azimuth coordinate
ϕ_b	5	10	ϕ bend angle
Quality	3	6	stub quality
Muon Flag	1	2	2nd muon of previous BX
BXN	2	4	2 LSB of BXN
BC0	1	2	bunch crossing 0
Calib	1	2	data not valid
Clock	1	2	clock for data
Total:	26	52	

SR/SP 2002 Board Layout

New Mezzanine Card has 6 Connectors - Allows>800 I/O signals to the main FPGA



SR LUT Triad



Identical for all tracks.

Contents depend on Sector or Station

All are synchronous GSI memories. Plan to use same technology for Pt LUTs.

- SR now has 3 memories rather than 6 per stub [total of 45 per board]. Need to define their contents. LUTs are created in ORCA, but have yet to be tested.
- >64 MB per board ⇒ Need high VME bandwidth, broadcast capability to identical chips, and crate broadcast capability to SPs

SR/SP 2002 Design Status

- **Schematics Complete:**
  - **Sector Receiver Front FPGAs (5 total)**
    - **Choice: XC2V1000-FF896C with 432 user I/Os**
  - **Sector Processor Main FPGA**
    - **Choice: XC2V4000-FF1152C with 824 user I/Os**
    - **Placed on mezzanine card (design started)**
    - **Firmware written in "Verilog++", validated by simulation**
  - **VME & control interface FPGA**
    - **Choice: XC2V250-FG456C with 200 user I/Os**
  - **DAQ Interface FPGA**
    - **Choice: XC2V250-FG256C with 172 user I/Os**
  - **SRAM:**
    - **51 SRAM chips (>64MB) for Look-up functionality**
    - **May require BGA packages to allow more space for routing**
- **Layout to commence soon**
  - **Board will be dense! (Merger of 4 boards, but I/O ~same)**

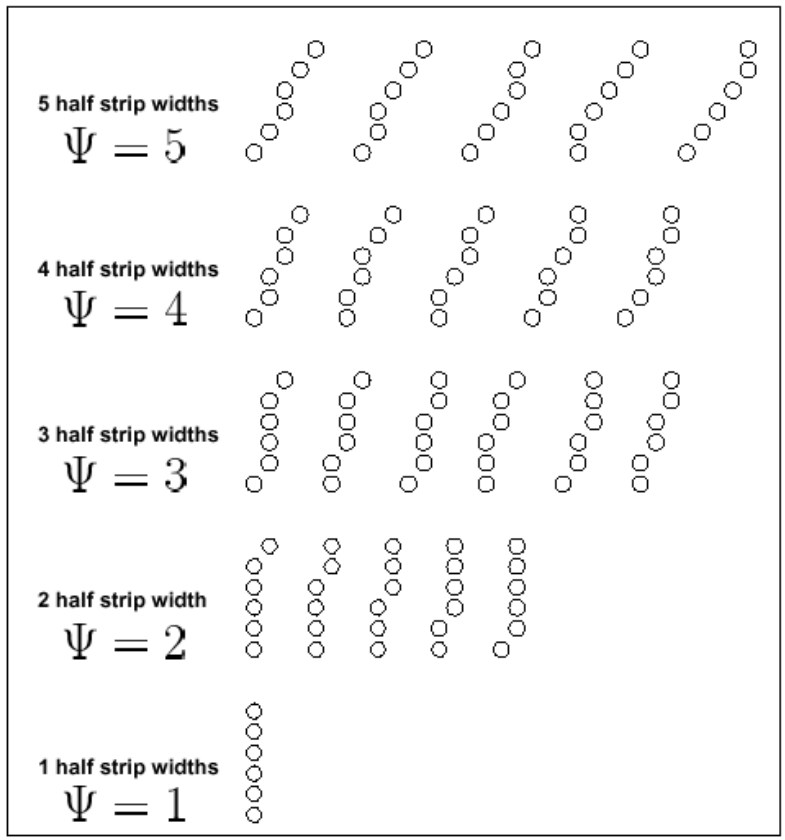
Software Update

- **Verilog++ SP model implemented and LUTs generated in ORCA.**
- **Also need to add Bunch Crossing Analyzer and Ghost Busting [background reduction] to Verilog++ model.**
- **Phi and Eta SR LUT Contents Have Been Specified in ORCA. [Thank You Slava Valouev!]**
- **Work underway to attach track-stub data to tracks in Verilog++ model and in DAQ (this will be useful for L2 Trigger).**

Software Update

- **Currently examining alternative bend patterns in CLCT Processor to improve ϕ resolution and Pt assignment.**

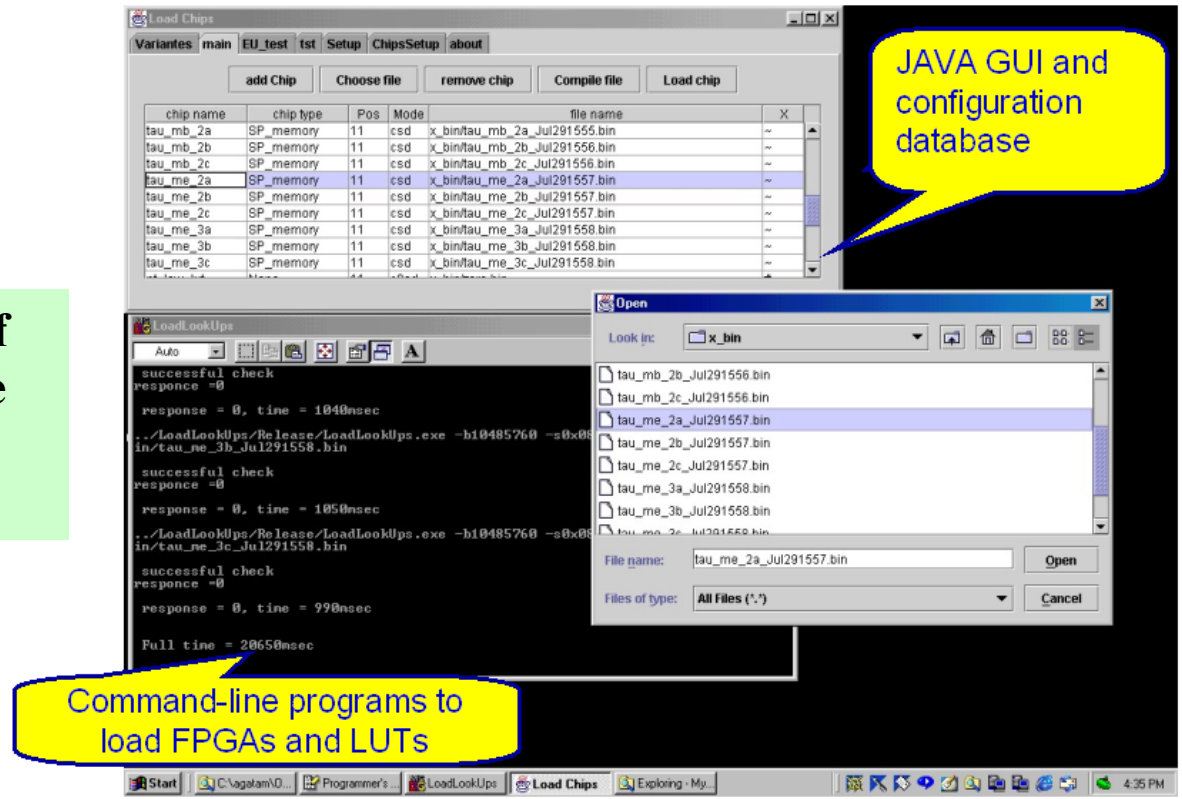
- **First attempt will be using patterns from CMSIM100 $\Rightarrow$ Bend value based only on the number of strips extended. For example:**



Test Software Update

We have started working on integrating software written for the 2000 TF crate tests into the XDAQ environment.

Screen shot of the Hardware configuration GUI.



Schedule

- November 2002: expect to finish the SP protoype. Will conduct single board tests
- MPC→SR/SP tests will continue through to 4/30/03.
- 5/1/03 to 9/30/03: Plan chain tests with CSC chambers and front-end electronics using cosmic rays and test beam.
- Also plan to do DT↔CSC tests sometime after May 1 2003.

Conclusions

- CSC TF Backplane Specified
- DT-CSC Interface Specified
- SR/SP Schematics Complete
- SR/SP Layout Started
- SR LUT Generation Completed in ORCA
- More Additions Scheduled for Verilog++ SP Model
- Work on ϕ_b Definition in Progress