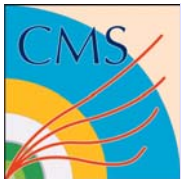


CSC Track-Finder Report

**Beam Test Results, Testing Plans,
Production Plans, Milestones**

**Darin Acosta
University of Florida**

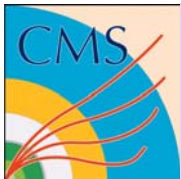


The Level-1 *Filter*

**Note: We should rename our project
(at least in the U.S.)**

**“Trigger” has politically incorrect
connotations, and can lead to a visit
from the F.B.I. to check on what you are
doing...**

**So, the Track-Finder should be
considered a part of the CMS Level-1
Filter electronics**

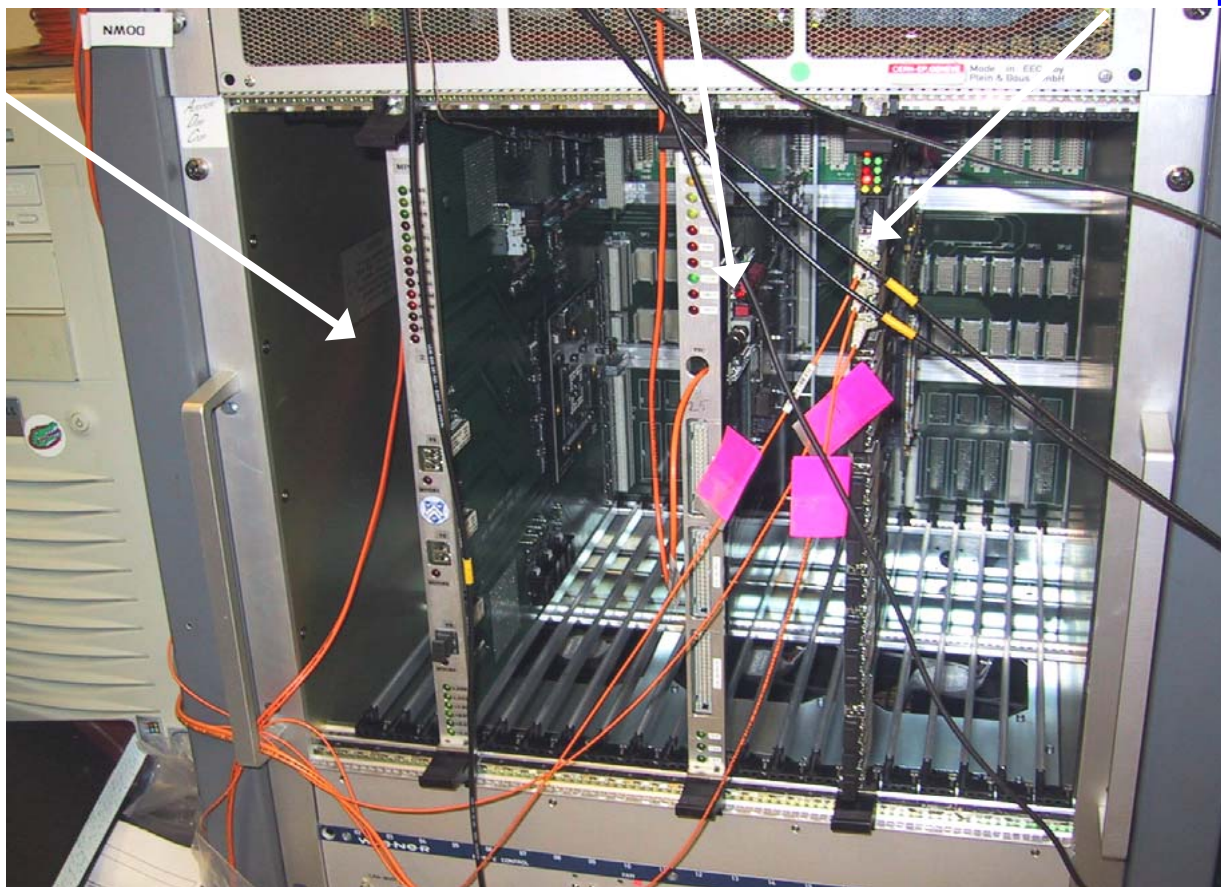


CSC Track-Finder Crate

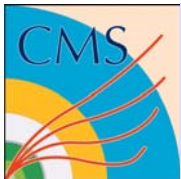
MPC, for
in-crate
tests

CCB with TTCRx

Sector Processor,
receives optical data



Second generation prototypes tested at beam test



CSC Track-Finder (SP) Trigger*

Test 3 x 1.6 Gb/s optical link connections from CSC electronics

Uses TLK2501 chipset from TI

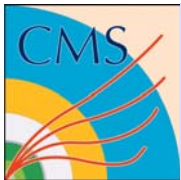
Requires very stable reference clock for error-free operation

Errors during May tests without PLL

Home-built VCXO & PLL clock patch added to clean incoming TTC clock for links, but TTC QPLL also tested



* Filter



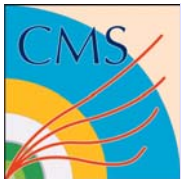
Data-taking Mode

Most data logged using two independent DAQ systems:

- “CFEB Control” for CSC detector data and front-end trigger
- “SP DAQ” for Track-Finder data (standalone SP readout)
 - SP records **5 BX** of input data for each L1A, with most trigger data arriving on central BX
 - Allows study of time-dependence of trigger data

XDAQ-based event builder also able to log data

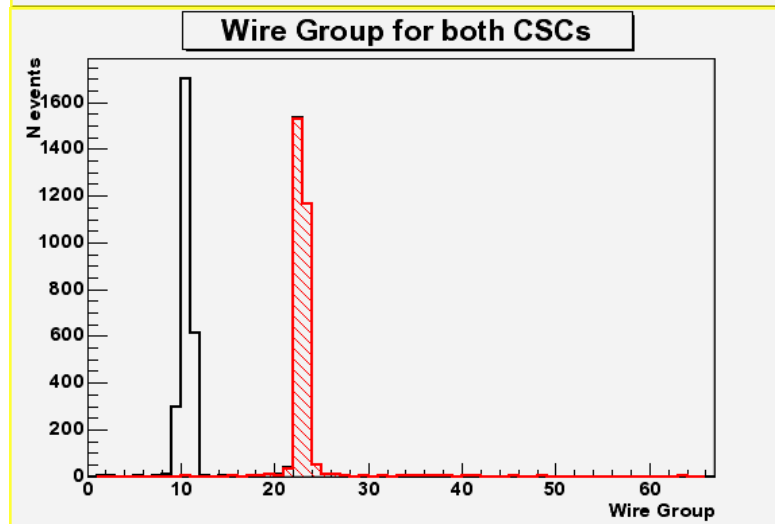
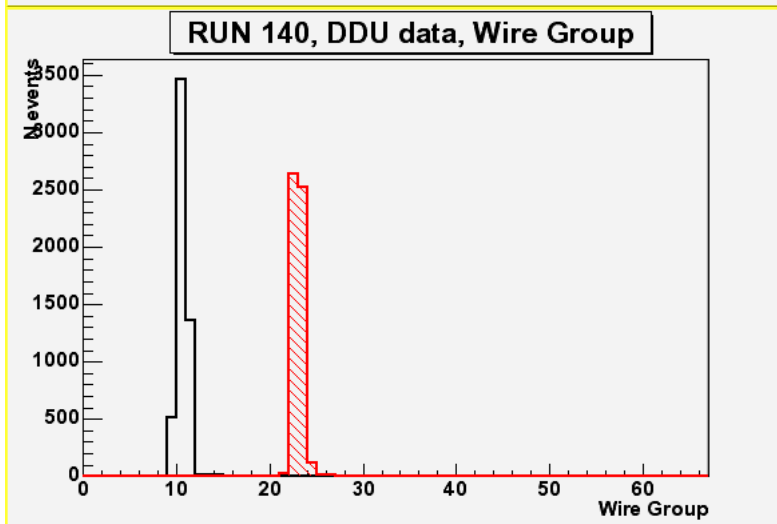
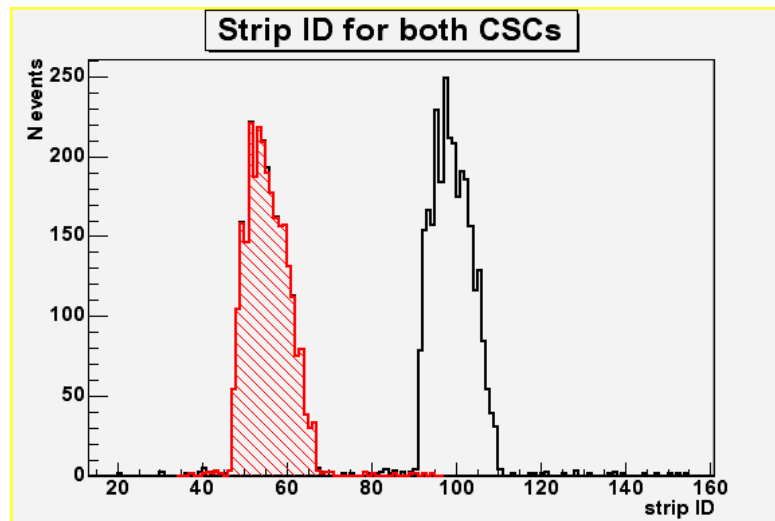
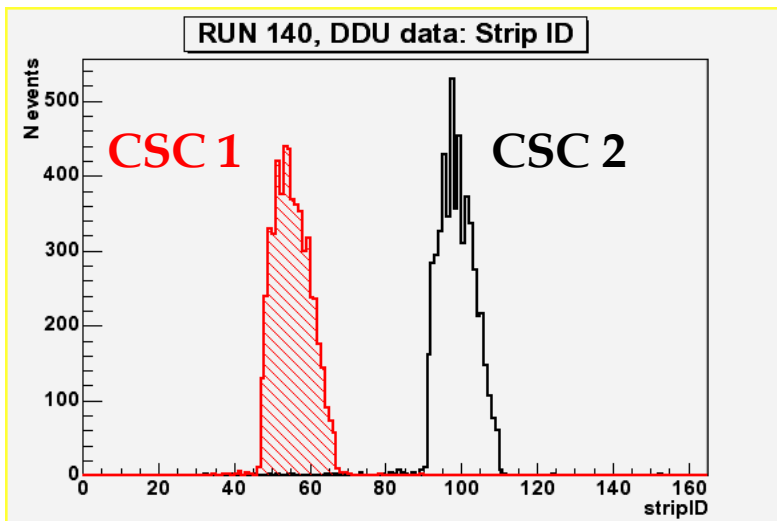
- Underlying SP code the same as for standalone DAQ since it was written using XDAQ
- All analysis of SP and DDU data from either DAQ system is done using the XDAQ-based software

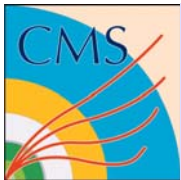


Data Comparison

CSC Data from DAQ

CSC Track-Finder Data





Detailed TMB–SP Comparison

Run TMB data (correlated LCT trigger primitives) through MPC simulation to compare with SP

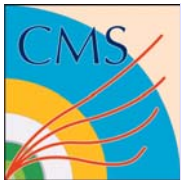
- MPC is not directly read out
- MPC sorts possible 4 LCTs to 3 in beam test data
- Use BXN reported by ALCT for each LCT

Preliminary comparison between SP and TMB for all 5 BX read out by SP for every L1A match:

- 99.7% agreement for ~70K events

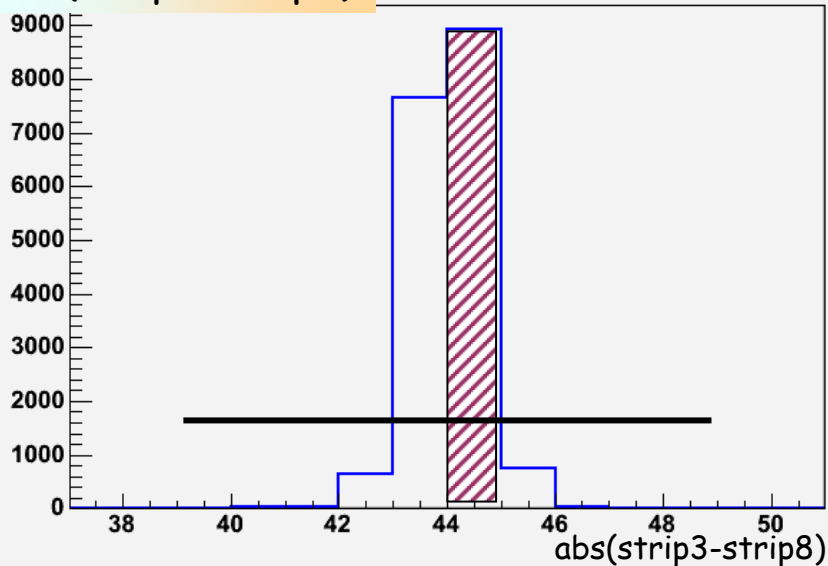
Mismatches between TMB and SP data are in BX assignment only, *not* in LCT frames

- More detailed checks will continue

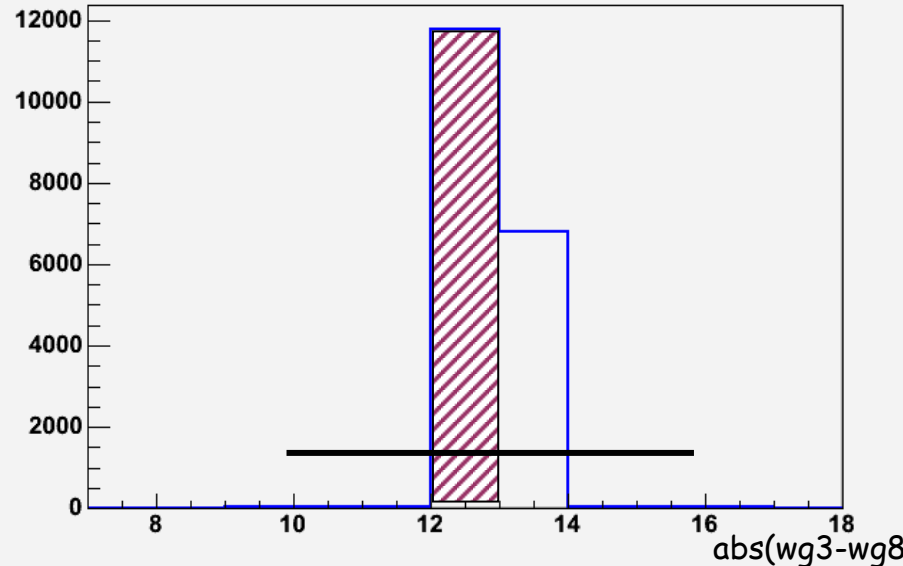


Correlated LCT Efficiency

abs(strip3-strip8)



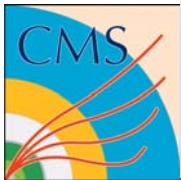
abs(wg3-wg8)



The efficiency to identify a correlated LCT (ALCT+CLCT) in one csc in a straight-line path from an LCT found in the other csc (within a ± 5 strip and ± 3 WG tolerance) is:

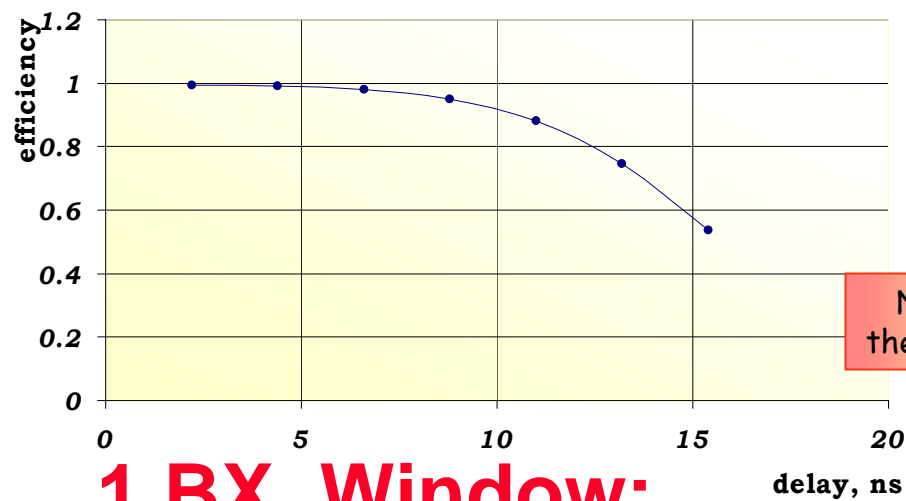
- 97.9% in one BX
- 98.9% in two BX (correct BX or one after)
- 99.1% in three BX (correct BX ± 1)

as determined from logged Track-Finder data



Correlated LCT Efficiency: timing

Efficiency for the middle BX (BX#2) vs. ALCT delay time (for CSC#8)



Note the scale

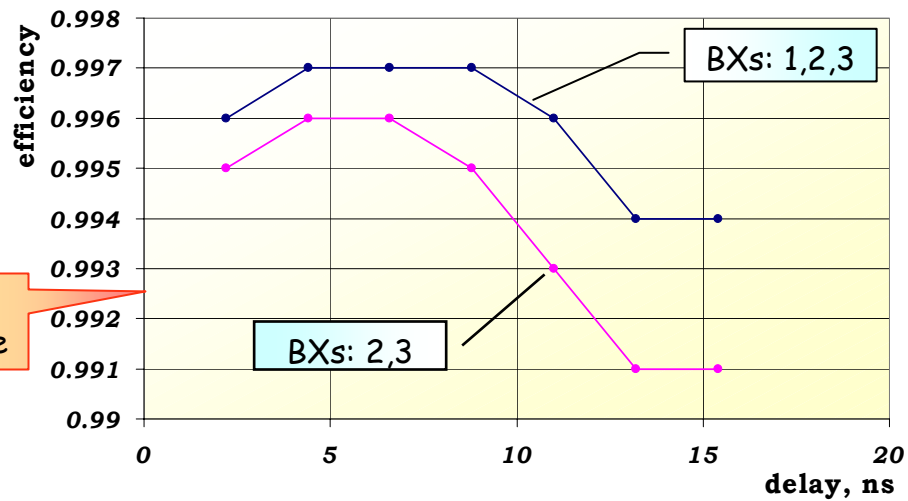
1 BX Window:

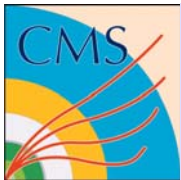
- Efficiency sensitive to ALCT delay (~5ns window)

Multi-BX Window:

- Efficiency very close to 100%
- Less sensitive to exact ALCT timing
- No spatial requirement on shown efficiencies

Efficiency for multi-BXs vs ALCT delay time (for CSC#8)





CSC Trigger Latency

Measured with scope during the beam tests:

- From CSC to MPC input: 32 bx (± 1 bx)
- From the CSC to SR/SP input:
(includes 100 m fiber, 18 bx delay) 57 bx

Estimated latency for output of SP:

- Add 10 bx for SR/SP processing: 67 bx

Estimated latency for output of Muon Sorter:

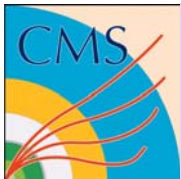
- Add 7 bx for backplane + sorting: 74 bx

Total compares well with 74.5 bx projected in TDR
(Latter includes 1 bx TOF delay)

Expect to save additional ~7 bx with Virtex-2 TMB

Estimated latency to send CSC data to DT TF:

- 57bx + 4bx for SR + 2bx cable + 1bx TOF: 64 bx – 7 bx = 57 bx
- Nearly aligned with DT data at DT TF: 54 bx according to TDR
- At what bx will CSC TF receive DT data?



SP Tests Completed

MPC→SP optical link tests

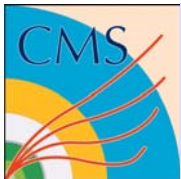
- Demonstrated to work in April in single crate using crystal-oscillator clock (~1 error/hour)

Optical Link tests with TTC

- Demonstrated to work error-free during September beam test with home-built PLL+VCXO and with latest QPLL (TTCRq)

DT/CSC Data Exchange Test

- Demonstrated to work during September in both directions, with only a few minor problems with swapped bits, connectors, and dead chips
- Repeat with longer cables and Track-Finding tests
- See talk by J.Ero



Remaining SP Tests

SP ↔ Muon Sorter, Part 1, 10/20/03 – 12/1/03

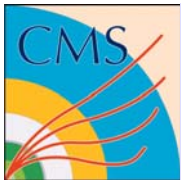
- Verification of data transmission from SP FIFO to MS FIFO through backplane at 80 MHz, including read-back of MS winner bits
- PT LUTs bypassed
- Status: SP output verified, sent to Rice for tests
- Also important to verify SP communication from all possible SP slots! (tests backplane and mezzanine card I/O)

SP Track-Finding Logic Test, 11/3/03 – 1/5/04

- Verification of TF logic on SP mezz. card with C++ model
- Input and output FIFOs on same mezz. card
- Status: need to finalize firmware and prepare software

SR LUT Test, 11/10/03 – 1/5/04

- Verification of the reading & writing to SR LUTs on SP main board and validation of 40 MHz performance



Remaining SP Tests Cont'd

PT LUT Test, 12/1/03 – 1/5/04

- Verification of the reading & writing to PT LUTs on SP main board and validation of 40 MHz performance

Complete SP functionality test, 1/5/04 – 1/19/04

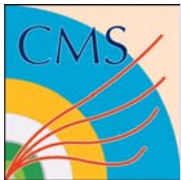
- “Chain test” of all onboard SP logic: Front FPGAs, SR LUTs, SP logic, PT LUT, with comparison against simulation

SP ↔ Muon Sorter, Part 2, 1/19/04 – 2/2/04

- Repeat of verification of data transmission from SP FIFO to MS FIFO with PT LUTs included

SP ↔ DDU (CSC DAQ board) Tests, Part 1, 2/2/04 – ?

- Probably will be postponed because DDU design is changing and because of the significant firmware changes required on DDU board



Other Interesting Tests

Multiple MPC \leftrightarrow SP Test

- Could be done any time we have several MPC's in TF crate
- Verify correct synchronization between multiple boards (even better would be to have several peripheral crates...)

SP \leftrightarrow SP Test

- Stress-test of all 15 trigger links on SP: one SP as data-generator and one SP in normal mode
- Could be done anytime

Multiple SP \leftrightarrow MS Test

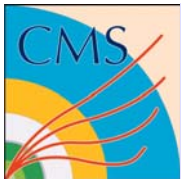
- Verify correct transmission, timing, and read-back from multiple sources
- Could be done once single SP \leftrightarrow MS test validated

Cosmic-Ray and Beam Tests (2004)

- Complete chain-test with detectors and fully functioning SP and MS
- Demonstrate self-triggering

DT/CSC Integration test, Part 2

- Demonstrate track-finding with exchanged data



Production and Test Plans

Will assemble 1 board first as pre-production prototype and test before launching full production (12 SR/SP + 3 spare)

- Not likely to occur before Trigger ESR in May'04, though

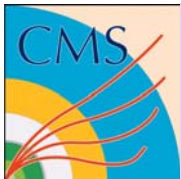
Each of the prototype tests (optical link PRBS tests, LUT tests, etc.) will become standard tests for the production modules

- Therefore, we will have a suite of tests in our XDAQ-based software (hopefully with a JAVA interface)
- Initial testing will be performed by a technician or student
- Encountered problems will be addressed by our engineers

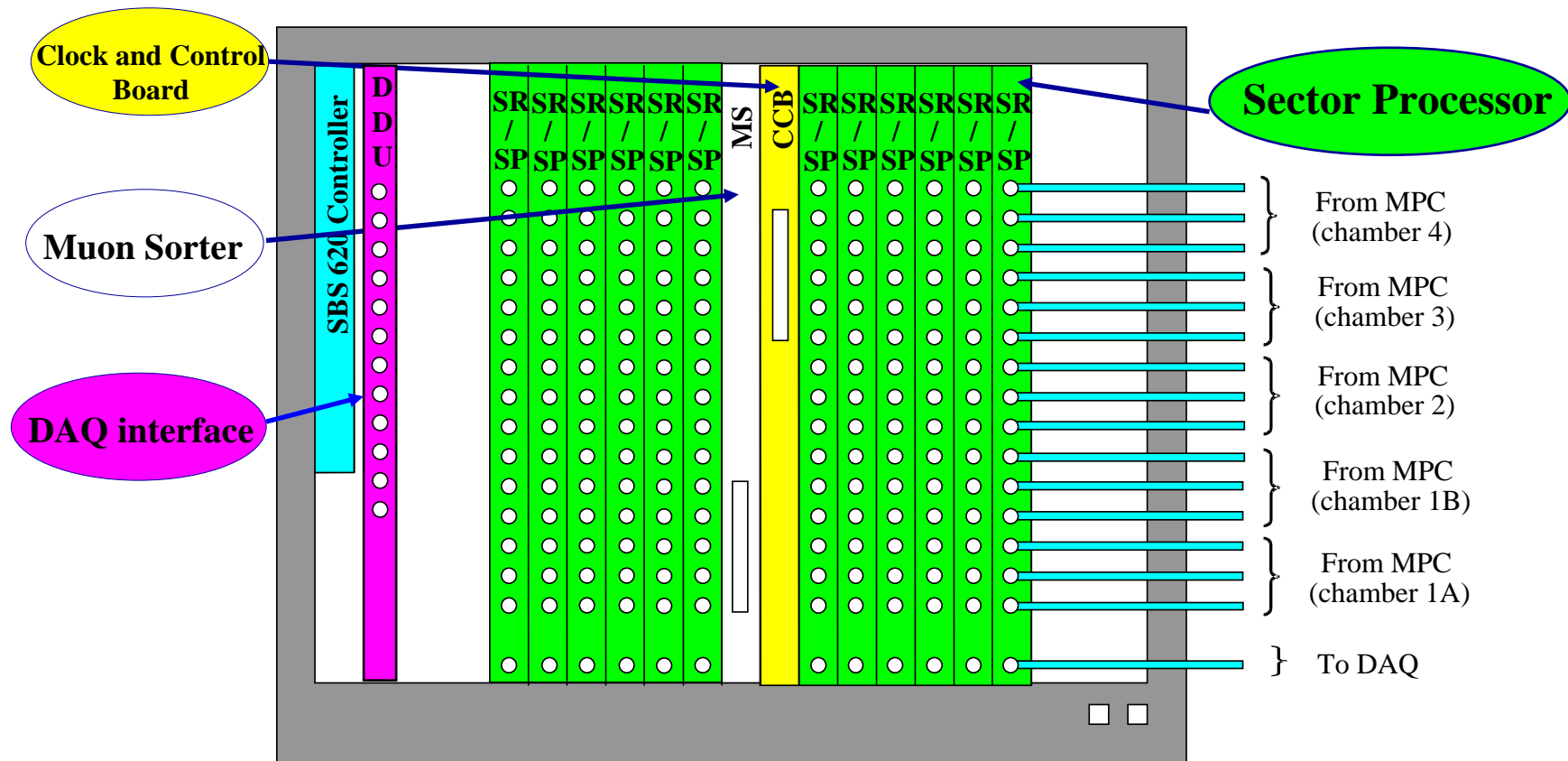


CSC Track-Finder Milestones

- TF Backplane Proto tested Sep-02 **Delay: Dec-03**
- SR/SP Prototype tested Mar-03 **Delay: Feb-04**
- TF Backplane Prodn started Jul-04
- SR/SP Production started Jul-04
- TF Backplane Prodn done Mar-04 **Delay: Jan-05**
- SR/SP Production done Jun-04 **Delay: Jan-05**

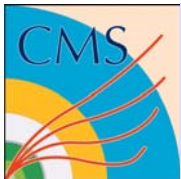


CSC Track-Finder Crate Layout



**Front-panel: 12x16 (SP) + 12 (DDU) + 1 (TTC) optical link inputs
4 LVDS SCSI connectors output (MS)**

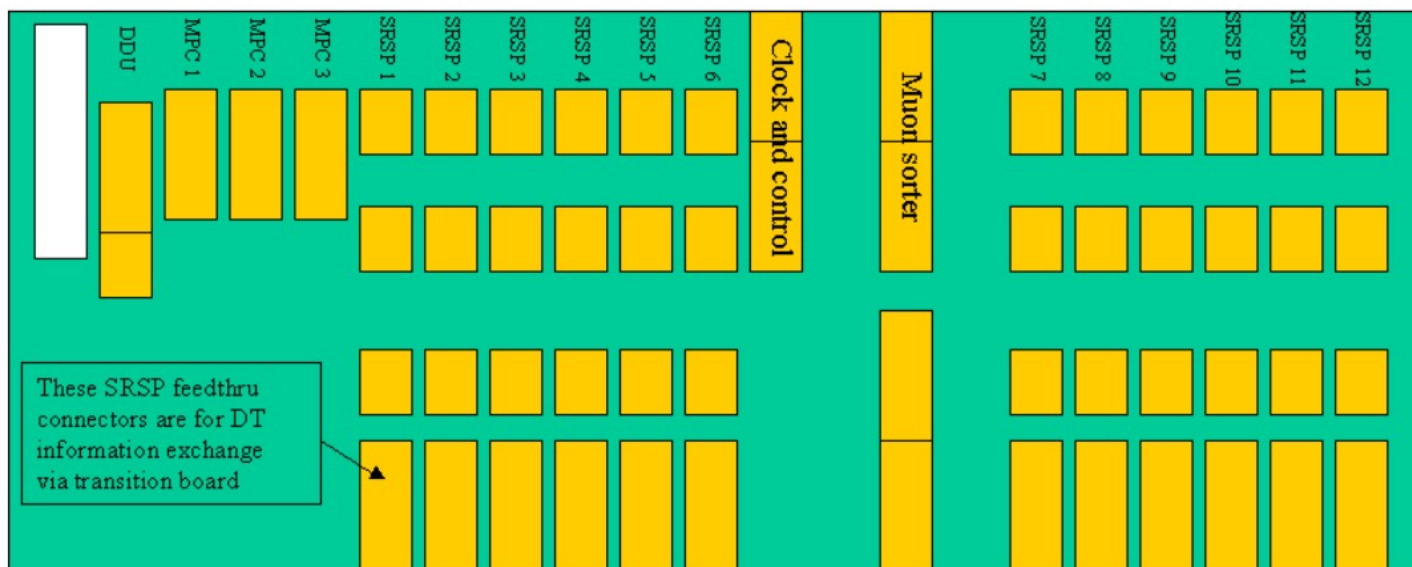
Back-plane (trans. cards): 12x6 SCSI connectors (SP) to/from DT



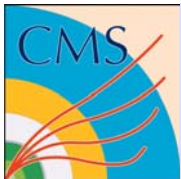
VME and Custom Backplane



Custom GTLP backplane



- Standard 9U VME crate and power (including 3.3V)

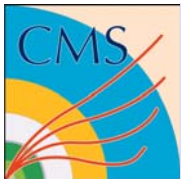


CSC Track-Finder Rack Layout

In principle, the entire CSC Track-Finder fits into one rack (one crate)

Should be close to DT Track-Finder and Global Trigger:

Lower	Floor	(Zone S1)		
	D	E	F	G
	TK. FEC	Opt.Cpl.	Presh. FEC	DT/RO/SC
OB	TK. FEC	TTC	DT TrkFnd	Pixel FEC
OB	RPC Trig	TTC	DT TrkFnd	Pixel FED
OB	RPC Trig	Global	DT TrkFnd	Pixel FED
	%RPC Trig	%Cal Global	CSC TrkFnd	DAQ
	RPC Trig	TTS	CSC TrkFnd	CSC FED
	RPC Trig	TTS	DAQ#	CSC FED
C+#	RPC Trig	BPTX	RPC E+ HV#	CSC FED



Conclusions

CSC beam test with Track-Finder was a success!

- Complete electronic chain test of synchronous data transmission from CSC front-end electronics to the Track-Finder
- Latest QPLL design from CERN tested and works

Initial tests show that DT and CSC Track-Finders can exchange data

- A few minor problems on both ends with swapped bits, connectors, and dead chips

Remaining Track-Finder tests underway

- Some delay, but production should complete in early 2005