Sector Processor Status Report

Status of Tests	– Acosta
Schedule	– Acosta
SP Latency	– Uvarov
Design changes	– Uvarov
DT/CSC transition card	– Uvarov
Status of cosmic ray test stand	– Stoeck
Simulation results	– Drozdetski
Track-Finder GUI	– Gray

SP Tests Completed

MPC→SP optical link tests

- ➔ Demonstrated to work April '03 in single crate using crystal-oscillator clock (~1 error/hour)

Optical Link tests with TTC

- ➔ Demonstrated to work error-free during September beam test with home-built PLL+VCXO and with latest QPLL (TTCRq)
- ➔ No errors

DT/CSC Data Exchange Test

- ➔ Demonstrated to work during September in both directions, with only a few minor problems with swapped bits (DT TF), connectors, and dead chips
- ➔ Repeat with longer cables, new transition card (see Golovtsov's talk) and add Track-Finding tests

Recently Completed SP Tests

LUT Tests (SR and PT LUTs)

Uvarov, Stoeck

- Validated loading and read-back of all 45 SR LUTs using random numbers and simulated muon LUT files
  - Multicast writing to all 15 Local Phi LUTs simultaneously, as well as Global Phi and Global Eta triplet LUTs
  - Caught pin assignment error on mezzanine card layout, fixed in firmware
- Validated loading and read-back of 3 PT LUTs using random numbers and simulated Pt LUT file
  - Good news, since we had to procure entire production order to get chips
- Tested real-time access of memory
  - Address data loaded on just 1 BX

Recently Completed SP Tests

SP Track-Finding Logic Test

Madorsky, Scurlock, Acosta

- **Validated SP track-finding logic**
  - Downloaded random data and simulated muon data into 512 BX input FIFO, read-back and compare output FIFO
  - No discrepancies in 1.2M random events
  - No discrepancies in 13K single muon events, or 4K triple muon events (3 single muons piled up)
  - Validation period much faster than for first prototype since firmware and model are written with same piece of code
- **Validated Verilog model against original C++ model**
  - Some bugs found in original model!
  - Some residual discrepancies observed for high multiplicity events
    - Differences in sorting for tracks in DT/CSC overlap (understood)
  - Ghost-busting in ME1 improved
    - Was partially working (only for ME1-ME2 tracks). Now corrected.
  - Bunch-crossing analyzer is still under study/development
    - Not even in original model
  - Everything will be propagated to full ORCA, drop old model.

Remaining SP Tests

Sector Processor ↔ Muon Sorter

- ➔ Awaiting test results from Rice
- ➔ Can now test SP with PT LUT and multiplexer installed

Complete SP functionality test

- ➔ "Chain test" of all onboard SP logic: Front FPGAs, SR LUTs, SP logic, PT LUT, with comparison against simulation
- ➔ Scheduled to take place this January

VME block transfer

- ➔ Will decrease time to load LUTs

VME crate multicast

- ➔ Load LUTs on multiple SP's in crate at same time

DDU FPGA bus validation

- ➔ Collect all SR input data and SP output data into FIFO in DDU FPGA (but still read out through VME)
- ➔ Needed for June'04 beam test
- ➔ Integration tests with redesigned DDU to occur after OSU completes next prototype

Other Interesting Tests

Multiple MPC ↔ SP Test

- ➔ Could be done any time we have several MPC's in TF crate
- ➔ Verify correct synchronization between multiple boards (even better would be to have several peripheral crates…)

SP ↔ SP Test

- ➔ Stress-test of all 15 trigger links on SP: one SP as data-generator and one SP in normal mode
- ➔ Could be done anytime

Multiple SP ↔ MS Test

- ➔ Verify correct transmission, timing, and read-back from multiple sources
- ➔ Could be done once single SP ↔ MS test validated

Cosmic-Ray and Beam Tests

- ➔ Complete chain-test with detectors and fully operational SP
- ➔ Demonstrate self-triggering with tracks in multiple CSC's
- ➔ Needed for June'04 beam tests

Sector Processor Schedule

Completion of SP board tests: **Feb ’04**

Completion of major production design changes: **May ’04**

- ➔ **Lev at UF**

Completion of redesigned DT/CSC card: **May ’04**

- ➔ **Victor at UF**

Firmware changes for beam test: **June ’04**

2004 beam test: **June ’04**

Second DT/CSC test (?) **June ‘04**

Start of production: **Sept ’04**

- ➔ **Lev at UF**

Completion of production and board tests: **Mar ‘05**

Documentation

General information and links:

- ➔ http://www.phys.ufl.edu/~acosta/cms/trigger.html

Lev's page on SP02 design specification

- ➔http://www.phys.ufl.edu/~uvarov/sp_spec/SP02_spec.htm

Specification of SP02 registers and VME/CCB interfaces:

- ➔ http://www.phys.ufl.edu/~uvarov/sp_spec/LU-SP02_Backplane_Interfaces_031210.pdf
- ➔ http://www.phys.ufl.edu/~uvarov/sp_spec/LU-SP02_Backplane_Interfaces_030901.pdf

Specification of main SP02 FPGA VME interface:

- ➔ http://www.phys.ufl.edu/~madorsky/sp/Main%20FPGA%20VME%20interface.doc