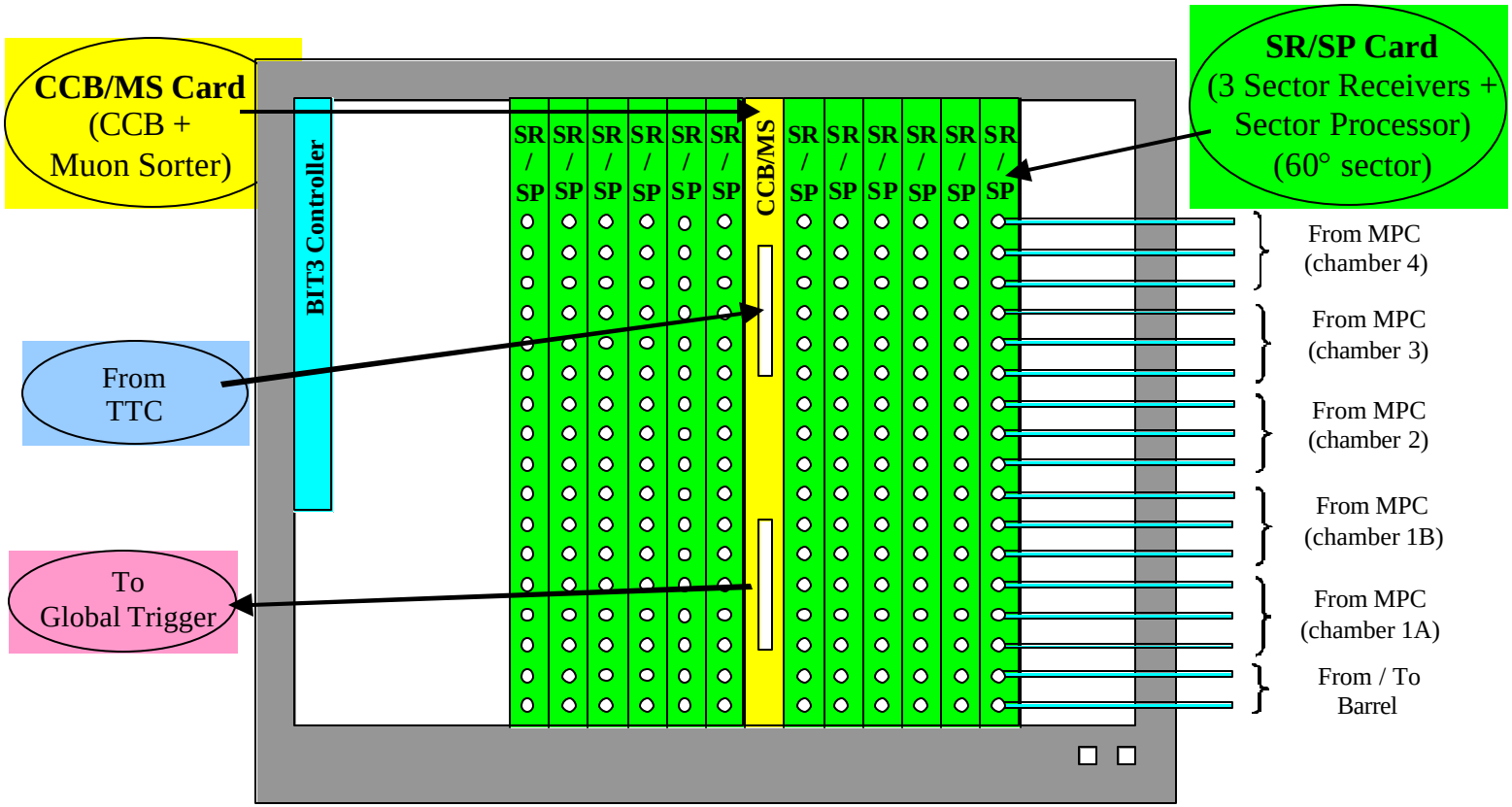
Conceptual Design for SR/SP

Topics:

- Board Layout
- Bit counts and data serialization
- Memory architecture (PNPI)
- SP to Verilog Translation (Madorsky)
- DDU plans

Possible Single Crate Solution

Track-Finder crate (1.6 Gbits/s optical links)

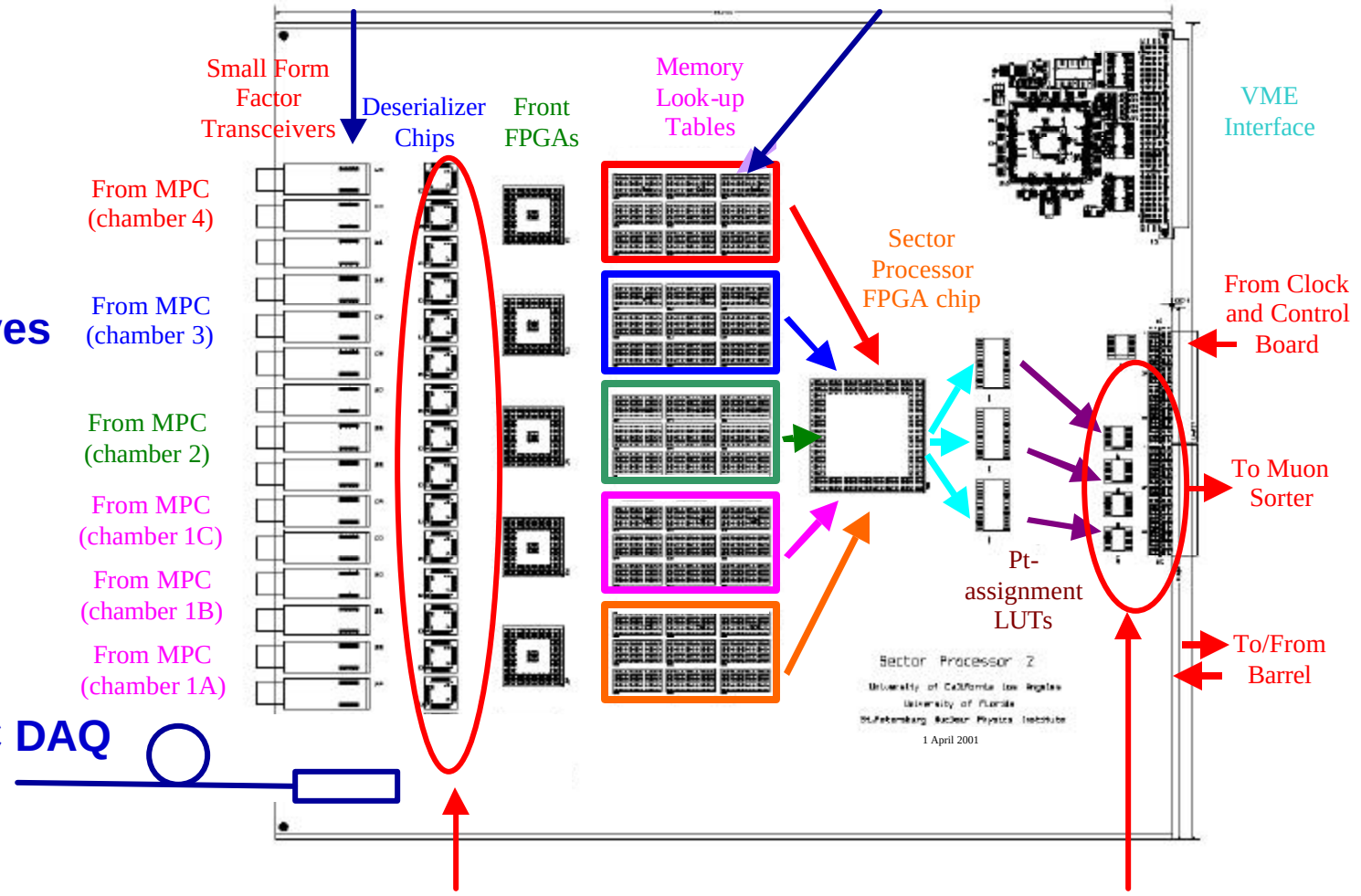


- **Total latency: ~ 20Bx (from input of SR/SP card to output of CCB/MS card)**
- **Power consumption: ~ 500W per crate**
- **15 optical connections per SR/SP card**
- **Custom backplane for SR/SPs < > CCB/MS connection**

Merged SR/SP

15 trigger links, 1 DAQ

45 SRAM



From trigger primitives

To CSC DAQ

Input: 528 bits/sector/b.x.

Output: 60 bits/sector/b.x.

Salient Features

Bi-Directional Optical Links

- ➔ Since we have both transmitters and receivers in the optical connection, this allows the option to send data as well as receive
- ➔ Makes testing much easier
  - One board sends data to other, or even itself through links

SR memory set for each muon stub

- ➔ No muon multiplexing means shortest latency

SP chip on a mezzanine board

- ➔ Decouples board development from FPGA technology
- ➔ Makes upgrades easier

DT fan-out on transition board

- ➔ Deliver all possibly needed signals to backplane connector
- ➔ Settle transmission technology, connector type, connector count on transition board at a later date

SR/SP Inputs

➔ **Muon Port Cards deliver 15 track stubs each BX via optical**

Sent on first frame

Signal	Bits / stub	Bits / 3 stubs (1 MPC)	Bits / 15 stubs (ME1–ME4)	Description
½ Strip *	8	24	120	½ strip label
CLCT pattern *	4	12	75	Pattern number without 4/6, 5/6, 6/6
L/R bend *	1	3	15	Sign bit for pattern
Quality *	3	9	45	Computed by TMB
Wire group	7	21	105	Wire group label
Accelerator m	1	3	15	Straight wire pattern
CSC i.d.	4	12	60	Chamber label in subsector
BXN	2	6	30	2 LSB of BXN
Valid pattern	1	3	15	Must be set for above to apply
Spare	1	3	15	
Total:	32	96	480	(240 bits at 80 MHz)

Reduced from 5

Needed for frame info

➔ **DT Track-Finder delivers 2 track stubs each BX via LVDS**

Signal	Bits / stub	Bits / 2 stubs (MB1: 60°)	Description
f	12	24	Azimuth coordinate
f_b	5	10	ϕ bend angle
Quality	3	6	Computed by TMB
BXN	2	4	2 LSB of BXN
Synch/Calib	1	2	DT Special Mode
Muon Flag	1	2	2nd muon of previous BX
Total:	24	48	

SR/SP Outputs

➔ **6 track stubs are delivered to DT Track-Finder each BX (delivered at 40 MHz to transition board)**

Signal	Bits / stub	Bits / 2 stubs (ME1: 20°)	Bits / 6 stubs (ME1: 60°)	Bits / 6 stubs @ 80 MHz	Description
f	12	24	72	36	Azimuth coordinate
h	1	2	6	3	DT/CSC region flag
Quality	3	6	18	9	Computed by TMB
BXN	–	2	6	3	2 LSB of BXN
	16	34	**102**	**51**	**Total**

➔ **3 muons per SP are delivered to Muon Sorter via GTLP backplane**

Sent on first frame

Signal	Bits / m	Bits / 3 m (1 SP)	Bits / 36 m (12 SP)	Description
f	5	15	180	Azimuth coordinate
h	5	15	180	Pseudorapidity
Rank *	7	21	252	5 bits p_T + 2 bits quality
Sign *	1	3	36	
BXN *	–	2	24	2 LSB of BXN
Error *	–	1	12	
Spare *	1	3	12	
Total:	19	60	**720**	**(360 bits at 80 MHz)**

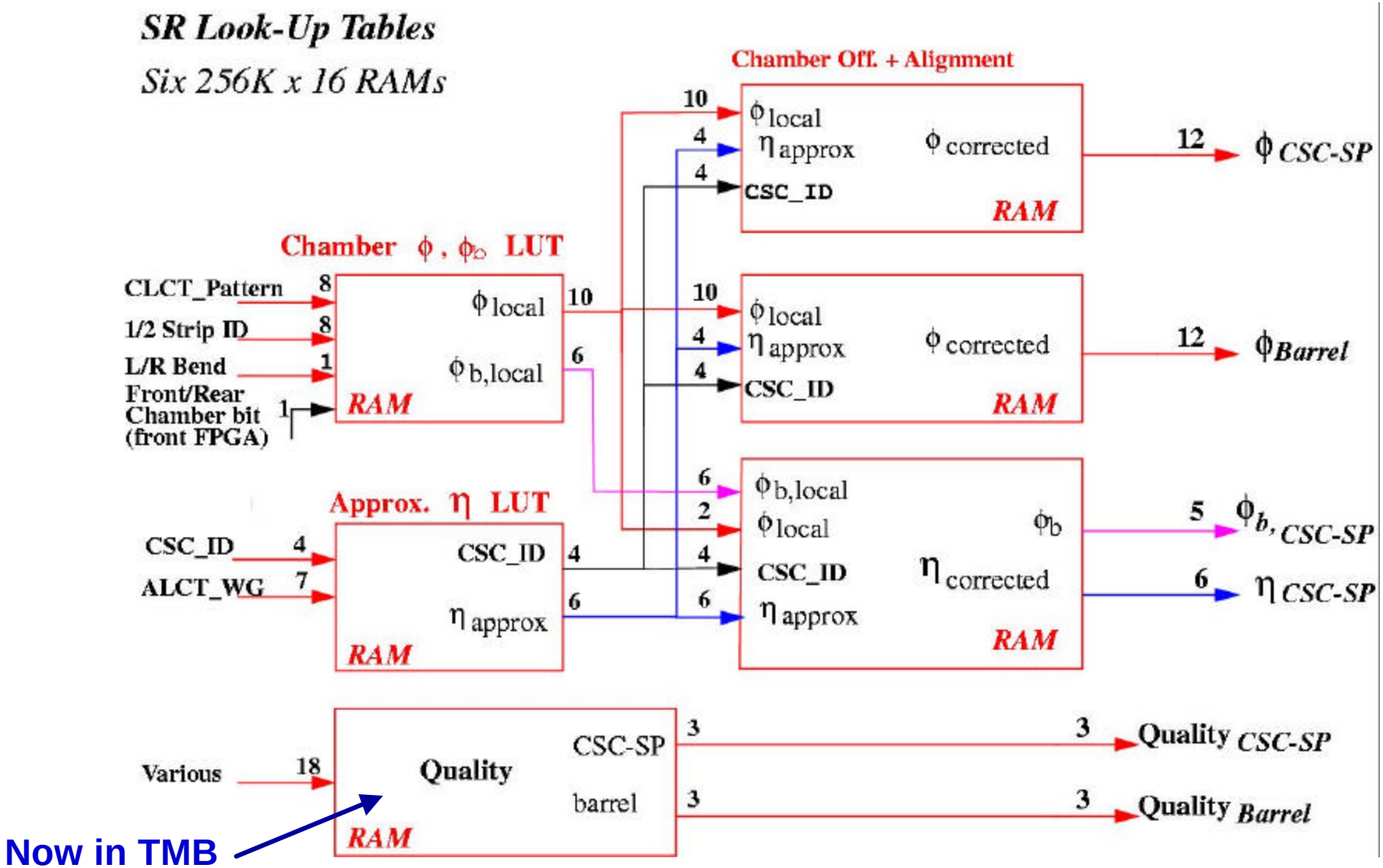
SR/SP Internal Dataflow

➔ **Data delivered from SR to SP**

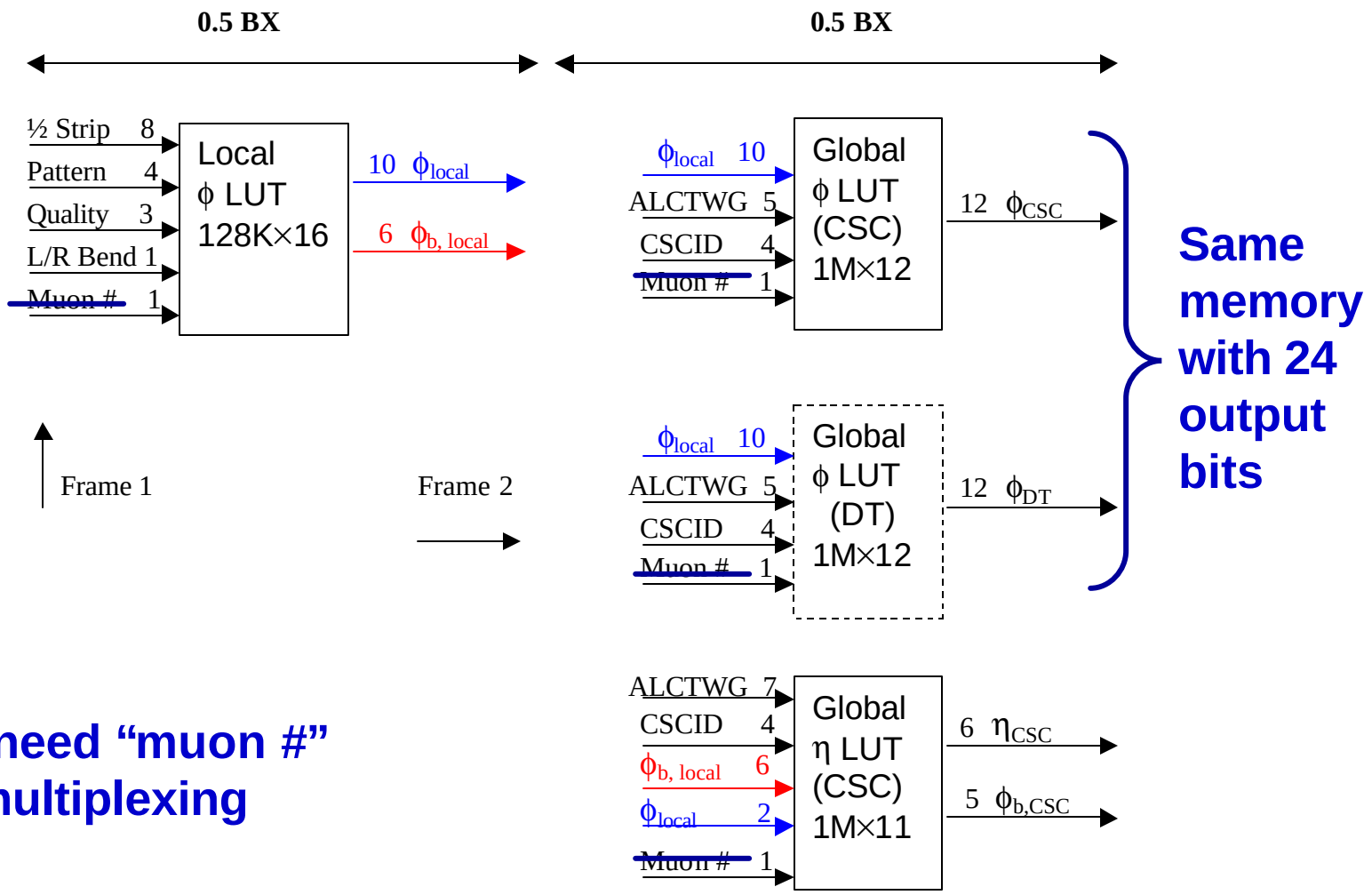
Signal	Bits / stub	Bits / 6 stubs (ME1)	Bits / 15 stubs (ME1–ME4)	Description
f	12	72	180	Azimuth coordinate
f_b	5	30	75	ϕ bend angle
h	6	36	90	Pseudorapidity
Accelerator m	1	6	15	η bend angle
Front/Rear *	1	6	6	ME1 chamber stagger
CSC ghost *	–	4	4	2 stubs in same ME1 CSC
Quality	3	18	45	Computed by TMB
Total:	28	172	**415**	~~(sent at 80 MHz)~~

ME1 only

Old SR Memory Scheme



New SR Memory Scheme



Don't need "muon #" if not multiplexing muons

Discussion of SR Memory (1)

Data Frames:

- Data arrives off links @ 80 MHz
- The proposed framing scheme implies no latency loss
  - First LUT operates on first frame only (but must reduce CLCT pattern label by 1 bit)
- This frame definition must be applied in the TMB where the data is generated and first serialized (i.e. before MPC) to avoid latency penalty

Memories:

- LUT for DT only applies to ME1
- Chip count is 3 per stub, down from 6 originally
- Increased memory size to 0.5M (okay for synch. SRAM)
- "Muon #" only applies if more than one stub in a BX is sent through same memory

Discussion of SR Memory (2)

One memory set per stub:

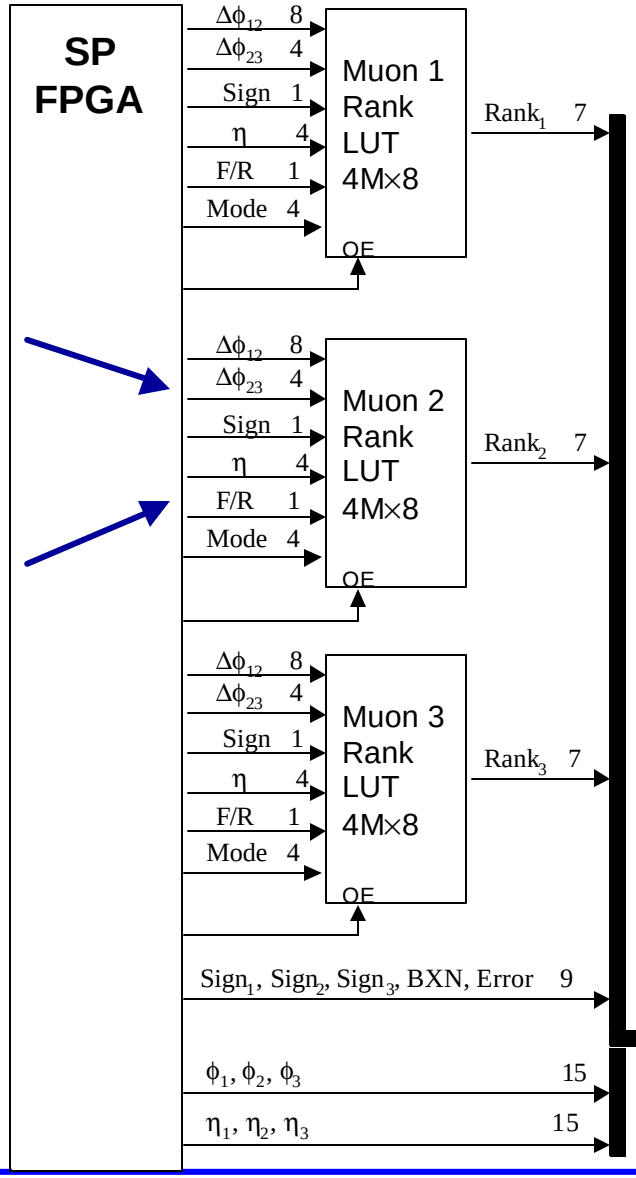
- ➔ **15´3 = 45 chips**
- ➔ **1 BX latency**
- ➔ **415 signals to SP**

First SR had 36 chips and 1 BX latency

Memory choices:

- ➔ **synch SRAM clocked at 160 MHz (tested to this frequency)**
- ➔ **Flow Through SRAM clocked at 80 MHz (see PNPI)**

SP Memory Scheme



Df_{23} could be replaced by f_b

Added F/R bit to improve P_T resolution

- Must serialize to fit data on backplane
- No latency penalty for serialization if Rank sent first to Muon Sorter
- SP FPGA contains tri-state buffers and generates enable for memories

Frame 1

30 GTLP backplane 80 MHz

Frame 2

SP to Verilog translation

What we said last time:

Will overhaul some of the SP software/firmware to facilitate changes to both

- ➔ Have SW algorithms match Verilog/Schematics better
- ➔ Have SW read same HW LUTs (it already generates them)

Plan to test next SP design even before construction!

- ➔ Add utilities to write ORCA data into Xilinx simulator format and to compare simulator output to ORCA
- ➔ Gives us a head start on validating logic design
- ➔ Will allow us to focus on HW debugging rather than SW debugging when testing the next prototype

This is now done! Latency: 12 ® 5 BX (See Madorsky)

CSC TF DAQ Plans

Send input of SR and output of SP to DAQ stream for diagnostics

Track-Finder DAQ acts as additional DDU for EMU system

- ➔ **Plan to use existing DDU design by OSU**
  - **OSU has decided to use T.I. Chip for serialization**
  - **12 SP fiber connections fits well into 15 planned for DDU**
  - **(Don't even need separate links as ours are bi-directional)**

Next step is to have Lev work with OSU (Jason Gilmore) to learn their design

- ➔ **Check bandwidth and buffer limitations**
- ➔ **Understand how to format our data**
- ➔ **Design buffers and readout on SR/SP**

Mirror CSC DAQ Path