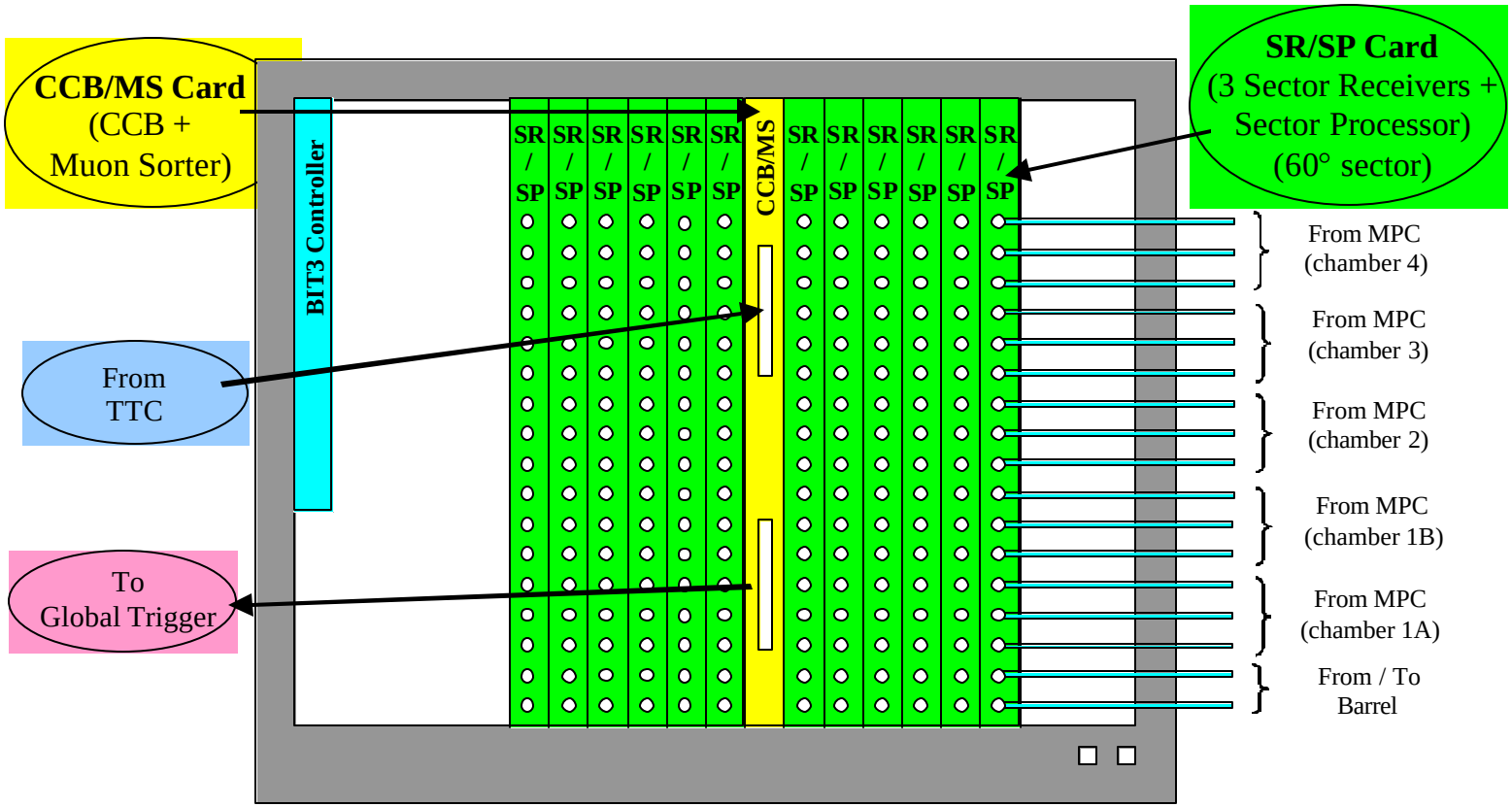
# Conceptual Design for SR/SP

## Topics:

- Board Layout
- Bit counts and data serialization
- Memory architecture
- SP-in-a-chip
- Backplane
- DAQ interface
- Manpower
- Software limitations

# Possible Single Crate Solution

**Track-Finder crate (1.6 Gbits/s optical links)**



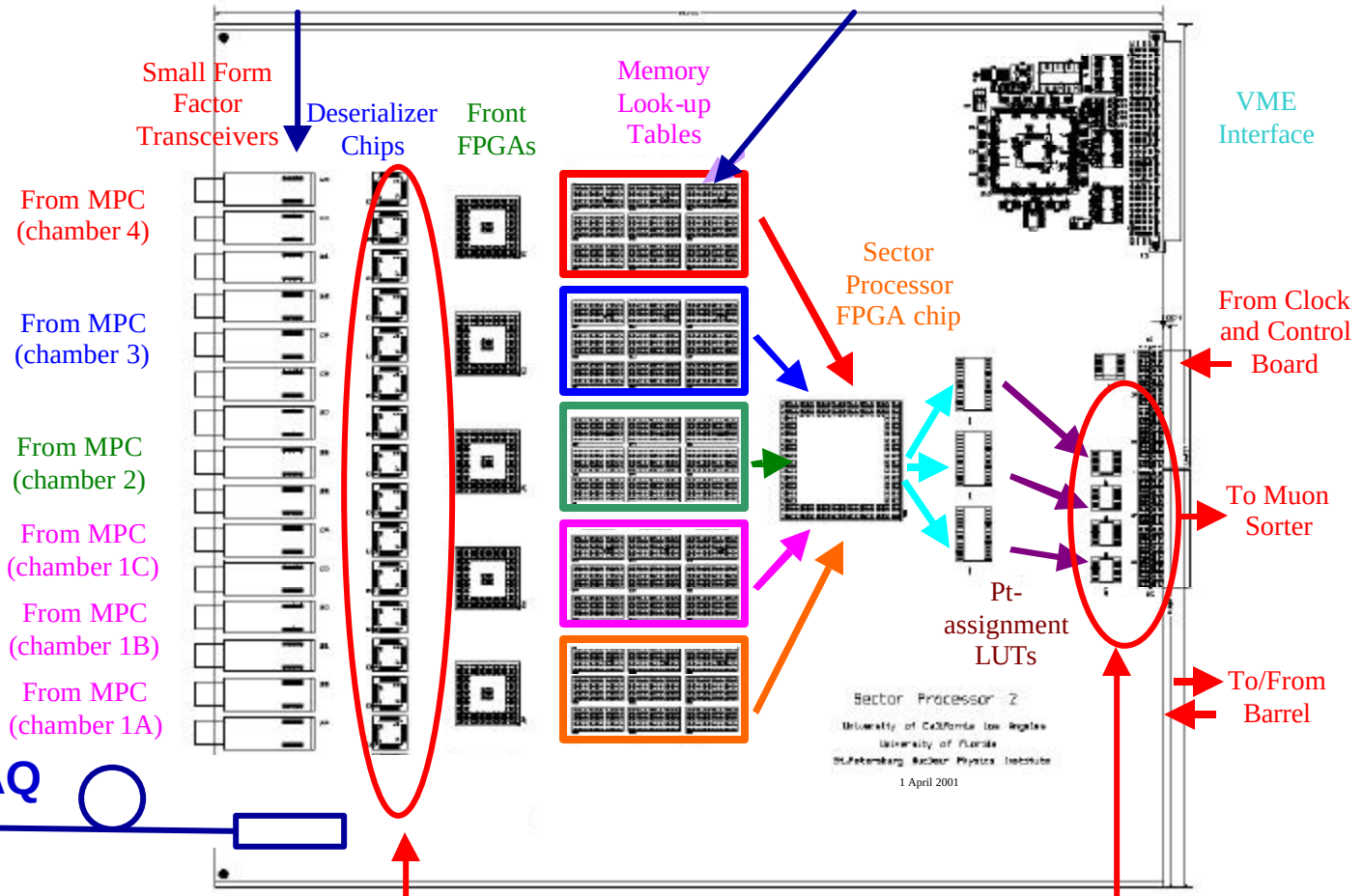

- **Total latency: ~ 20Bx (from input of SR/SP card to output of CCB/MS card)**
- **Power consumption: ~ 500W per crate**
- **15 optical connections per SR/SP card**
- **Custom backplane for SR/SPs < > CCB/MS connection**

# Merged SR/SP

**15 trigger links, 1 DAQ**

**51 or 27 SRAM**

**From trigger primitives**




**To CSC DAQ**

**Input: 528 bits/sector/b.x.**

**Output: 60 bits/sector/b.x.**

# Bi-Directional Optical Links

**Since we have both transmitters and receivers in the optical connection, this allows the option to send data as well as receive**

- ➔ **Makes testing much easier (1 board sends data to other)**

# SR/SP Inputs

## ➔ Muon Port Cards deliver 15 track stubs each BX via optical

Sent on first frame

| Signal | Bits / stub | Bits / 3 stubs (1 MPC) | Bits / 15 stubs (ME1–ME4) | Description |
|---|---|---|---|---|
| ½ Strip * | 8 | 24 | 120 | ½ strip label |
| CLCT pattern * | 4 | 12 | 75 | Pattern number without 4/6, 5/6, 6/6 |
| L/R bend * | 1 | 3 | 15 | Sign bit for pattern |
| Quality * | 3 | 9 | 45 | Computed by TMB |
| Wire group | 7 | 21 | 105 | Wire group label |
| Accelerator m | 1 | 3 | 15 | Straight wire pattern |
| CSC i.d. | 4 | 12 | 60 | Chamber label in subsector |
| BXN | 2 | 6 | 30 | 2 LSB of BXN |
| Valid pattern | 1 | 3 | 15 | Must be set for above to apply |
| Spare | 1 | 3 | 15 | |
| Total: | 32 | 96 | 480 | (240 bits at 80 MHz) |

Reduced from 5

Added

## ➔DT Track-Finder delivers 2 track stubs each BX via LVDS

| Signal | Bits / stub | Bits / 2 stubs (MB1: 60°) | Description |
|---|---|---|---|
| f | 12 | 24 | Azimuth coordinate |
| $f_b$ | 5 | 10 | ϕ bend angle |
| Quality | 3 | 6 | Computed by TMB |
| BXN | 2 | 4 | 2 LSB of BXN |
| Synch/Calib | 1 | 2 | DT Special Mode |
| Muon Flag | 1 | 2 | 2nd muon of previous BX |
| Total: | 24 | 48 | |

# SR/SP Outputs

➔ **6 track stubs are delivered to DT Track-Finder each BX via LVDS (can we multiplex at 80 MHz to save connector space?)**

| Signal | Bits / stub | Bits / 2 stubs (ME1: 20°) | Bits / 6 stubs (ME1: 60°) | Bits / 6 stubs @ 80 MHz | Description |
|---|---|---|---|---|---|
| f | 12 | 24 | 72 | 36 | Azimuth coordinate |
| h | 1 | 2 | 6 | 3 | DT/CSC region flag |
| **Quality** | 3 | 6 | 18 | 9 | Computed by TMB |
| **BXN** | – | 2 | 6 | 3 | 2 LSB of BXN |
| | 16 | 34 | **102** | **51** | **Total** |

➔ **3 muons per SP are delivered to Muon Sorter via GTLP backplane**

| Signal | Bits / m | Bits / 3 m (1 SP) | Bits / 36 m (12 SP) | Description |
|---|---|---|---|---|
| f | 5 | 15 | 180 | Azimuth coordinate |
| h | 5 | 15 | 180 | Pseudorapidity |
| **Rank *** | 7 | 21 | 252 | 5 bits $p_T$ + 2 bits quality |
| **Sign *** | 1 | 3 | 36 | |
| **BXN *** | – | 2 | 24 | 2 LSB of BXN |
| **Error *** | – | 1 | 12 | |
| **Spare *** | 1 | 3 | 12 | |
| **Total:** | 19 | 60 | **720** | **(360 bits at 80 MHz)** |

**Sent on first frame**

**Added, quality?**

# SR/SP Internal Dataflow

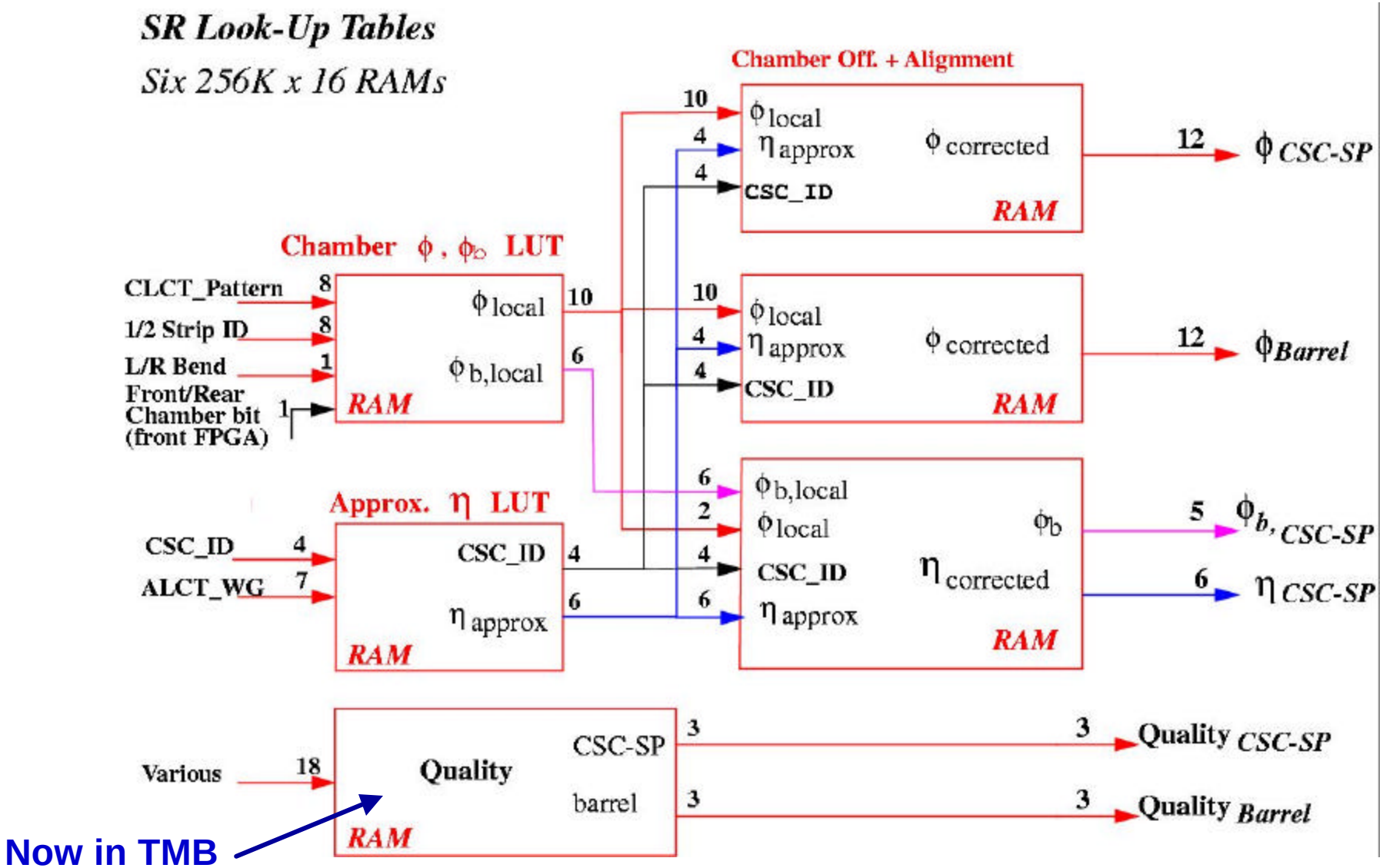
➔ **Data delivered from SR to SP**

| Signal | Bits / stub | Bits / 6 stubs (ME1) | Bits / 15 stubs (ME1–ME4) | Description |
|---|---|---|---|---|
| f | 12 | 72 | 180 | Azimuth coordinate |
| $f_b$ | 5 | 30 | 75 | $\phi$ bend angle |
| h | 6 | 36 | 90 | Pseudorapidity |
| **Accelerator** m | 1 | 6 | 15 | $\eta$ bend angle |
| **Front/Rear *** | 1 | 6 | 6 | ME1 chamber stagger |
| **CSC ghost *** | – | 4 | 4 | 2 stubs in same ME1 CSC |
| **Quality** | 3 | 18 | 45 | Computed by TMB |
| **Total:** | 28 | 172 | **415** | (sent at 80 MHz) |

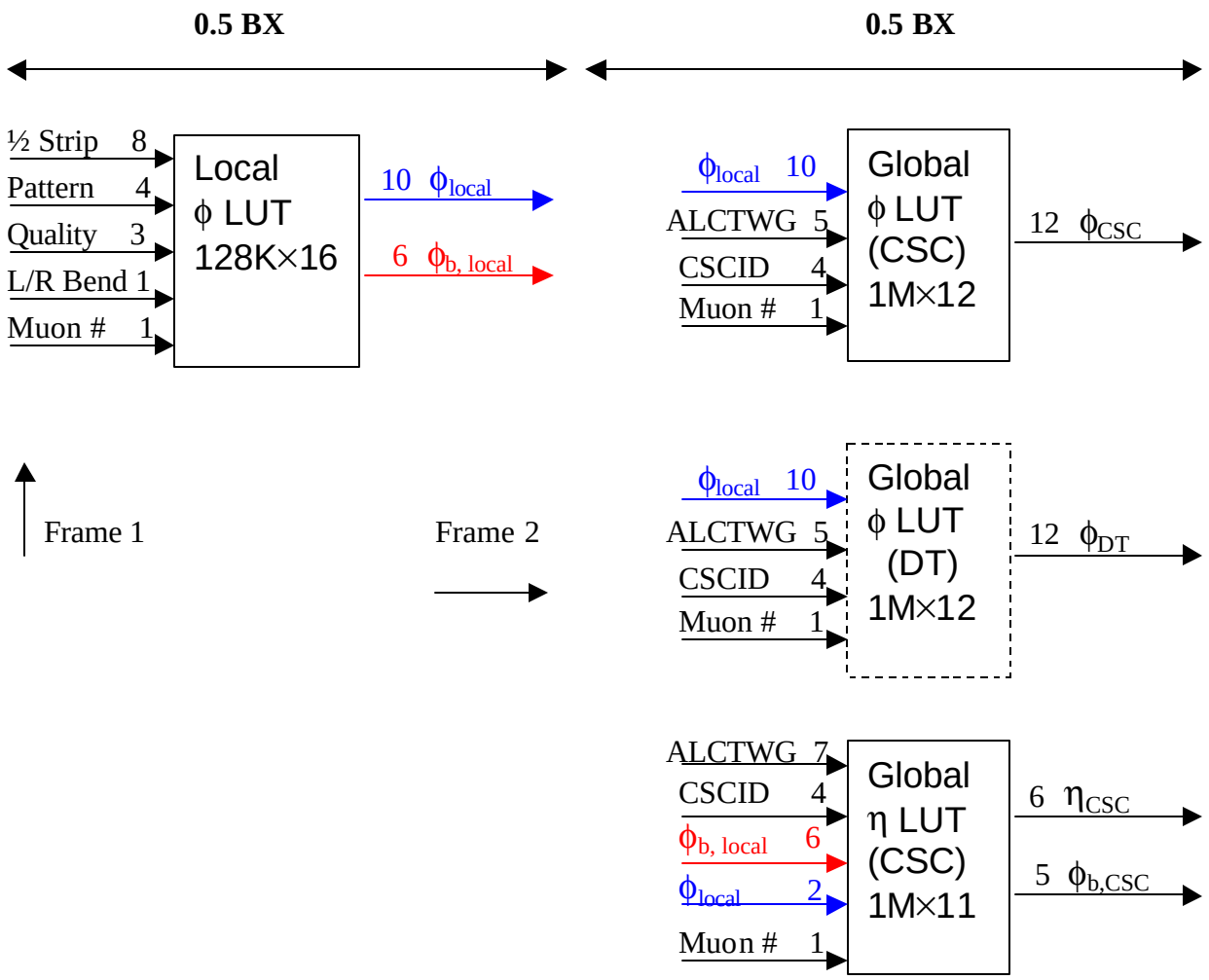
**ME1 only**

**226 if stubs multiplexed**

# Old SR Memory Scheme



# New SR Memory Scheme



# Discussion of SR Memory (1)

## Data Frames:

- Data arrives off links @ 80 MHz
- The proposed framing scheme implies no latency loss
  - First LUT operates on first frame only (but must reduce CLCT pattern label by 1 bit)
  - Can send 2 muons through one memory set with only 0.5 BX latency penalty to reduce chip count
- This frame definition must be applied in the TMB where the data is generated and first serialized (i.e. before MPC) to avoid latency penalty

## Memories:

- LUT for DT only applies to ME1
- Chip count is 4 or 3 per stub, down from 6 originally
- Increased memory size to 1M (okay for synch. SRAM)
- "Muon #" only applies if more than one stub in a BX is sent through same memory

# Discussion of SR Memory (2)

**One memory set per stub:**

- ➔ 6´4 + 9´3 = 51 chips
- ➔ 1 BX latency
- ➔ 415 signals to SP

**Multiplex stubs at 80 MHz:**

- ➔ 3´4 + 5´3 = 27 chips
- ➔ 1.5 BX latency
- ➔ 226 signals to SP

**First SR had 36 chips and 1 BX latency**

**Memory choices:**

- ➔ Current synch SRAM clocked at 160 MHz (tested) ⟶
- ➔ next generation synch SRAM clocked at 80 MHz
- ➔ asynch SRAM (but must remove 2 bits in final LUTs)

# Pipelined Memory Tests

**Developed small evaluation board to test two pipelined memories in series**

- ➔ **Samsung 1M x 18 synch. SRAM (K7A161800M)**
- ➔ **Include scheme to multiplex two muon stubs through same memory set @ 80 MHz**

**Tested chips up to 150 MHz and encountered no errors with random number inputs**

- ➔ **Specified maximum frequency is 180 MHz**

**Low power**

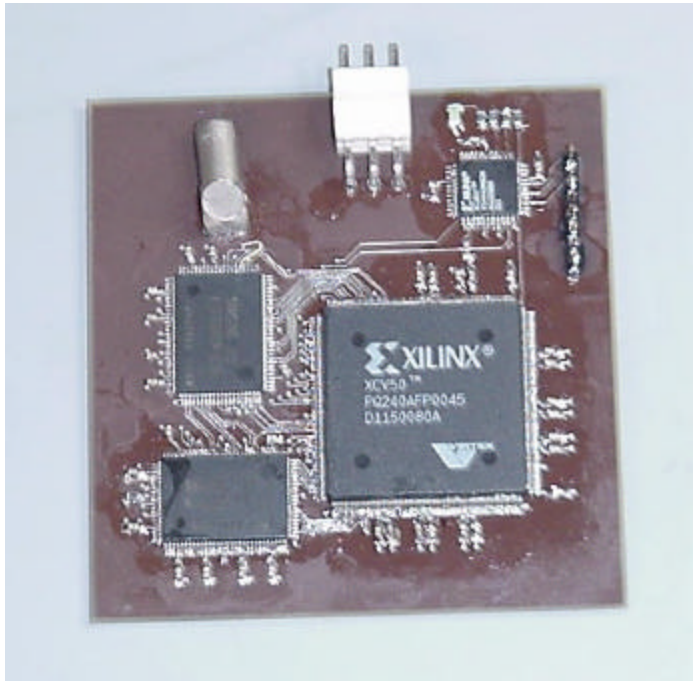
- ➔ **~1W per memory at 150 MHz**

**Latency determination**

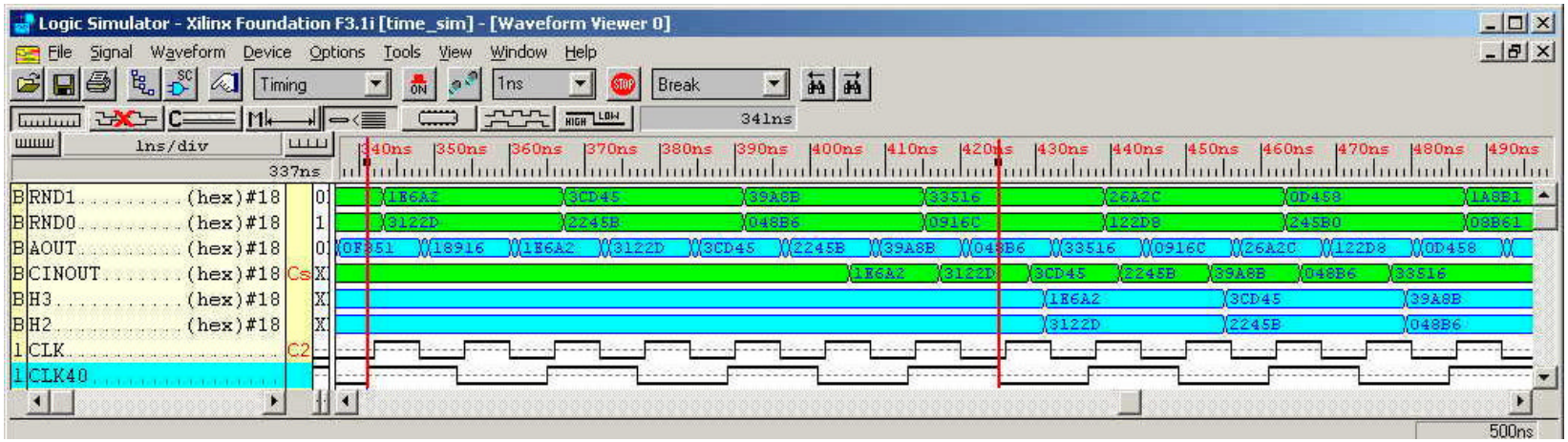
- ➔ **2 clocks per memory (4 clocks for two in series)**
- ➔ **Next generation will require just one clock**

# SR Memory Prototype

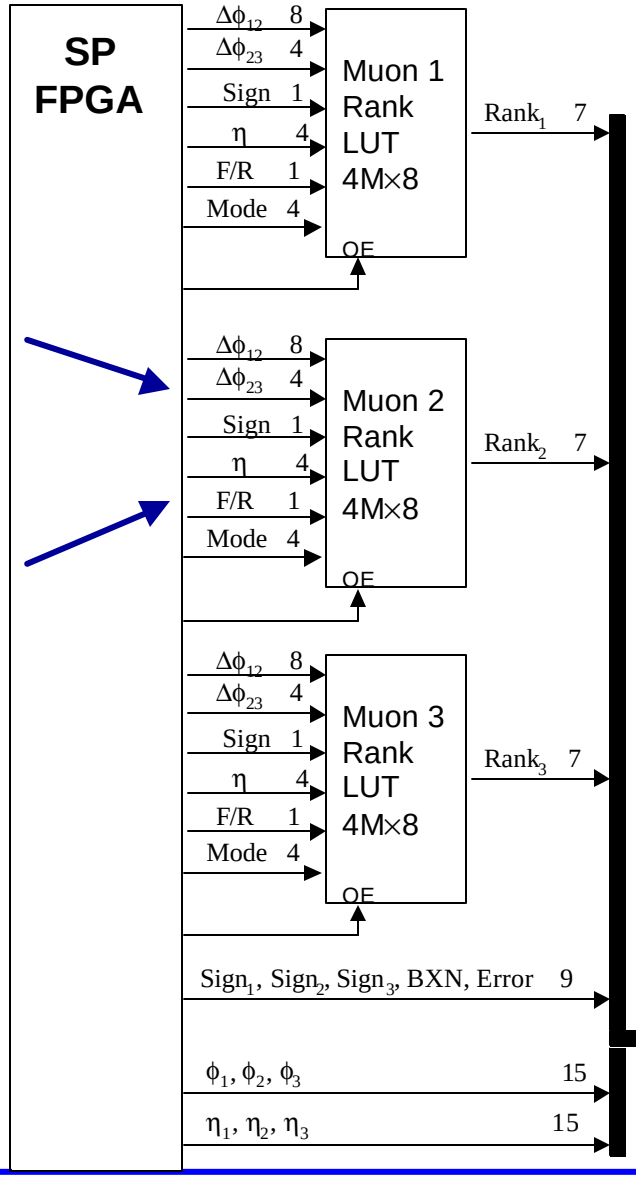
**Tested hardware →**




**Simulation illustrating clocking of board**



# SP Memory Scheme




$Df_{23}$ could be replaced by $f_b$

Added F/R bit to improve $P_T$ resolution

- Must serialize to fit data on backplane
- No latency penalty for serialization if Rank sent first to Muon Sorter
- SP FPGA contains tri-state buffers and generates enable for memories

# SP in a Chip Study

**Feasibility study was performed to fit all Sector Processor logic into one FPGA**

- Merged all separate schematics from current SP prototype into one project (17 FPGAs)
- Transformed large Track Assembler LUTs into a Verilog algorithm for FPGA
- Utilized 63% of the resources of a Xilinx Virtex-E (XCV1600EFG680-8)
  - Must understand how much $f_b$ logic adds
- Simulation shows that the latency of the SP logic is 11 BX at a maximum frequency of 41 MHz
  - Add 1 BX for final $P_T$ Assignment LUT
  - Compare to 15 BX of current SP prototype Þ save 3 BX
- ChannelLink between SR and SP removed (save 4 BX more)
- SP Chip I/O:
  - 415 (or 226) CSC + 48 DT input bits
  - ~135 output bits + control signals

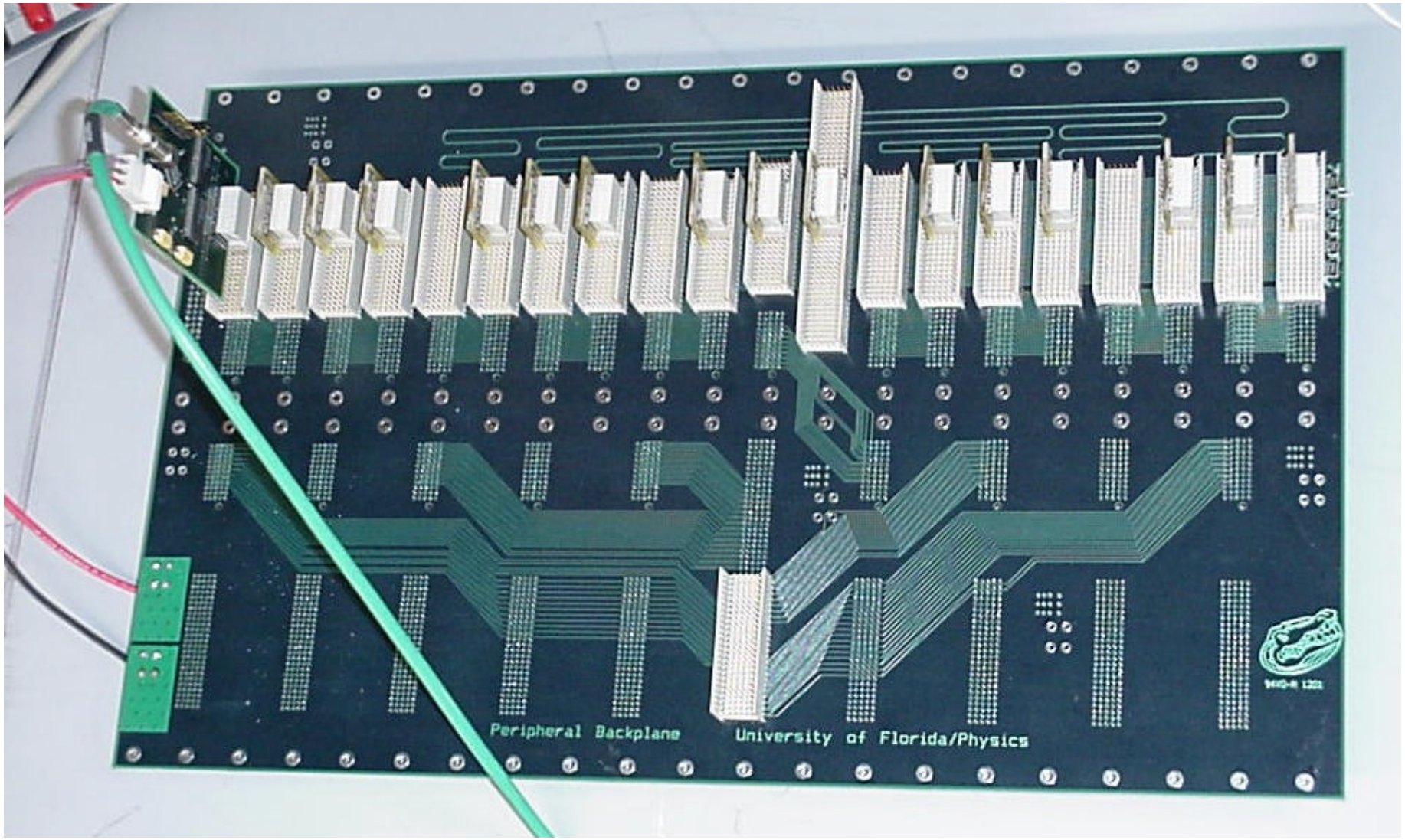
$\Rightarrow$ ~600 max I/O

# Backplane Development

## Next generation backplane technology will be GTLP

- No differential signals (fewer traces)
- We first tested a small prototype backplane with GTLP signals
  - It works: tested drivers from Fairchild, and Xilinx Virtex I/O
- We have now tested a full 21 slot custom VME backplane for use in the CSC front-end peripheral crate
  - Includes 40 MHz bussed signals and 80 MHz point-to-point
  - Highest density is ~660 signals into Muon Port Card (vs. ~720 signals into CSC Muon Sorter in CSC TF crate) multiplexed at 80 MHz
  - Have tested bussed signals with backplane fully loaded Þ

# Prototype Peripheral Crate Backplane



# CSC TF DAQ Bandwidth

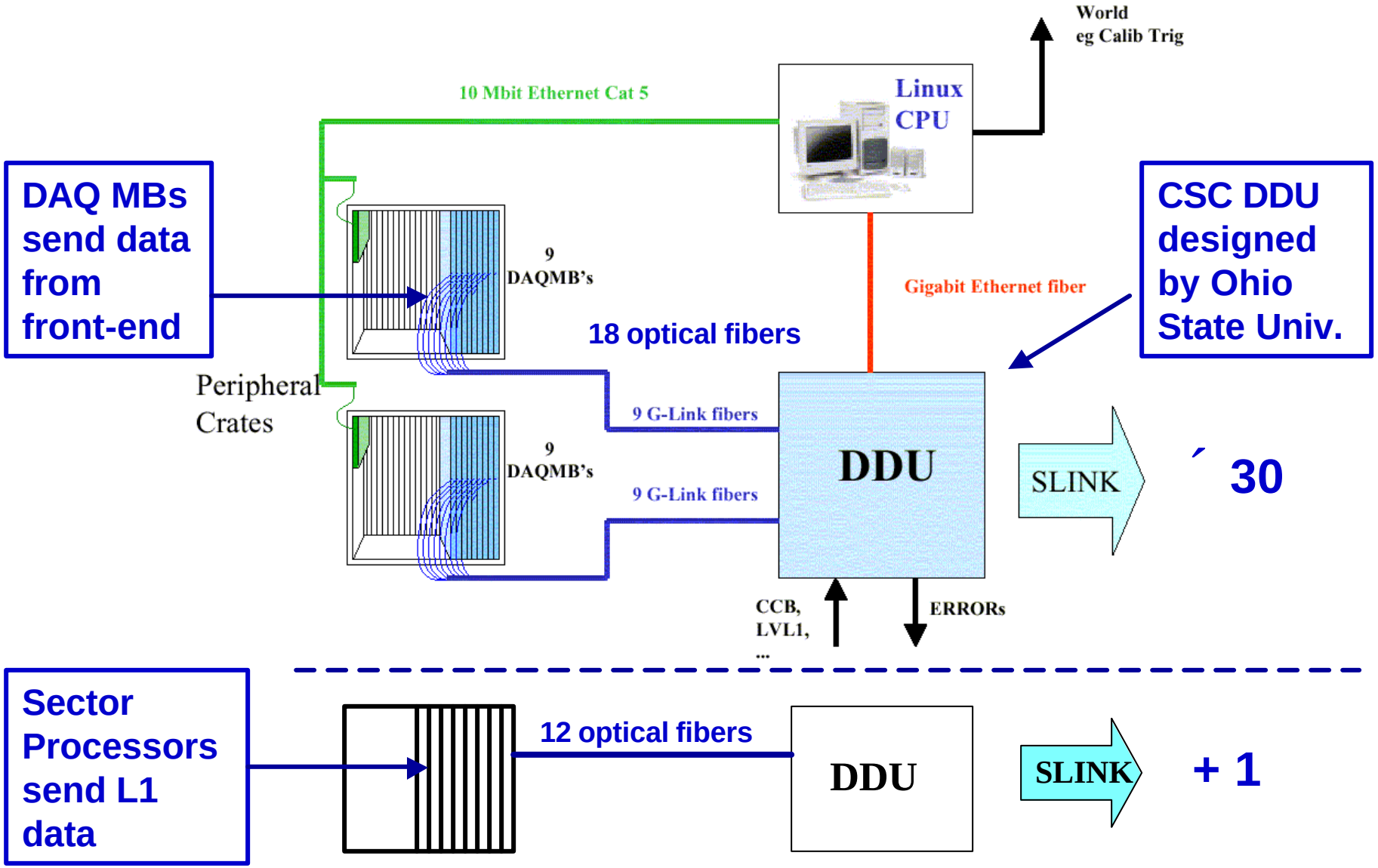
## Send input of SR and output of SP to DAQ stream for diagnostics

- Send ~600 bits (80B) per L1A per SR/SP
- 12 SR/SP send 1kB per L1A
- 100 kHz L1A rate Þ 100 MB/s
- One S-LINK64 handles 200 MB/s

- Note that trigger data is expected to be sparse, so this bandwidth is an upper limit and should be compressed

- CSC Track-Finder DAQ acts as additional DDU for CSC system (plan to use existing DDU design by OSU)
  - OSU may use new HP serializer in place of TI for compatibility with Gbit ethernet
  - They should have results from an evaluation board within a month

# Mirror CSC DAQ Path



# Manpower

## University of Florida

- D.A. – PI
- Alex Madorsky – lead engineer
- Bobby Scurlock – graduate student
  - Trigger simulations
  - SP firmware/software tuning, crate tests

## PNPI

- Victor Golovtsov – PI
- Lev Uvarov – design engineer
  - Replaces Boris
  - Extensive experience on D0 (muon readout), E781, E761

## UCLA

- R.C. – PI
- Jason Mumford – graduate student
- Slava – postdoc
  - Both maintain trigger primitive and SR software

# Software Limitations

## CLCT patterns and pattern number

- No $f_b$ from SR
- $f_b$ not used for extrapolation in SP
  - Might reduce backgrounds
  - Logic size not counted in SP chip study
- $f_b$ could improve $P_T$ assignment
- Improved $f$ precision results from using 6 layers vs. 1
  - Could improve $P_T$ resolution

## Track-Finder algorithms

- Bunch Crossing Analyzer not implemented or tested
- New Verilog Track Assembler needs simulation
- Miscellaneous cuts need tuning: $h$, quality,…
  - Should improve low $P_T$ rejection

## Validation against current HW designs

- Need closer link to hardware LUTs and algorithms
- Improve maintenance of design to shorten debug time for next prototypes

# Design Maintenance

**Will overhaul some of the SP software/firmware to facilitate changes to both**

- ➔ **Have SW algorithms match Verilog better**
- ➔ **Have SW read same HW LUTs (it already generates them)**

**Plan to test next SP design even before construction!**

- ➔ **Add utilities to write ORCA data into Xilinx simulator format and to compare simulator output to ORCA**
- ➔ **Gives us a head start on validating logic design**
- ➔ **Will allow us to focus on HW debugging rather than SW debugging when testing the next prototype**