CSC Beam Test, Take 2

SP / TMB comparisons and DT / CSC integration tests

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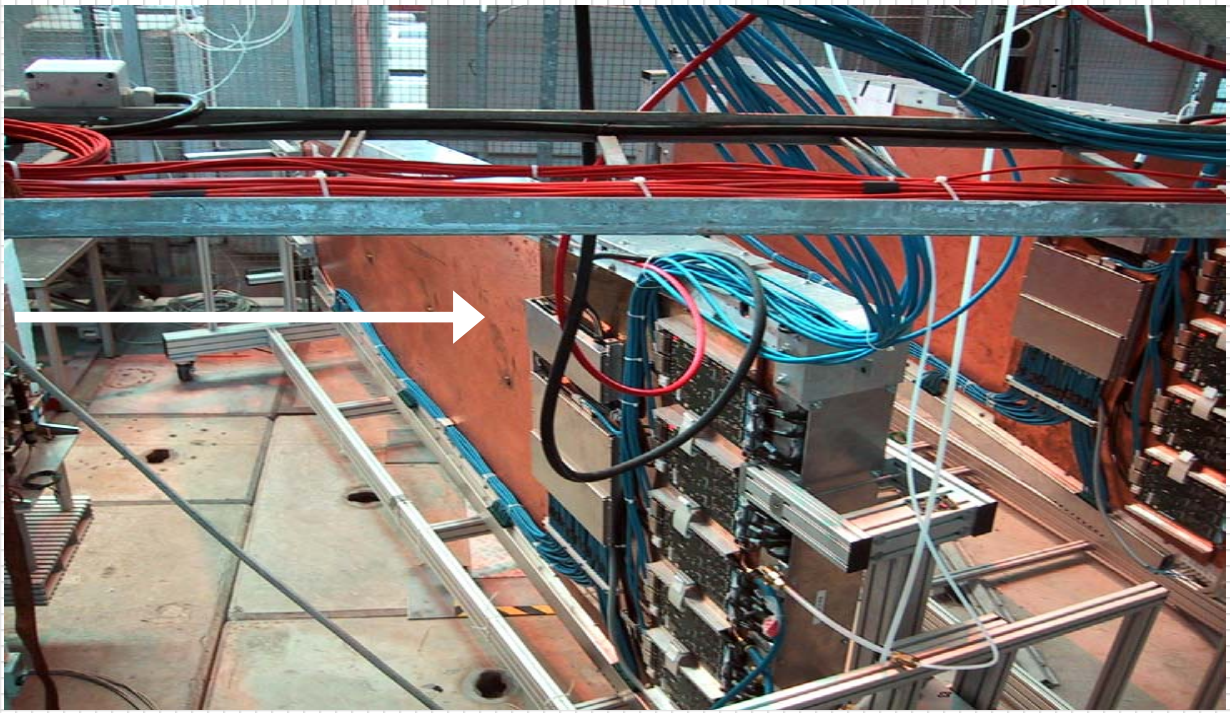
Where to find information

- Documentation:
  - http://www.phys.ufl.edu/~acosta/cms/trigger.html
  - Includes scanned pages from log books and links to online log and other web sites

- Data:
  - /castor/cern.ch/user/t/tbx5ccdr/
  - “rfdir” for listing
    “rfcp” for copying
    (may need to wait a long time as data is staged from tape)
  - Runs 5018 – 5164
  - Correlated SP data starts with run 5108

Beam Test of 2 CSC's at X5a

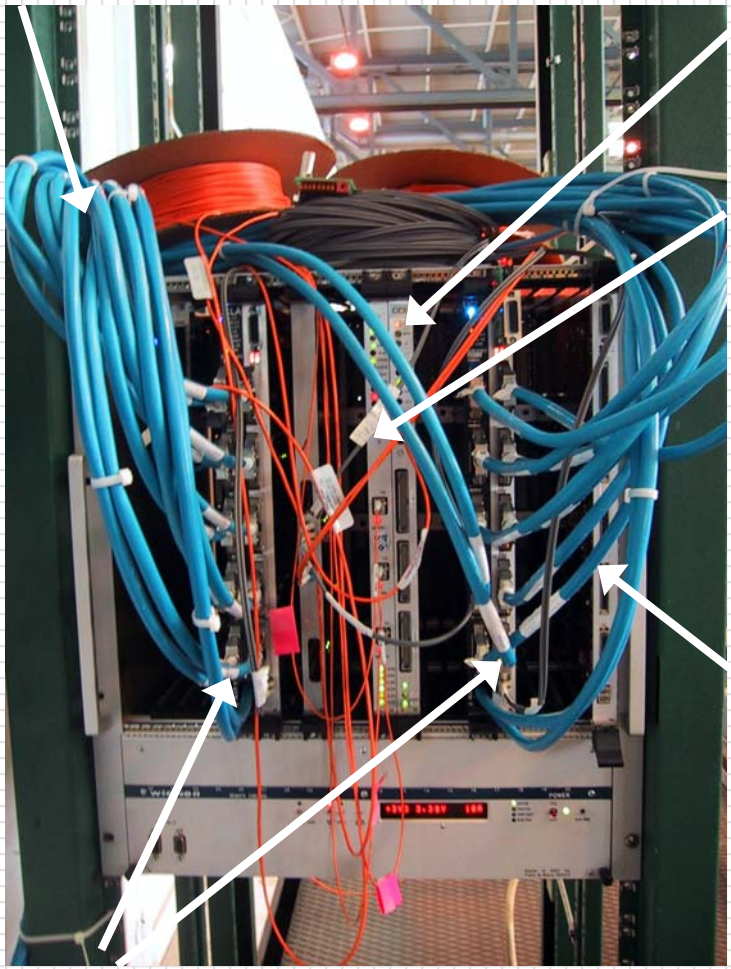


Goal: complete electronic chain test of data transmission from CSC front-end electronics to the Track-Finder trigger, all operating synchronously with the 40 MHz structured beam

MPC and SP included in tests, various clocking solutions tried

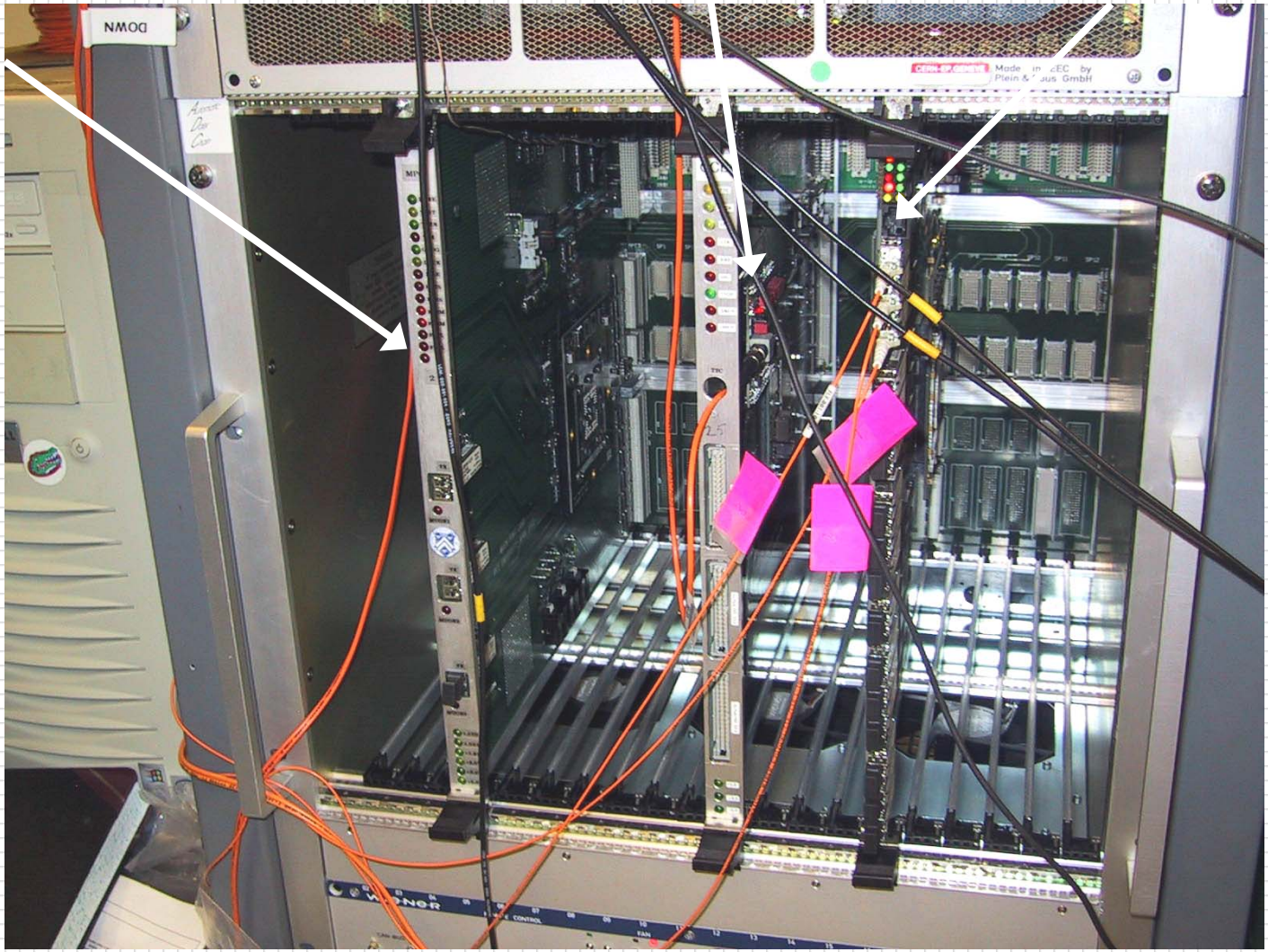
CSC Peripheral Crate

From front-end cards



2 TMBs and DMBs (CSC id's 3 and 8)

CSC Track-Finder Crate



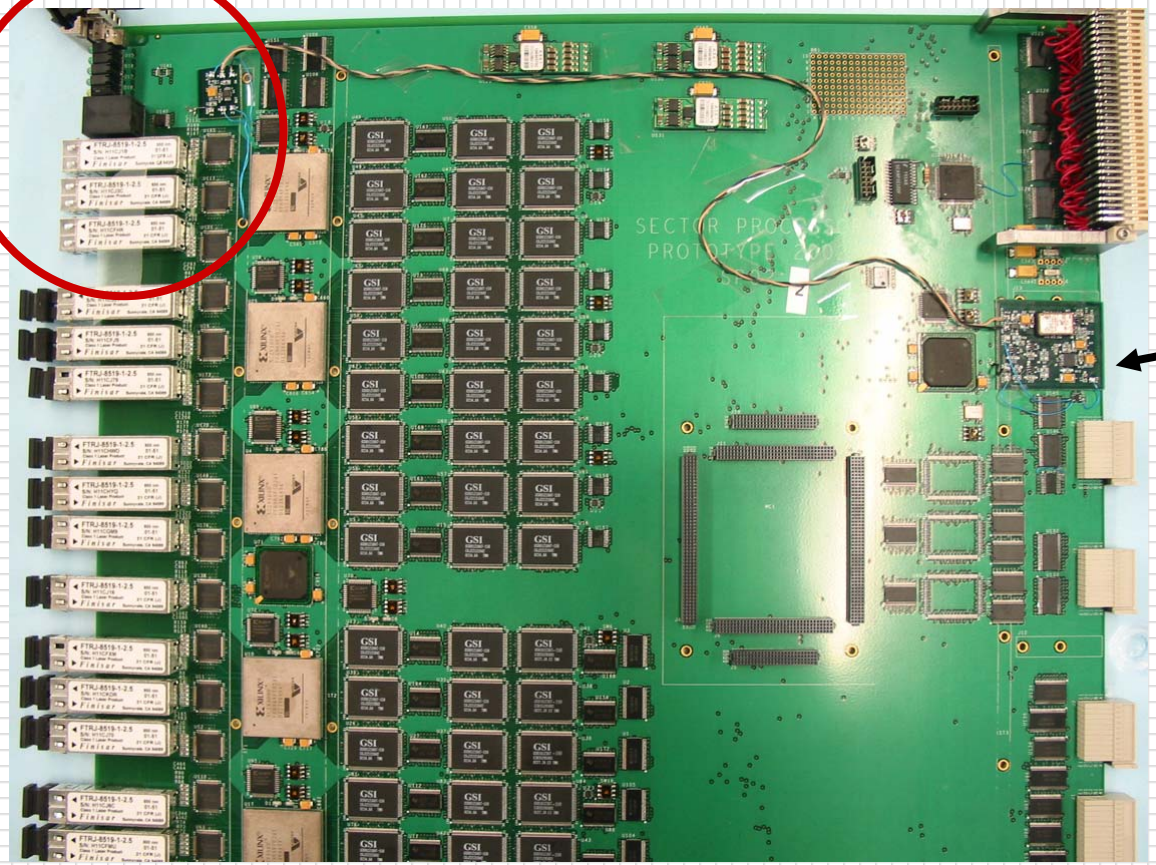
CSC Track-Finder Trigger

Test 3 × 1.6 Gb/s optical link connections from CSC electronics

Uses TLK2501 chipset

Requires very stable reference clock for error-free operation

Home-built VCXO & PLL clock patch added to clean incoming TTC clock for links, but TTC QPLL also tested



Test Results

- Using home-built VCXO+PLL solution (or QPLL) for 80 MHz reference clock to TLK2501 receivers:
  - PLL locks to incoming machine clock
    (Once Bruce Taylor helped us set up the TTCmi crate correctly)
    - Measured frequency: 40.078893(1) MHz
  - No errors on optical links reported over many hours of PRBS and data tests
    - Continuous data transmission or framed mode (idle frames sent)
- Data successfully logged by both CSC DAQ and CSC Track-Finder readout
  - SP data FIFO synchronized to L1A

TTC QPLL Mezzanine card (TTCRq)

- Three made available to CSC group for testing during Sept.03 structured beam test
- Provides stable clock signals at 40, 80, and 160 MHz at correct LHC frequency
- Installed on CCB with 40 MHz clean clock sent to backplane, 80 MHz clock sent by twisted pair to SP or MPC
  - Noticed that CCB commands have 1 BX extra latency with TTCRq

TTCRq (QPLL) Test Results

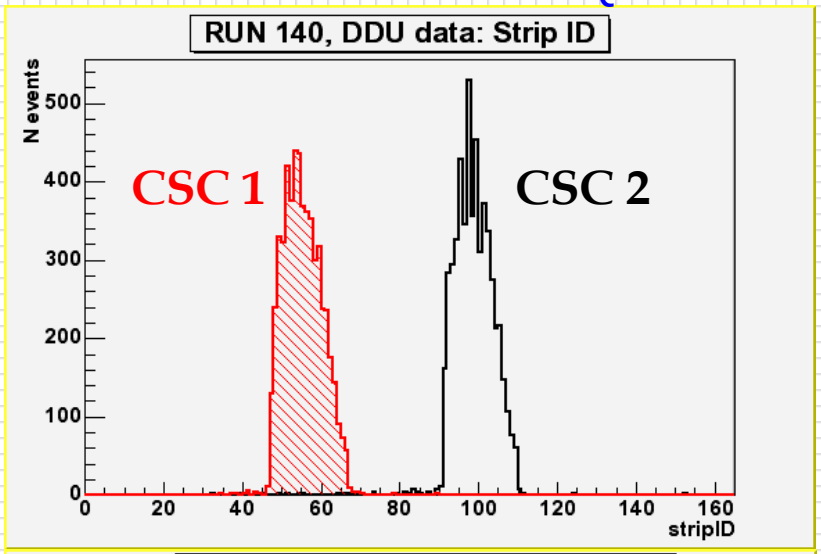
1. QPLL 80 MHz clock directly to MPC transmitters
   Lev's VCXO+PLL for SP receivers
   - No link errors for 20 minute PRBS test
2. QPLL 80 MHz clock directly to SP receivers
   MPC uses default clock multiplier
   - No link errors for 15 minute PRBS test
   - Successfully logged data for 10K events (run 5151)
3. QPLL 40 MHz clock on TF crate backplane
   SP uses DLL in FPGA for clock multiplier
   - Link errors observed in PRBS test
4. TTCRq on CCB in peripheral crate
   TTCRm on CCB in TF crate
   - Able to take data with same trigger efficiency
     (i.e. TTCRq works for peripheral crate as well)

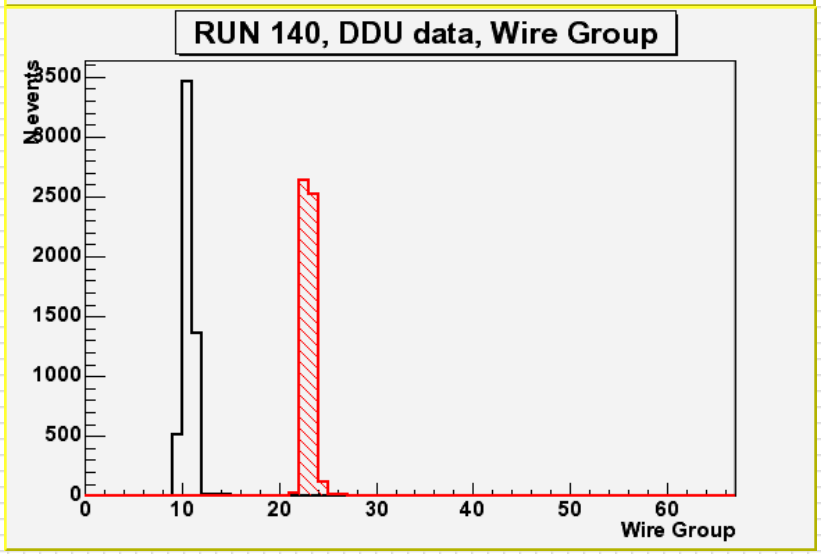
Data-taking Mode

- Most data logged using two independent DAQ systems:
  - CFEB Control for DDU data $\Rightarrow$ run00nnnn.dat
  - SP DAQ for Track-Finder data $\Rightarrow$ SPDAQ*.dat
- Maximum data rate limited to ~400 L1A/spill
- SP records 5 BX of input data for each L1A, with most trigger data arriving on central BX
- XDAQ version by Wilkinson, Tumanov, et al. also logs data correctly
  - Underlying SP code the same as for standalone DAQ since it was written using XDAQ
  - All analysis of SP and DDU data done using the "DataFormat" packages

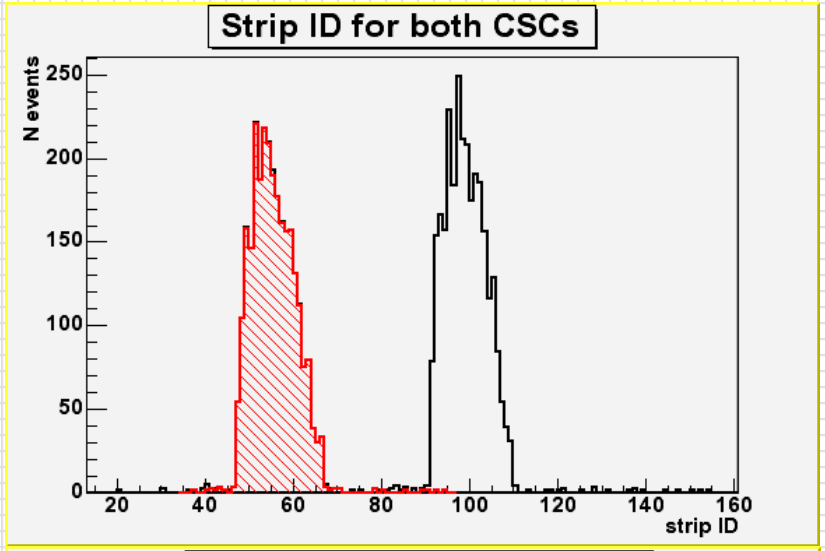
Comparison of TF Data with DAQ

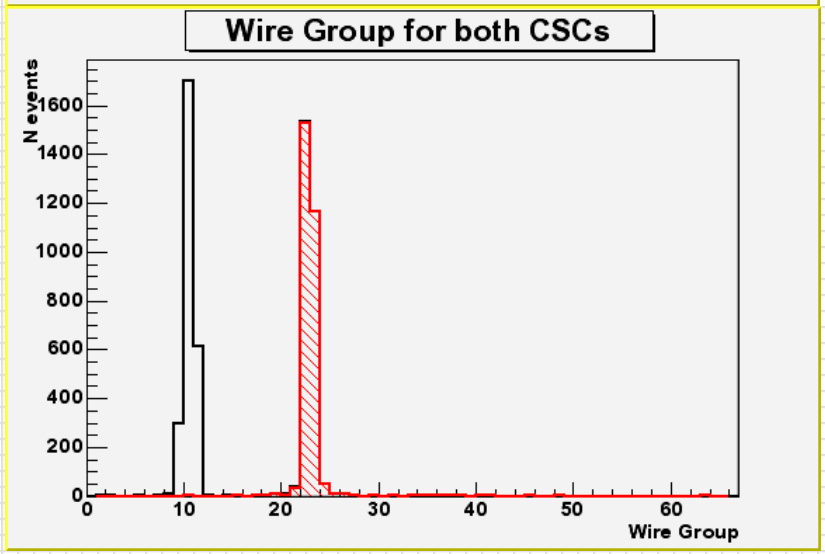
CSC Data from DAQ





CSC Track-Finder Data





Detailed TMB–SP Data Comparison

- Use TMB BXN @ Pre-trigger, and LCT BX offsets, to assign BXN to LCT's
  - SP BXN – LCT BXN = 44 typically
    (may be affected by CCB command delays)
  - Empirically find:
    - If LCT BX Difference = 0x1 ⇒ Add +1 to TMB BXN
    - If LCT BX Difference = 0x2 ⇒ Add +2 to TMB BXN
    - If LCT BX Difference = 0x3 ⇒ Add -1 to TMB BXN
- Run TMB data through MPC simulation to compare with SP
- Comparison between SP and TMB for all 5 BX read out by SP for every L1A match:
  - 98% agreement for ~70K events
- Mismatches between TMB and SP data are in BX assignment only, *not* in LCT frames

SP – TMB Mismatches

- Nearly all of the mismatches involve differing BX assignment for LCTs from the TMB for csc#8
  - Data frames are in agreement, however
- Excluding csc#8 in these cases and comparing TMB and SP for csc#3 $\Rightarrow$ near perfect agreement
  - Just 32 discrepancies from an analysis of 60K events, where BX assignment of TMB for csc#3 differs
- For these mismatches, the SP usually has the LCTs on the central BX in the SP read-out
  - So trigger data appears to be good!
- Conclusion for DAQ readout of TMB data:
  - TMB #8 has BX error 2% of time
  - TMB #3 has BX error 5×10^{-4} of time

  } **Can be 2 or more BX off from SP**

    - This increased to 5×10^{-3} for runs with TTCRq in Peripheral crate (which changed the timing)

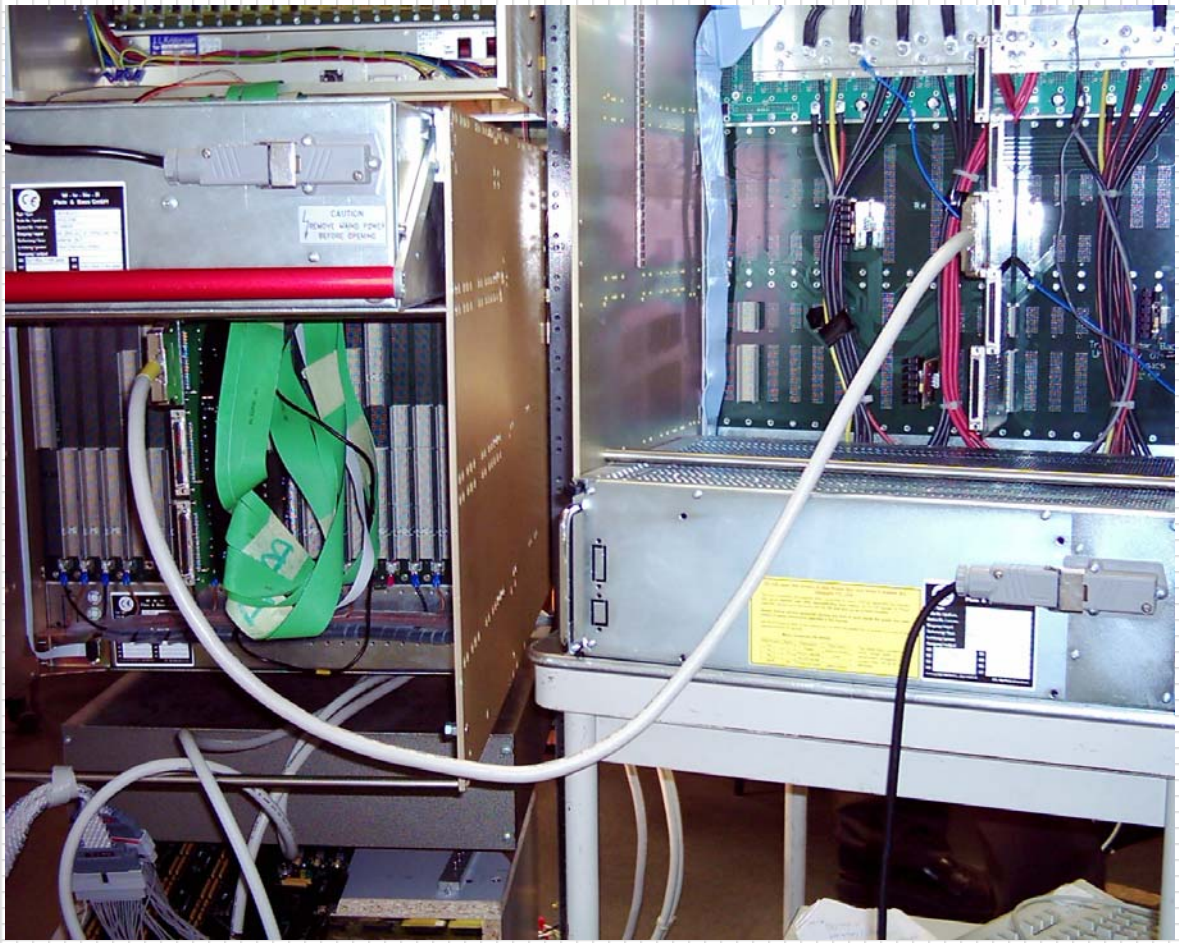
Other effects

- TMB/SP mismatch rate seems independent of ALCT delay setting (timing scan runs)
- When DDU errors occur in DAQ, lots of TMB/SP mismatches result
- SP DAQ FIFO sometimes fills up if L1A rate is too high
  - Affected pion runs mostly
  - BX counter still increments, but data is frozen at last event
  - Need to add FULL flag to event header

First DT/CSC Integration Tests

(The fun continues the week after the beam test…)

DT TF transition card ↔ CSC TF transition card



DT/CSC interface

- Reminder: data is exchanged between the two systems for efficient coverage of the region $0.9 < |\eta| < 1.2$
  - CSC sends 3 LCT's/BX (52 bits) from ME1 to two 30° DT sectors
  - DT sends 1 segment/BX (26 bits) from each 30° sector
  - Signaling standard is LVDS at 40 MHz through SCSI cables and connectors
- Layout problem on CSC transition card meant connectors had to be attached on opposite side of board
  - Cable connector had to be flipped 180° at one end so that signals are received on correct pins
    - Only had time to make & test custom 1m cables
  - Signals inverted in firmware to handle polarity change

DT → CSC transmission test

- DT Data Source Card → DT TF → DT transition card → CSC transition card → CSC TF
  - Data was received in a FIFO in the main FPGA of the SP mezzanine card
  - BC0 marker sent on first data word
  - Tested walking 1's, walking 0's, & simulated muon data
- All bits and clock were received, but some bits were swapped at DT output before being sent to CSC

CSC → DT transmission test

- CSC TF → CSC transition card → DT transition card → DT TF
  - Data is sent from Front FPGAs, bypassing LUTs, and delivered to CSC transition card
  - Tested walking 1's and walking 0's
    - DT TF has no FIFO to store received data
- Two dead TTL→LVDS buffer chips on CSC transition card leads to 7 missing signals
  - But signals are OK and in correct order on SP backplane connector
  - Remaining signals are seen by DT TF, albeit with limited storage capability

Cosmic Test Stand at UF

- Testbeam setup being reassembled at UF for future Track-Finder integration tests, slice-test code devlopment, etc.

Conclusions

- CSC beam test with Track-Finder was a success!
  - Complete electronic chain test of data transmission from CSC front-end electronics to the Track-Finder trigger, all operating synchronously with the 40 MHz structured beam
  - Latest QPLL design from CERN tested and works
  - “Slicetest” control and event-building software tested
- Initial tests show that DT and CSC Track-Finders can exchange data
  - First integration test between UF and Vienna (good check on documentation!)
  - A few minor problems on both ends with swapped bits, connectors, and dead chips
  - More sophisticated Track-Finding tests with longer cables in future

Thanks!

- Thanks to everyone who helped make the second beam test a success