

Development and Test of a Prototype Regional Track-Finder for the Level-1 Trigger of the Cathode Strip Chamber Muon System of CMS

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Abstract

We report on the development and test of a fast 3-D Track-Finder for the Level-1 trigger of the CMS endcap muon system. System tests included four types of custom circuit boards clocked at 40 MHz, optical links, and a high-speed custom auxiliary backplane in a VME crate. The hardware results, calculated using field-programmable gate arrays, programmable logic devices, and memory lookup tables,

agreed bit-for-bit with software simulations for both random patterns and realistic tracks.

Key words: First-level muon trigger, Fast track finder

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1 Introduction

The Large Hadron Collider (LHC) will offer a new window on electroweak symmetry breaking when it provides proton-proton collisions at a center-of-mass energy of 14 TeV later this decade. At the full design luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$, the beam crossings occurring at 40 MHz are each expected to contain approximately 20 minimum-bias collisions. The role of the Level-1 trigger of the Compact Muon Solenoid (CMS) Experiment is to filter the data rate from 40 MHz to 100 kHz using custom electronic processors, before initiation of the full detector digitization and subsequent analysis by the online computer farm for the Level-2 and Level-3 filters. The latency allocated for this first level of filtering (including cable delays) is $3.2 \mu\text{s}$ from bunch crossing to the trigger decision and return of the Level 1 accept signal to the front-end electronics boards. The processing must be pipelined so that the trigger operates deadtime free.

The Level-1 trigger electronics of the CMS muon system must identify the number of distinct penetrating particles, and measure the momentum of each, in order to reduce the several megahertz rate of low-momentum muons produced at full LHC luminosity. With a safety factor of 3, and with equal sharing

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of bandwidth between muon, electron/photon, and jet triggers, the Level-1 muon triggers are limited to no more than about 12 kHz rate. This requires a momentum resolution no worse than about 25% in order to sufficiently reduce the rate of low momentum muons.

There are three largely independent systems to perform this task [1,2]: a barrel muon system composed of drift tubes (DT) in the central region, resistive plate chambers (RPC) throughout, and the endcap muon system composed of cathode strip chambers (CSC). The Track-Finder associated with the latter system is the subject of this paper. A separate 2-D Track-Finder associated with the DT system is described in Refs. [2,3].

The design of the endcap muon system of CMS [1,4] contains four stations (ME1–ME4) of cathode strip chambers on each end of the experiment, covering the range in pseudorapidity (η) from 0.9 to 2.4 (see Fig. 1). (ME4 is not in the baseline design, but its eventual inclusion has been anticipated in the design of the trigger.) A single station is composed of six CSC layers, where a single layer has cathode strips aligned radially and anode wires aligned in the orthogonal direction. Each CSC is trapezoidal in shape with either a 10° or 20° angular extent in azimuth (ϕ). Iron disks between the muon stations serve as a return yoke for the central 4 T solenoid, and the muon momentum is measured from the track sagitta induced by the magnetic return field.

The task of the CSC Track-Finder is to reconstruct muon tracks in the CSC endcap muon system and to measure for each the following three quantities:

- p_T , the transverse momentum,
- ϕ , the azimuthal angle, and
- η , the pseudo-rapidity.

This objective is complicated by the non-axial magnetic field in the CMS endcap and by the expected high background rates at full LHC luminosity. Consequently, the design incorporates full 3-dimensional spatial information into the track-finding and measurement procedures.

We have developed and tested a prototype of the CSC Track-Finder, combining the following custom-built components:

- a high-speed auxiliary backplane for the VME crate that contains the prototype circuit boards;
- a Clock and Control Board (CCB) that receives and redistributes signals from the CMS experiment's Trigger Timing and Control system, which distributes the clock and other signals.
- two Muon Port Cards (MPC) that receive digital track information from the CSC front-end electronics, process and filter it, and send it over optical links to the control room;
- three Sector Receivers (SR) that receive the optical data, process it, and pass it over the custom backplane; and
- a Sector Processor (SP) that links together track segments to make tracks, and computes the track quantities.

Our online software, coupled to our offline simulation, allowed us to perform extensive tests which verified the integrity of all these components and their interaction with each other at the full design speed.

The next section gives an overview, and is followed by sections describing each of the above components. Section 8 describes the systems test combining the various components. We conclude in Sec. 9, which briefly describes improvements which will be incorporated in the production version of the Track-Finder

in order to improve the computation time (latency) and reduce cost.

2 Track-Finder Overview

A block diagram of the CSC Track-Finder architecture [2] is shown in Fig. 2. The portion described in this paper includes the custom backplane and CCB (not shown), and the MPC (labeled PC), SR, and SP circuit boards. Front-end electronics boards (either mounted directly on the CSC chambers or in nearby crates) use pattern-recognition firmware based on pattern templates to reconstruct track segments spanning the six layers within each CSC chamber [5]. These segments, called Local Charged Tracks (LCT), are found independently in both the anode (ALCT) and cathode (CLCT) views, and are combined in a Trigger Mother Board (TMB). Up to two combined anode/cathode LCTs are sent from 9 TMBs to Muon Port Cards which reduces the number of LCTs delivered from each CSC sector to a maximum of three. The Track-Finder (SR and SP) receives data from several MPCs, reformats the data into tracking variables, applies alignment corrections, reconstructs tracks across the four endcap disks, and computes the p_T , η , and ϕ . The processing in two of the boards (the MPC and the SP) includes sorting on quality indicators and elimination of low-quality track segments or tracks if necessary.

The CSC trigger system is logically partitioned into 12 azimuthal sectors (6 per endcap) for purposes of regional track-finding. Thus, 12 Sector Processors (SP) identify the three best muons (if present) in each 60° azimuthal sector. Each processor is a 9U VME card housed in a crate in the underground counting room of CMS. Each SP receives its data from three Sector Receiver (SR) cards also in the crate, which collect and reformat the track segment data delivered

over optical links from the CMS detector. The source of these signals are Muon Port Cards (MPC) that reside in separate crates of the periphery of the CMS endcaps and that collect track segments from up to nine CSCs.

A maximum of six track segments are delivered to a SP from the first muon station (ME1) of a sector. These track segments arrive from three MPCs, each delivering up to 2 track segments in a 20° subsector, as illustrated in Fig. 3. For the other muon stations (ME2–ME4), one MPC per station delivers 3 track segments. In addition, up to four track segments from the barrel drift-tube (DT) muon system are propagated to a transition board in the back of the crate and delivered to each SP as well.

The output of the Track-Finder consists of the four best identified muons and their kinematic and quality descriptions; these are sorted by a Muon Sorter and then transmitted to the Global Muon Trigger (GMT), which combines these CSC tracks with tracks from two other muon systems in CMS: the barrel muon drift-tube (DT) system at central rapidity, and the resistive-plate chamber (RPC) system throughout CMS [2]. The GMT in turn sends combined results of all three muon systems of CMS to the global Level-1 decision logic. In the region near $\eta = 1$, the CSC and DT systems overlap, and their respective Track-Finders exchange information to make composite tracks.

3 Crate, Backplane, and Computer Interface

The Muon Port Cards will reside in crates located on the periphery of the detector. The rest of the CSC Track-Finder will be contained in several 9U VME crates in an underground counting room separated from the high-radiation de-

tector hall by a concrete wall. In the present prototype design, it was foreseen that 2 Sector Processors, 6 Sector Receivers (3 per SP), and 1 Clock and Control Board would occupy one crate; thus 6 crates were foreseen for the entire CSC Track-Finder.

For the tests reported here, only the contents of half a crate were prototyped (1 SP, 3 SR, and 1 CCB), as shown in Fig. 4. Additionally, the two MPCs were placed in the same crate, although communication to the SR was through a 100 m optical fiber as will be the case when the MPCs are in the detector hall.

The crates are 9U×400 mm VME crates with the upper 3U part of a 21-slot VME64x backplane. A custom 6U point-to-point backplane is used to carry all track segment data from the Sector Receivers and DT Track-Finder to the Sector Processor. In order to reduce the backplane trace count by approximately a factor of 3, all data (except the clock) are serialized/deserialized using Channel Link LVDS drivers from National Semiconductor (models DS90CR285/286). This chipset is specified to work without errors at input frequencies up to 66 MHz (data transmitted at 462 MHz), for link lengths up to 10 m. In our design, the data are driven at 40 MHz (data transmitted at 280 MHz), and the link length does not exceed 30 cm. Care was taken in the layout to place the driver chips as close as possible to the backplane connector. The backplane line impedance was measured to be 130 ohms, and 4 layers were required for routing, including 2 ground planes. The connectors used are AMP Z-Pack 2 mm hard metric connectors, which are 5 rows wide. With all parameters well within specification, we had no problems with Channel Link communication.

This test crate was replicated at three institutions (UF, Rice, and UCLA),

so that individual boards could be debugged before being brought together. In each case a VME to PCI interface (Bit3 Model 917 or 918 from SBS Technology) was connected to a PC running a version (98, NT) of the Microsoft Windows operating system. Downloading of EEPROM and/or Field-Programmable Gate Array (FPGA) contents, Programmable Logic Device (PLD) contents, LUT contents, and test data was successfully performed in a variety of modes (single-word and block transfer, memory-mapped or not). Typically JTAG, the IEEE 1149.1 standard of the Joint Test Action Group (JTAG), was used internally and from front panel connectors during tests.

4 Clock and Control Board

A Clock and Control Board (CCB) is in each crate to receive timing information from the LHC accelerator Timing, Trigger, and Control (TTC) system [6] and distribute it to the other boards in the crate. Similar CCBs will be used in the crates in the detector hall containing MPCs and in the crates in the electronics room containing the Track-Finder. The backplanes and CCB modules are designed to account for path-length delays so each trigger module receives the clock at the same point in time.

Clock, bunch-crossing-reset, and bunch-crossing-zero signals are distributed from the CCB to the trigger modules. Each trigger module will maintain an internal counter that increments every clock cycle. When a bunch-crossing-reset signal arrives, the counter halts, and resets to its initialization value. Counting resumes when the bunch-crossing-zero signal is received.

The CCB can generate and distribute the clock, bunch crossing reset, and

several other fast control signals including the Level 1 trigger accept. It can also derive these signals from the TTC system [6]. For the results described in this report the TTC system was not used, and the 40 MHz clock was taken from the quartz oscillator on a CCB board.

The clock signal is distributed to the SP and SR modules in the crate via its custom backplane. The phase of each clock signal distributed over this backplane can be adjusted with 2 ns step accuracy with respect to the main master clock individually to each slot in the crate. There is also the possibility to send just a single 25 ns clock pulse to all modules in a crate.

5 Muon Port Card

The high cost of optical links makes it prohibitively expensive to send every LCT from the TMBs to the counting room, and the huge number of possible LCTs would greatly increase the complexity of the Track-Finder. Thus, a Muon Port Card (MPC) is used to reduce the data. In each of stations 2, 3, and 4, a MPC receives signals from 9 chambers corresponding to 60 degrees in ϕ in one station. In station 1, a MPC receives signals from 8 chambers² corresponding to 20° in ϕ . Each MPC in stations 2, 3, and 4 reduces the number of LCTs to three or less and sends them to the Sector Receiver (SR) module via optical links. In station 1, the number of output LCTs is two or less.

Fig. 5 contains a block diagram of the MPC, which performs the following

² We also have the flexibility for a MPC in station 1 to receive signals from 9 chambers corresponding to 30° in ϕ , if triggering is limited to $|\eta| < 2.1$.

functions:

- (1) Data collection. The MPC receives data from nine TMB every bunch crossing. Each TMB sends up to two LCT patterns. Thus, up to 18 LCT patterns may come to a MPC simultaneously.
- (2) Synchronization of incoming LCTs with the MPC local master clock.
- (3) LCT selection. The MPC selects the best three LCTs out of 18 possible, except in ME1 where two LCTs may be selected out of 16 possible.
- (4) Reformatting of the three selected LCTs and their transmission to SRs via G-Link protocol (labeled GL) over optical links.

When the LCTs are sent from the TMB to the MPC, they have a phase shift with respect to the local clock at the destination, and must be synchronized. Also, there are separate bunch crossing counts accompanying each of the 18 LCTs. These are compared to the Port Card bunch crossing counter to detect errors.

5.1 Selection Logic

The flexible selection logic is based on Look-Up Tables (LUT) implemented in an Altera EPF10K200E PLD. Pattern identifiers from all incoming LCTs serve as addresses for the LUT, and the LUT output represents a quality factor corresponding to a particular combination of wire and strip patterns. Currently we are allowing up to 11 bits to be used to address the memory, of which the lower 8 bits are the CLCT pattern number and two higher bits are the ALCT quality number. One bit is unassigned. The LUT output is currently an 8 bit number representing the most significant bits of the product

of the two pattern/quality numbers. This output of the LUT is arbitrary and reprogrammable allowing us to modify the function as we gain experience under real running conditions.

5.2 *Interface to Sector Receiver Card*

The distance between on-chamber electronics (FEBS, MBs, MPC) and the counting room is about 100 m. The MPC must be able to transmit 120 bits of data every 25 ns. Optical links are the best and possibly the only choice for communication between MPCs and SRs. The general requirements for these optical links are:

- (1) Simplex links, i.e, uni-directional communication through the optical links.
- (2) 25 ns framing to match the 40 MHz master clock.
- (3) Simple error detection, no error correction.

Each MPC contains parallel to serial converters and optical transmitter modules, while each Sector Receiver (SR) contains optical receiver modules and serial to parallel converters. For these prototypes we used the Hewlett Packard HDMP-1022/1024 serializer/deserializer (G-Link) chip set. This chip set has user-selectable parallel data widths (16, 17, 20, or 21 bits) and high-speed serial data rates. The specified bit error rate is less than 10^{-14} . For the prototypes, we selected 20 bits of data per frame, which along with 4 bits of frame header resulted in a rate of about 1 Gbit/s during the 25 ns (1/40.08 MHz) of frame transmission. We transmitted the required 120 bits of data per MPC by using six sets of serializer/deserializer chip sets, Methode MDX-19 Transmit-

ter/Receiver optical modules, and optical fiber. Our transmission rates were safely within the specifications, and the system performance confirmed expectations of reliability based on our bench tests, which had no bit errors over days of continuous testing.

Due to the limited number of inputs/outputs available at the main processing Programmable Logic Device, this Muon Port Card prototype receives data from up to three Trigger Motherboard prototypes (rather than 8-9 foreseen in the production version), performs sorting and selection of up to 3 best muons out of 18, and transmits data representing those best three muons to a Sector Receiver (SR) board over the six optical links.

In addition to the main sorter logic, two groups of FIFO buffers are implemented to test the MPC internal logic and its communication with the Trigger Motherboards (TMB) over Channel Links and with the Sector Receiver (SR) board over optical links. The MPC testing circuitry consists of two independent groups of FIFO buffers: an input FIFO which can be used to input muons stubs into the board and an output FIFO which can be used to examine the results of the sorting logic. Test patterns representing six muons can be transmitted simultaneously from all input FIFOs to the G-Link transmitters and further to the SR at 40 MHz upon a VME command.

Data communication was successfully tested between the TMB prototypes (1999 version) and MPC by loading pass-through logic in the sorting Programmable Logic Device. LCTs were input from the TMB over Channel Links and then read back from the Port Card via the output FIFO over VME.

6 Sector Receiver

The basic elements of the SR are shown in Fig. 6. Each Sector Receiver (SR) receives via optical links the Local Charged Track (LCT) information for 3 muons from each of two Muon Port Cards (MPCs) (except for the first station, where 2 muons from each of three Muon Port Cards are received). Thus, there are 12 optical fibers entering each SR. This information is then synchronized and reformatted within the SR (via look-up tables) into angular variables for the muons: the azimuthal angle ϕ , the local slope angle in ϕ (ϕ_b), and the pseudo-rapidity η . These data, along with bits summarizing muon quality and other diagnostic information are then communicated to the Sector Processor and the (barrel muon) DT Track-Finder in the (differing) format expected by each. Complete input information is also stored for readout by the DAQ system for accepted events. In addition, a VME-readable counter and log of detected hardware errors is foreseen, but was not included in the prototype.

Each half of a SR can receive 6 muons: either 2 muons from each of 3 MPCs in a 60° sector, or 3 muons from each of 2 MPCs in a sector. For each sector in the current prototype architecture, there are:

- (1) A SR receiving data from the three MPCs from ME1
- (2) A SR servicing the MPCs from each of ME2 and ME3
- (3) A half-used SR servicing the MPCs from ME4, assuming the scenario in which this fourth CSC station is built.

A single SR design has the flexibility to handle these cases; three such prototype boards were thus built.

6.1 Backplane inputs

The SR gets its clock and control signals from the CCB off the backplane. The SR maintains an internal bunch crossing counter which is incremented each clock cycle. With the arrival of a RESET signal, the counter halts and re-initializes to a preset value. It then starts counting upon receipt of the bunch-crossing-zero (BC0) signal. The 5 least significant bits of this locally determined bunch crossing number are compared to the BXN arriving from the MPC, and an error condition results if they are different.

6.2 Sector Receiver Outputs to Trigger Path

There are two separate streams of trigger outputs from the SR, one to the SP via the backplane, and one to the DT Track-Finder via (not-yet-prototyped) transition modules and cables. These output streams are similar but are customized for each recipient. They contain: the locally-measured muon track segment variables ϕ and η ; the local slope in the bending view, called ϕ_b ; an accelerator muon bit that is simply copied from the input from the MPC; and quality bits computed from MPC inputs as described below. For each set of 3 muons coming from a MPC, a “CSC tag” encodes in 2 bits which pair of muons, if any, had a common CSC ID (i.e., came from the same chamber); this information helps resolve ambiguities in combining anode and cathode views. Finally, an Error bit is set if the data is invalid, for example if an optical link error has been detected.

6.3 Sector Receiver Outputs to DAQ Path

The SR will store all incoming data in a buffer for a time long enough (several μs) so that the DAQ system can read it for accepted events. The data will be transmitted from the SR to a Front-End Driver using an optical link.

Another buffer will contain a VME-readable error counter and error log, with bunch crossing number and error type for any errors found. Error conditions detectable by the SR include: the above-mentioned mismatch in BXN; a set error bit in data from the MPC, indicating error further upstream; and error bit provided by the HDMP chipset, indicating loss of synchronization in the optical link.

In the prototype, buffers storing such information were implemented, but transmitting chips were not included.

6.4 Front FPGA

As discussed above, the data from the MPCs arrive on optical cables, and is de-serialized, forming a 120-bit-wide data set arriving from each MPC each beam crossing. The data are latched into the Front FPGA with clocks derived from the CCB-derived 40-MHz clock. Data arriving on separate links can be re-synchronized by programmable delays within the FPGA.

For maximum flexibility, the Front FPGA is connected to all address lines of the muon's first stage of memory lookup tables, to the DAQ output path, and to the SR's VME interface. The Front FPGA keeps a copy of the incoming data in a buffer several μs deep for readout via DAQ. For diagnostic purposes,

the Front FPGA can insert test data into the Sector Receiver, simulating data arriving from the MPC, either in single-event-mode, or burst-mode at 40-MHz for 256 beam crossings. Finally, the Front FPGA contains logic for downloading the LUT contents via the VME interface.

6.5 *Memory Look-up Tables*

The LUT functions are shown schematically in Fig. 7. In this prototype, 6 identical 256K by 16 bit memories are used for each of the 6 muons. In the first stage, the cathode LCT information is translated into local or approximate values of ϕ and ϕ_b , and anode LCT information is translated into the approximate η . In the second stage, each coordinate is corrected using information from other coordinates. The second stage also corrects for any alignment problems as well as slanted anode wires. In addition, a sixth LUT is used to compute quality bits.

The 8-bit “1/2 strip ID” corresponds to a coarse ϕ position at layer 3 within a particular 6-layer station (ME1–ME4). For a track traversing this station at an angle, the true ϕ depends on the depth within the 6 layers. Furthermore, at each station, chambers alternating in ϕ are overlapped, with “front” chambers closer to the interaction region than “back” chambers. The Sector Processor can function most effectively if the ϕ passed to it is at a conventional distance from the interaction region. In the first LUT, such a ϕ is computed, using in addition: the 8-bit “CLCT pattern” which encodes which strip pattern was recorded in the 6 layers (and which also carries information for decoding the “1/2 strip ID”); the “L/R Bend” bit, and a “Front/Rear chamber bit” which is derived in the Front FPGA from the 4 CSC ID bits. The resulting “local

ϕ'' is 10 bits, in half-strip units, spanning only that particular chamber. From the same LUT also comes a local ϕ_b , which with 6 bits encodes the change in ϕ between layer 1 and layer 6, in fractional strip units, inferred from the CLCT pattern. (Although there are 256 possible CLCT patterns, many of them correspond to identical values of ϕ_b .) In the prototype, only a small fraction of these patterns were loaded, and hence the ϕ_b information was not exploited in the Track-Finding.

In the other first-stage LUT, the approximate 6-bit η is computed from the 7-bit ALCT wire group (WG) and the 4-bit CSC ID (which is necessary since the chambers are at different radii from the beam line and since the wire grouping depends on the chamber). Unlike the first-stage local ϕ , this η is already global, although still requiring correction in the second stage. In this LUT, we also use some of the extra output bits to pass on an in-time copy of the 4 CSC ID bits to the second stage LUTs.

In the second-stage LUTs, four independent quantities are calculated:

- (1) For the SP, a 12-bit global ϕ is computed from the 10-bit local ϕ using the CSC ID, with alignment corrections also possible using the most significant 4 bits of η from the first stage.
- (2) For the DT Track-Finder, a similar 12-bit global ϕ is computed independently in order to provide for coordinate conventions different from the SP.
- (3) For the SP, a 5-bit corrected ϕ_b with a common scale is computed from the local value in fractional strip units. This requires the CSC ID and η since the strip width depends on the chamber and on the position along the strip.

- (4) For the SP, the 6-bit corrected η is computed from the first-stage η . This is corrected using the 2 most significant bits of local ϕ from the first stage, primarily to account for slanted anode wires in ME1/1. The (essentially negligible) ϕ -dependence of η along other anode wires can also be corrected for, at no cost.

Items (1) and (2) each have a dedicated LUT, while items (3) and (4) are combined into one LUT.

For each muon, 3 quality bits are passed to both the DT Track-Finder and the SP. They are functions of the following inputs to the SR: the Valid Pattern flag, the cathode pattern number, the anode pattern quality, the ALCT/CLCT BXN match, all 4 TMB status bits, the incoming error bit, as well as the SR's internally generated error flags.

6.6 Back FPGA

After the second LUT stage, the data go directly to both the Back FPGA and the Channel Link chips for transmission to the SP on the backplane (or to SP functions on the same board). Since the Back FPGA is connected to all output signals as well as the VME interface, there is flexibility for various diagnostic tests, all run at 40 MHz. In a typical test, the Back FPGA spies on the data from 256 events as it is sent to the Sector Processor. For more specialized tests of the SR-SP interface, 256 events can be loaded into the Back FPGA buffer and then clocked out to the SP. These capabilities facilitated debugging of both the SR and the SP. As with the Front FPGA, the Back FPGA is used to load and read the memory LUT contents.

6.7 VME and JTAG Interfaces, and Operational Modes

The VME interface is in a FPGA near the backplane. This FPGA also contains miscellaneous logic such as the bunch crossing counter. It drives a serial controller for servicing the Front and Back FPGAs using JTAG. There is also a front-panel JTAG connector for bench tests. Currently, we use it to load the EEPROMs at the top of the board; the FPGAs themselves are then loaded from the EEPROMs.

The SR has VME addressable registers to define various modes for reading and writing to memory LUTs, for normal operation, and for test modes. The number of clock cycles per start command and various clock delays are all VME-programmable. Depending on the mode, access to the memory LUT address and data lines is reconfigured using tri-state and bi-directional buffers.

6.8 SR Construction

In order to test the Sector Processor with a full complement of inputs, three prototype Sector Receivers for the CSC Track-Finder were built and tested. The design has 10 layers and about 9400 vias. The (thirteen) Front, Back, and VME Interface FPGAs were implemented in Xilinx Virtex FPGAs, part number XCV50-6BG256C.

The memory LUTs were initially implemented in 36 identical 256Kx16 asynchronous static RAMs, GSI part number GS74116TP. The use of asynchronous static RAM allows the output of the second-stage RAMs to appear as soon as the inputs to the first-stage RAM propagate freely through the chips. Two of

the SR prototypes were built with 8-ns RAM, the fastest available, to guarantee that the entire propagation through the two chips could take place within one cycle at 40 MHz. The third prototype was built with 10-ns RAM, which worked equally well in all tests. However, with even the faster RAM chip a rare condition was identified in which an error occurred if the addresses input to the second-stage LUTs were the same on consecutive clock cycles, while the addresses input to the first-stage RAMs were different. This behavior, which we could not explain using the data sheets and measured timing, disappeared when we substituted the equivalent ASRAM part from IDT.

Xilinx EEPROMs load all FPGAs upon power-up. Front-panel LEDs display the status of a number of internal and VME bits.

7 Sector Processor

A block diagram of the Sector Processor logic is shown in Fig. 8. The reconstruction of complete tracks from individual track segments is partitioned into several steps in the Sector Processor to minimize the logic and memory size. First, the data are latched and synchronized in the Bunch Crossing Analyzer. Then, nearly all possible pairwise combinations of track segments are tested for consistency with a single track in the Extrapolation Unit. The Track Assembly Unit assembles complete tracks from the extrapolation results, and cancels redundant tracks so that the number of distinct muons can be reported. Finally, the best 3 muon candidates are selected by the Final Selection Unit, and the track parameters are measured in the Assignment Unit.

7.1 *Bunch Crossing Analyzer*

The input data to the Sector Processor from the DT and CSC trigger systems are synchronized to the local clock before being sent to the Extrapolation Units. It is envisioned that the design should include some ability to analyze track segments received in out-of-time bunch crossings, since the bunch crossing assignment is not 100% accurate and since it will be easier to commission the system when cable delays are not exactly known. Such a multi-bunch mode can take advantage of the sparseness of the data, since if the data are not sparse, the CSC track segments would be lost already after sorting in the Muon Port Card. However, this capability has not yet been tested in the current prototype.

7.2 *Extrapolation Unit*

A single extrapolation unit forms the core of the Track-Finder trigger logic. It takes the three-dimensional spatial information from two track segments in different stations, and tests if those two segments are compatible with a muon originating from the nominal collision vertex with a curvature consistent with the magnetic bending in that region. All possible extrapolation pairs should be tested in parallel to minimize the trigger latency. However, we have excluded direct extrapolations from ME1 to ME4 in order to reduce the number of combinations and to reduce some random coincidences (since those chambers are expected to have the highest rates). The exclusion also facilitates track assembly based on key stations, which is explained in the next section.

The extrapolation unit is composed of several sub-units which analyze the

η coordinates of the two track segments from different stations, the ϕ coordinates, and the quality of the resulting extrapolation. These sub-units are described below.

7.2.1 *Eta Road-Finder*

The tests involving the η information from the two track segments are the following:

- Determine if each track segment is in the allowed trigger region in η
- Compare the η values of the two track segments to determine if both lie along a straight line projection to the collision vertex within a certain tolerance
- Check that the bend angle in η for at least one track segment is consistent with a track originating from the collision vertex. Currently, only one bit (the Accelerator Muon bit) is used to flag if a track segment is parallel to the beam axis rather than projective.

7.2.2 *Phi Road-Finder*

The tests involving the ϕ information from the two track segments are the following:

- Compute the difference in ϕ between the two track segments
- Check that the difference in ϕ is consistent with the bend angles in ϕ_b measured at each station
- Compare the difference in ϕ to the maximum allowed at that η . Several thresholds may be employed to provide a coarse p_T measurement.

7.2.3 *Quality Assignment Unit*

The final quality assignment for the extrapolation is based on the bits from the η and ϕ road-finder units as well as the track segment quality bits. It is generated by a small look-up table. The resulting quality word is either 1 or 2 bits, depending on the stations involved. Its definition is programmable, but we use it to assign a coarse p_T (low, medium, and high) to extrapolations involving the first muon station. Otherwise, the quality just represents whether the extrapolation was successful or not. The expected p_T resolution for a ϕ resolution of 10 bits is about 30% when ME1 is involved. The quality word is used later when muon candidates are sorted.

7.3 *Track Assembly Unit*

The track assembly stage examines the output of the extrapolation units and determines if any track segment pairs belong to the same muon. If so, those segments are combined and a rank is assigned based on the muon stations involved. The identification of the participating track segments is registered also.

The underlying feature of a Track Assembly Unit is the concept of a “key station”. For this Track-Finder design, ME2 and ME3 are key stations. A valid trigger in the endcap region must have a hit in one of those two stations. In this way, the output of the extrapolation units can be separated into three data streams: one for patterns keying off ME3, one for patterns keying off ME2 in the endcap region, and one for patterns keying off ME2 in the DT/CSC overlap region. Only ME2 is used as a key station in the overlap region, since

ME3 has no coverage there and ME1 has twice as many track segments. Some muons will be found by more than one stream, so the Final Selection Unit described in the next section must resolve the double counting.

Each track segment of a key station, of which there are three each for ME2 and ME3, is tested for extrapolations to the other stations. Therefore, the extrapolation results appropriate for that key segment are interrogated. The Track Assembler logic checks if the key track segment has successful extrapolations to more than one station. The output of this logic is a code designating the best track pattern which contains the given key segment. Thus, up to three tracks may be found per data stream, 9 total for all three streams.

There are six track segments allowed in ME1, and the extrapolation quality to ME1 is 2 bits. There are three track segments allowed in each of the other non-key stations, and the extrapolation quality to those stations is 1 bit. Thus, a total of 18 bits are interrogated. Since the number of input bits is small, each of these “Link” units can be implemented as a static RAM look-up memory. The latency, therefore, is just one beam crossing. The output code is a 9-bit word labeling the track segments used in each station (*e.g.* 3 bits for ME1, 2 bits each for ME2–ME4), and a 6-bit quality word giving the type and rank of the assembled track for later sorting purposes.

7.4 *Final Selection Unit*

The final selection logic combines the information from the Track Assembler streams, cancels redundant tracks, and selects the three best distinct tracks. For example, a muon which leaves track segments in all four CSC stations will

be identified in both track assembler streams of the endcap since it has a track segment in each key station. The Final Selection Unit must interrogate the track segment labels from each combination of tracks from the two streams to determine whether one or more track segments are in common. If the number of common segments exceeds a preset threshold, the two tracks are considered identical and one should be canceled (presumably the lower rank combination, if the two tracks are not completely identical). Thus, the Final Selection Unit is a sorter with cancelation logic. It sorts and cancels 9 tracks down to 3 since there are two endcap data streams and one overlap data stream.

A block diagram of the Final Selection Unit is shown in Fig. 10. The sorter part of the logic compares the qualities of all pairwise combinations of tracks from the Track Assembler streams. The cancelation part of the logic does the same for the hit labels. Not all track segments need to be identical for two tracks to be considered identical. Bremsstrahlung, for example, might cause a single muon to deliver two track segments in one station, and this would lead to a fake di-muon trigger which should be suppressed. The actual criterion employed is programmable.

7.5 Assignment Unit

The Sector Processor measures the momentum of the identified muons in the final stage of processing. This includes the ϕ and η coordinates of the muon, the magnitude of the transverse momentum p_T , the sign of the muon, and an overall quality which we interpret as the uncertainty of the momentum measurement. The p_T and the track quality are combined into an overall rank before transmission to the Muon Sorter. The coordinates are to be reported

at the second station, since this is convenient for later association with RPC trigger data in the Global Muon Trigger. This is also convenient for the Track-Finder because the muon track parameters do not need to be extrapolated back to the interaction point, which would be prone to errors.

The most important quantity to calculate accurately is the muon p_T , as this quantity has a direct impact on the trigger rate and on the efficiency. Simulations have shown that the accuracy of the momentum measurement in the endcap using the displacement in ϕ measured between two stations is about 30% at low momenta, when the first station is included. (It is worse than 70% without the first station because of the reduced magnetic field through the outer iron disks) We would like to improve this so as to have better control on the overall muon trigger rate, and the most promising technique is to use the ϕ information from three stations when it is available. This should improve the resolution to at least 20% at low momenta, which is sufficient. (The best momentum resolution possible from an offline standalone muon measurement in the endcap is 15% [1].) We take advantage of the large multiple scattering for low p_T muons. Although there is a small probability that a scattering will offset the large magnetic bending between the first two stations (and thus appear as a high momentum muon), it is much less likely to offset the bending between all three stations.

The first step of the 3-station p_T measurement is to do some pre-processing in FPGA logic: the difference in ϕ is calculated between the first two track segments of the muon, and between the second and third track segments when they exist. Only the essential bits are kept from the subtraction. The subtraction results are combined with the η coordinate of the track and the track type, and then sent into a megabyte-sized memory for assignment of the track

rank (p_T and quality) and sign. Tracks composed of only two track segments are allowed also in certain cases. This scheme is illustrated in Fig. 11 for the parameter assignment of one muon. Three such units are necessary for the three best muons selected by the Final Selection Unit.

The 2-bit quality assigned to a muon reflects the uncertainty in the p_T assignment. Specifically, the highest quality is assigned to tracks that have segments in 3 or 4 CSC stations, including ME1, since the best resolution is possible. Medium quality is assigned to tracks that have segments in only two stations, of which ME1 must be one. Finally, lowest quality is assigned to all tracks that do not include ME1, since only a very poor p_T resolution is possible in the weaker magnetic field of the outer iron disks.

7.6 *SP Construction and Operation*

The hardware implementation of the Sector Processor trigger logic is listed below.

Bunch Crossing Analyzer: The logic of the Bunch Crossing Analyzer is partitioned across 7 moderately-sized FPGAs from the Xilinx Virtex series (XCV50-6BG256C).

Extrapolation Units: The extrapolation logic, as well as the global FIFO which stores the information for the Assignment Unit, occupies 4 large Xilinx Virtex FPGAs (XCV400-6BG560C).

Track Assembler Units: The Track Assembler Units are realized with nine 256Kx16 SRAM memory chips from Integrated Device Technology.

Final Selection Unit: The Final Selection Unit is implemented in one Xilinx Virtex FPGA (XCV150-6BG352C).

Assignment Unit: The Assignment Unit is implemented in three Xilinx Virtex FPGAs (XCV50-6BG256C) and three 2Mx8 SRAM memory chips from Toshiba.

In addition to the fast trigger logic, a Xilinx Virtex FPGA makes up the VME interface for the board, and a parallel-to-serial interface chip (SCANPSC100F) from National makes up the JTAG interface used to program the FPGAs. Configuration of the FPGAs via JTAG, including the VME interface, takes advantage of the VME parallel data transmission using the National chip, and the total configuration time is reduced to 6 seconds from approximately 6 minutes using the standard Xilinx Parallel III cable.

In total, 17 Xilinx FPGAs with a ball-grid array footprint, 12 memory chips, and 25 32-bit buffers were used. The entire board was routed using 12 layers and approximately 10,000 vias. A front panel connector provides the SP output in LVDS.

8 Stand-Alone and System Tests

The critical functions of the CSC Track-Finder prototypes (SR, SP, and CCB), as well as the MPC were tested using the custom backplane during the summer and fall of 2000. The CCB prototype was used to distribute clock and control signals to each board. In particular, the CCB issues a BC0 to initiate the start of a chain test between two or more prototypes. Tests followed the natural evolution of increasing board-to-board interaction complexity, as follows.

MPC Functionality

After verifying communication between all locations on the board and the host computer, the sorting logic was successfully tested by loading many millions of test patterns into the input FIFO and reading the results of the sorting logic from the output FIFO.

SR Functionality

For stringent standalone tests of the Sector Receiver, we used pseudo-random numbers for all LUT contents and event data. Events were loaded into the Front FPGA in groups of 252, passed through the SR at 40 MHz, and read out of the storage buffer in the Back FPGA. Perfect agreement was achieved between the expected and observed data for more than 30,000 cycles. For tests involving the Sector Processor, data and LUT contents were derived from a full CMS detector simulation in order to test the track-finding algorithms. This typically tests only a small subset of all the SR memory addresses, however, and is not as stringent as the pseudo-random test.

SP Functionality

All the track-finding algorithms of the Sector Processor have been tested dynamically at 40 MHz, except for the Bunch Crossing Analyzer which was configured as an input FIFO for the tests. In particular, perfect agreement was achieved between the simulation and the hardware for approximately 200,000 simulated single muon events. Moreover, agreement also was achieved when the same events were piled-up three at a time to mimic triple-muon events, which is a stronger test of the track assembly and sorting functions on the board. Pseudo-random numbers also were tested successfully.

MPC to SR Optical Communication and Data-Flow Tests

After a SR passed its standalone tests, a Muon Part Card was connected to it with 100 m optical fibers driven and received by HP G-Links. Unsorted tracks were put into a buffer in the front of the MPC. These were clocked through the MPC, with the sorted highest-priority tracks sent to the SR, where they were ultimately recorded by the Back FPGA. No errors were encountered using pseudo-random or simulated muon data in tests involving up to 1.6 million events and exercising two different crates.

SR to SP Backplane Communication

The integrity of the data sent from two SR prototypes (corresponding to stations ME2–ME4) to the SP prototype through the custom Channel Link backplane operating at 280 MHz has been verified. A FIFO in either the input or output of each SR can be loaded with data 256 bunch crossings (bx) deep.

Three SR's to SP Test

At the time of the tests, it was foreseen to have one SR servicing ME1, a second servicing ME2 and ME3, and (half of) a third servicing ME4. Thus, we configured the three prototype SR's in this way, and loaded simulated MPC data into the Front FPGA of the SR's. The SP reconstructed the full muon tracks, consistent with the expectation from simulation.

Full MPC to SR to SP Test

The entire trigger path from the MPC to the SP has been tested successfully using simulated muons from the standard CMS offline package as input. Two MPCs representing ME2 and ME3 of one trigger sector sent data to one

SR, which in turn re-formatted and transmitted the data to one SP. The SP successfully reconstructed tracks in agreement with the simulation.

System Latency

System latency (transit time for signals and calculations) is most conveniently expressed in LHC in bunch crossings (bx), each approximately 25 ns. In our tests, 20 bunch crossings were required for transit of the optical fiber, whereas in the actual experiment, a shorter fiber 18 bx in length is foreseen. Assuming the shorter cable, the latency of the tested system from the input of the MPC (after de-serialization) to the output of the SP (before serialization) was 47 bunch crossings (bx), broken down as follows: 5 bx for MPC processing, 1 bx for HP G-Link serialization, 18 bx for transmission through the optical fiber, 3 bx for HP G-Link de-serialization and resynchronization to the local (crate) clock in the SR, 1 bx for SR processing, 4 bx for Channel Link serialization/de-serialization and transmission over the custom backplane, and 15 bx for SP processing. As discussed below, this latency must be reduced in the final system, and this should already be possible with advances in technology which occurred during construction and testing of the prototype system.

9 Conclusion and Future Plans

We successfully designed, built, and tested a prototype trigger system that employs 3-D track-finding algorithms in order to identify muons in the CSC muon system of CMS. Four distinct digital boards clocked at 40 MHz were developed, and were connected together either by optical links or by a custom backplane operating at 280 MHz. The designs make use of field-programmable

gate-arrays and memory look-up tables, and thus are very flexible. Tests of the hardware were in complete agreement with a bit-level offline simulation.

Despite the success of these prototypes, the overall latency of the CSC trigger, including prototypes of front-end trigger boards not described here, is approximately 20 ns too long to fit in the overall 3.2 μ s Level-1 latency. Therefore, further improvements and new technologies are under investigation. Specifically, the following design changes are foreseen:

- The new Texas Instruments TLK2501 gigabit chipset and the Finisar FTRJ-8519-1-2.5 optical transceiver have been successfully evaluated [7] and will replace the HP chipset. By using a higher operating frequency of 80.16 MHz in the serializer, which corresponds to 1.6 Gbps transmission across the optical link, we can reduce the number of serializers and optical modules on each MPC from 6 to 3. Moreover, 15 such modules can fit along the front panel of a single slot 9U VME board, allowing all the Sector Receiver circuitry for one sector to fit onto the same board as the Sector Processor. This consolidation allows us to build a compact single-crate system that houses all the Sector Receiver, Sector Processor, and Muon Sorter logic.
- The Channel Link backplane between the Sector Receiver and Sector Processor is not needed for the merged solution, which will remove the serialization latency. Instead, a point-to-point backplane based on GTLP logic levels and running at 80 MHz without a serialization penalty will be developed for communication between the Sector Processors and the Muon Sorter.
- The Sector Processor logic will be consolidated into a single high-density FPGA (*e.g.* Xilinx Virtex 2 series) from the current 15, enabling much faster performance [8]. This FPGA, and that for the Muon Sorter, will be placed on mezzanine boards to reduce the complexity of the main 9U boards and

to simplify future upgrades.

With all these improvements, we anticipate a reduction in the MPC latency from 5 to 4 bx, essentially unchanged latency for the optical path and associated serialization/deserialization, and a reduction of the SR-SP Track-Finder latency by about 14 bx. When combined with new lower-latency prototypes of the front-end trigger boards, this will meet our design goal.

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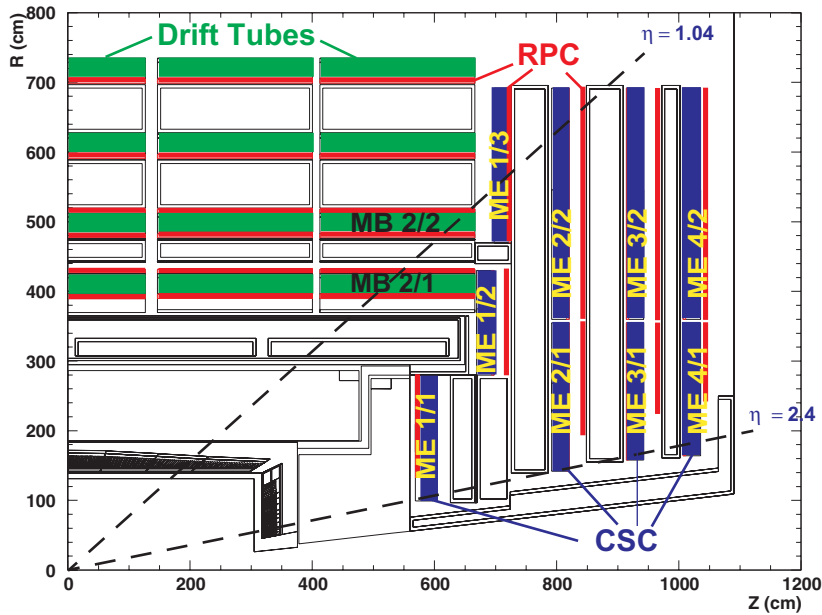


Fig. 1. Illustration of the CMS muon system showing division between the DT and CSC Track-Finders at $\eta = 1.04$.

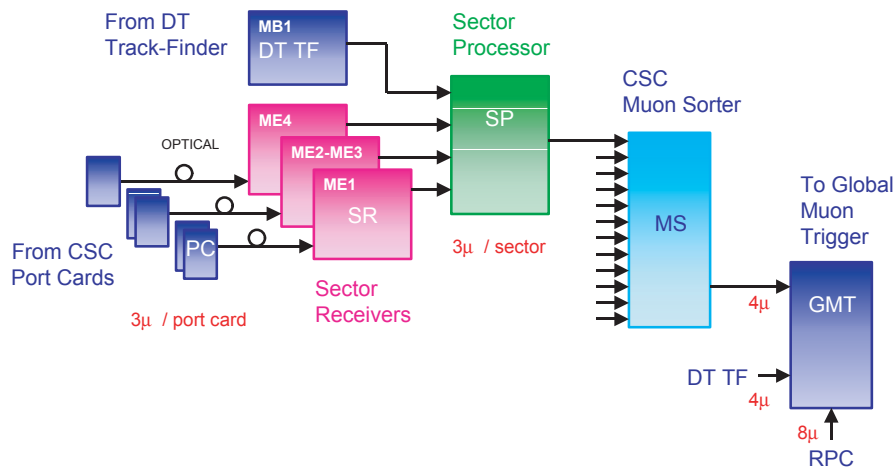


Fig. 2. Block diagram showing the connections among the the Muon Port Cards, CSC Track-Finder, Muon Sorter, and Global Muon Trigger.

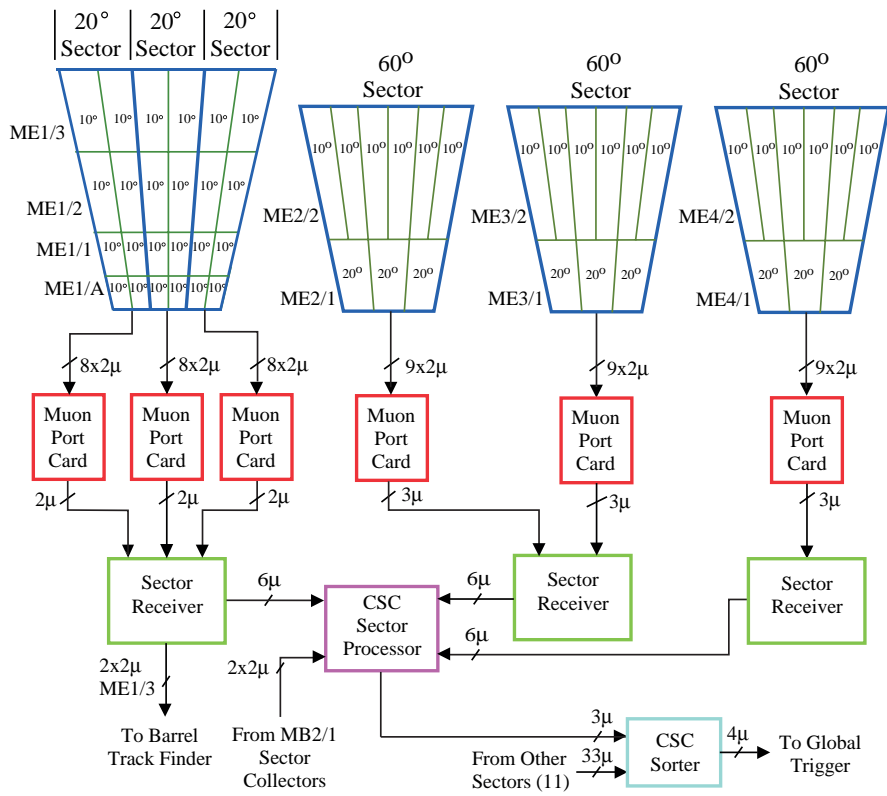


Fig. 3. The data mapping from CSC chamber-level LCT information into 60° sector information for the CSC Track Finder. Also shown are interfaces to and from the Barrel Drift Tube system for handling overlap regions.

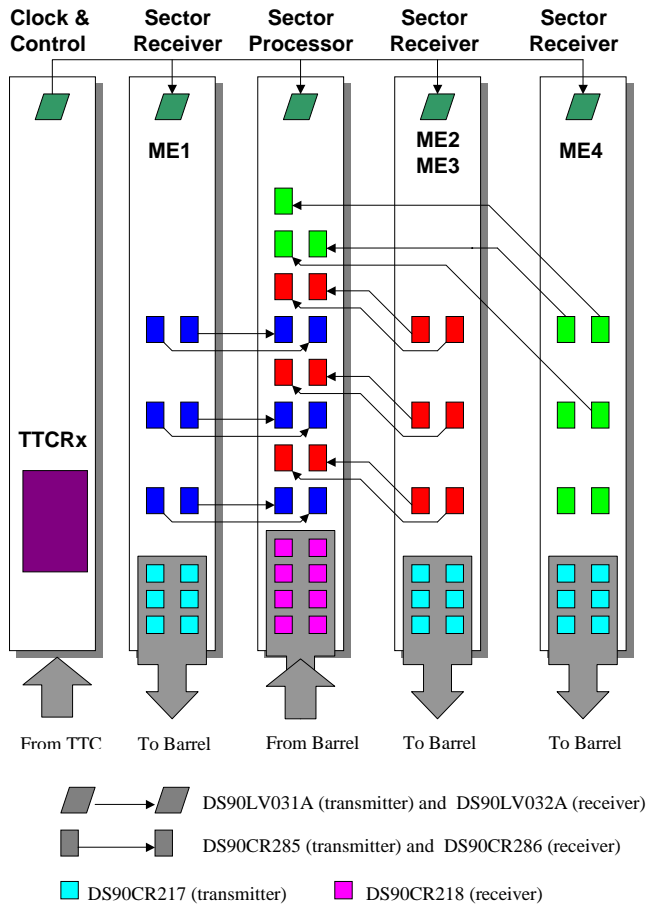


Fig. 4. Illustration of the card placement and backplane connections for one sector in the Track-Finder crate, according to current prototypes.

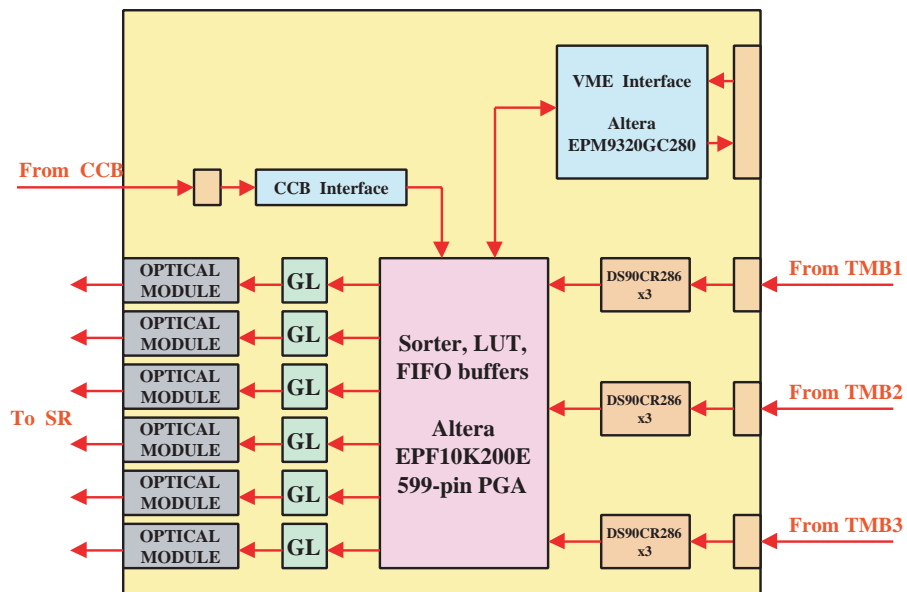


Fig. 5. Block diagram of the MPC prototype.

Sector Receiver Block Diagram

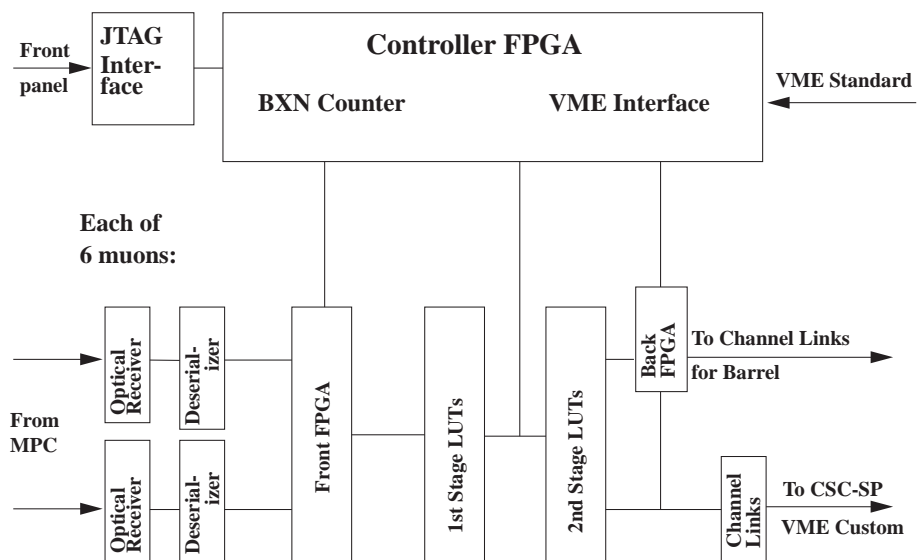


Fig. 6. Block diagram of the Sector Receiver logic.

SR Look-Up Tables
Six 256K x 16 RAMs

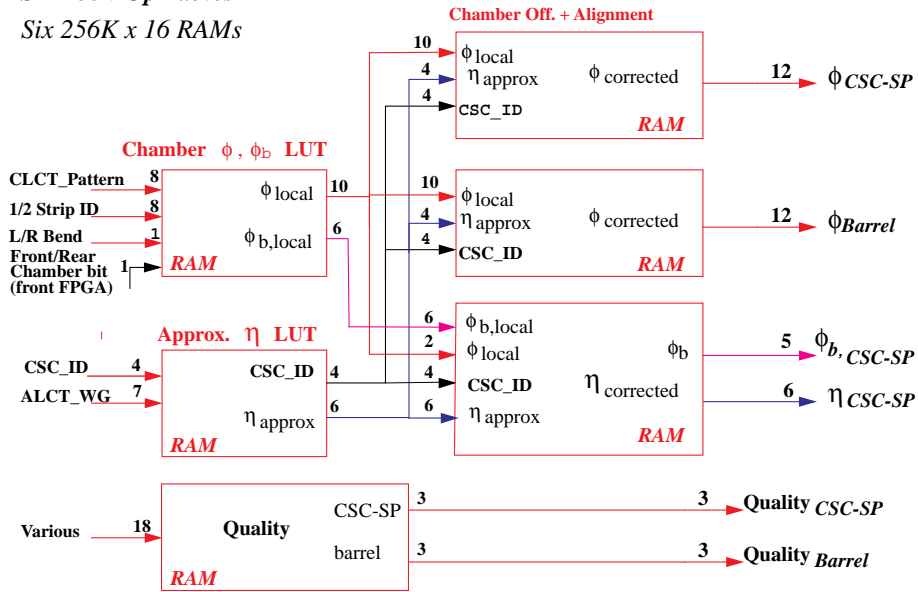


Fig. 7. Diagram of the Sector Receiver memory lookup table connections.

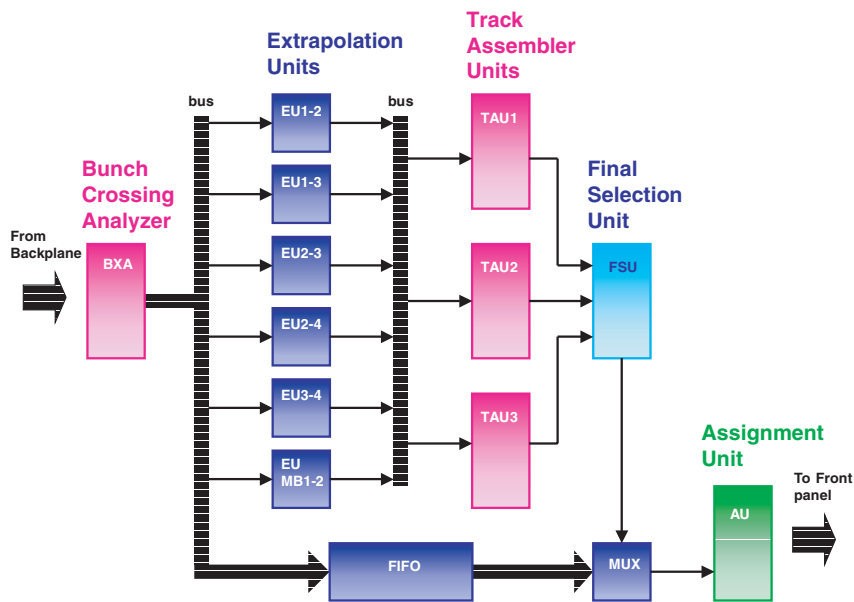


Fig. 8. Block diagram of the Sector Processor logic

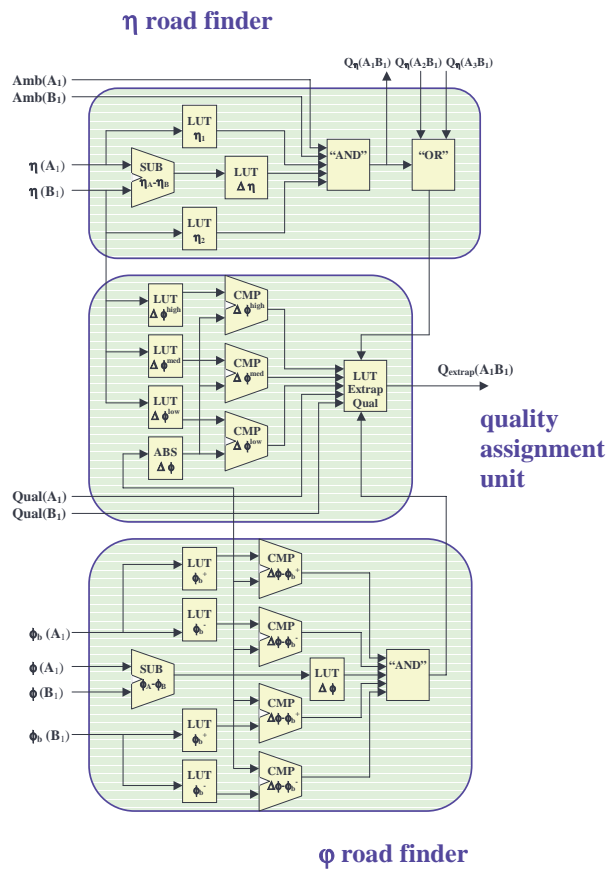


Fig. 9. Block diagram of the extrapolation unit logic, which compares a track segment in one station (A_1) with that in another (B_1).

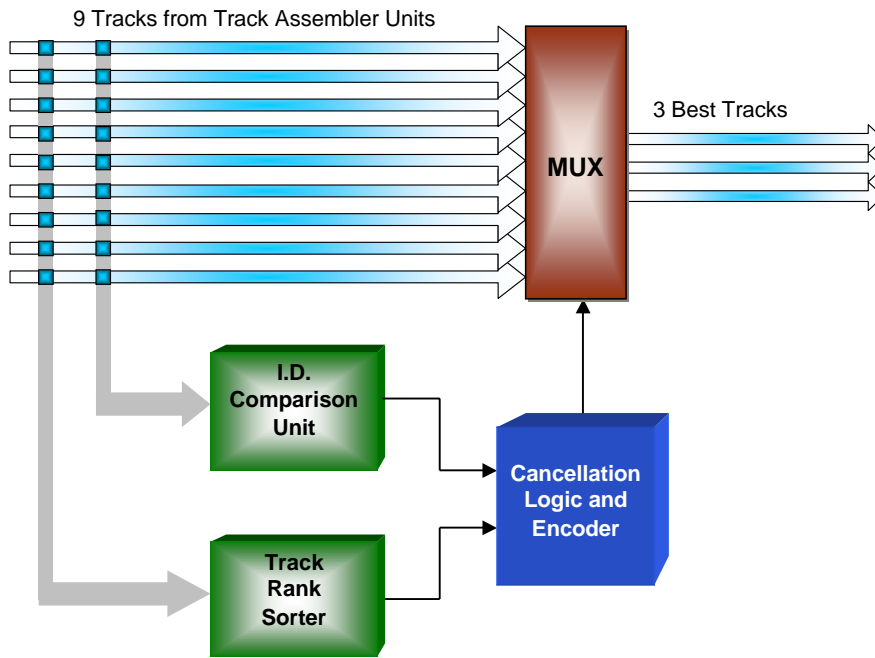


Fig. 10. Block diagram of the Final Selection Unit

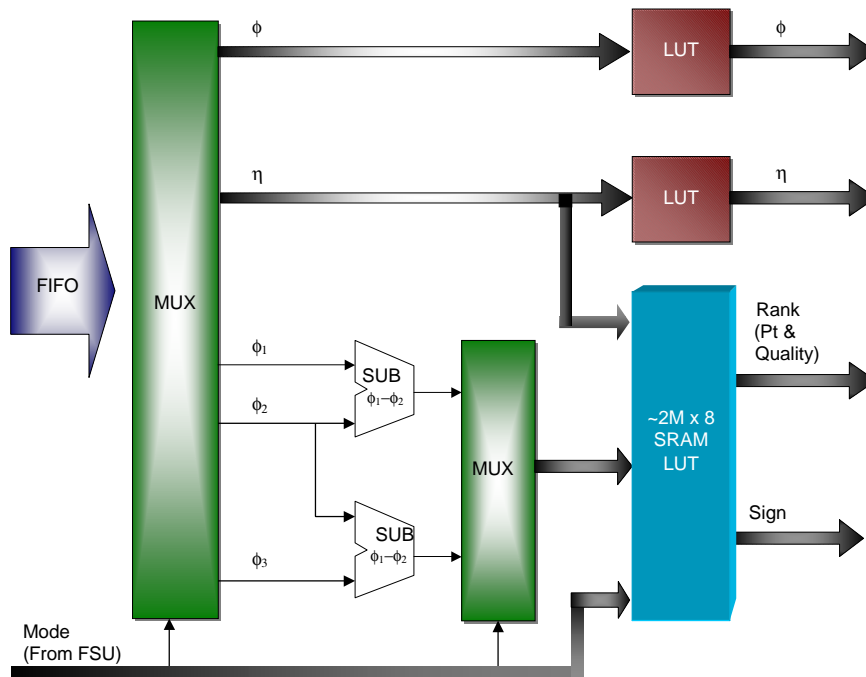


Fig. 11. Block diagram of the Assignment Unit for one muon.