From SP02 to SP04

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SP02 Design & Test Summary

Positive experience:

- ✓ Three SP02 cards have been fabricated and tested
- ✓ All performed tests are now successful, although there were problems before

There are still some tests to do
before declaring SP02 completely tested:
- test the DDU readout,
- test Fast Monitoring functionality,
- test multicast commands,
- test BLK VME access,
- test SP02 self-triggering

SP02 Fixes & Improvements Checklist

1. **Fix the DIN160 (VME connector) library schematic component, initially designed with mislabeling of pin rows.**

   History: After the SP02 #1 smoke test, four chips (VME buffers) did not pass because of this problem, and have to be replaced to put the card back into operation. The VME connector has been put on standoffs and wired to the board.

2. **Drive the TLK2501 reference clock from the on-board VCXO-based PLL clock (QPLL or QPLL substitute), and not from the Virtex II DCM clock.**

   History: The Virtex II DCM clock, due to its digital nature, experiences discrete phase shifts of the order of 50 ps and can NOT be used as a TLK2501 reference clock. A QPLL substitute has been developed and the SP02 clocking solution has evolved from a single 40 MHz to a pair of 40/80 MHz clocks on-board.

SP02 Fixes & Improvements Checklist

3. **Make provision for the on-board QPLL reference clock to be either 40 MHz or 80 MHz backplane clock**

   Detail: **The QPLL generates a free-running 40/80 MHz clock without the presence of the backplane clock and locks to it otherwise**

4. **Visualize QPLL Lock condition with a front panel LED**

   Detail: **Make the QPLL "Lock" signal available to VME**

SP02 Fixes & Improvements Checklist

5. **Redesign implementation of multicast VME commands to comply with the ANSI/VITA 23-1998 VME64 Extensions for Physics and Other Applications**

   Detail: The IACK* daisy-chain should be used to allow Slaves to indicate that they have successfully latched the data. When the token arrives at the LAST Slave it may respond to the Master with DTACK* (if it, too, has accepted the data).
   The token mechanism is not implemented at the moment.

6. **Replace a Through-Hole JTAG Connector for Xilinx Parallel Cable IV with an SMT one**

   Detail: Pins are short for a 93 mil board

7. **Fix mapping of five signals in the DT->SP interface**

   Detail: At the moment they are remapped in the firmware

SP02 Fixes & Improvements Checklist

8. **Make a three-bit hardwired chip ID for each FPGA**
   Make a six-bit hardwired card ID for each SP

   Detail: On the CSR_CID VME command,
   each FPGA returns its ID and firmware revision date.

9. **Put /OE pins of all MS/CCB/DT backplane transceivers under the control of VME_FPGA**

   Detail: Not critical, but may be useful in future

10. **Terminate the winner bit lines from the MS and tie the V_{REF} pin of the GTLP transmitters to 1V**

    Detail:

11. **Add ground test point hooks across the board and uncover signal pads on the solder side of the board**

    Detail: To facilitate board debugging with a scope, if needed

12. **More fixes / improvements to come -?**

SP02 Latency Budget

SPO2 Simulated Timing