APPARATUS AND DEMONSTRATION NOTES

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Synchronous analog I/O for acquisition of chaotic data in periodically driven systems

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A new data acquisition technique has been designed for measuring chaotic attractors in periodically driven systems. Analog output hardware generates a continuous periodic waveform used in the drive while analog input hardware digitizes one or more chaotic waveforms characterizing the system phase space variables. With both processes synchronized to a common clock, the construction of multiple Poincaré sections is reduced to the simple process of redimensioning the chaotic waveforms and taking slices in one of the array indices. The implementation described here is applied to an electronic Duffing oscillator running at 1.6 kHz and provides quality Poincaré sections in near real time.
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I. INTRODUCTION

Notwithstanding the continuing growth in the field of experimental nonlinear dynamics, data acquisition techniques capable of collecting complete phase space trajectories remain relatively rare. Here we describe a technique applicable to periodically driven systems and capable of continuously collecting phase space variables at points uniformly spaced along the drive waveform. The data acquisition system is demonstrated on a two-well Duffing oscillator circuit and collects data for ten Poincaré sections at drive frequencies up to several kHz.

Desktop computers equipped with multifunction data acquisition boards are commonplace equipment in many teaching laboratories.[1] These systems are capable of simultaneous waveform generation using a digital to analog converter and waveform acquisition using an analog to digital converter. Most importantly here, the two processes can be synchronized by properly configuring the signals that trigger the conversions. By driving a chaotic system with a periodic output waveform and synchronously measuring phase space variables with the input waveforms, chaotic trajectories can be acquired in a form that is well suited for the construction of multiple Poincaré sections and for the determination of fractal dimensions and Lyapunov exponents.

II. DUFFING CIRCUIT

The technique is applied to the double-well Duffing oscillator circuit depicted in Fig. 1. This circuit is simpler than one recently reported,[2] consisting of an LRC circuit and two AD633 analog multipliers[3] that generate the circuit nonlinearity from the capacitor voltage. The AD633 has differential inputs V_1 and V_2, a fixed coefficient: $V_{\text{out}}=V_1V_2/10$ V, and an output amplifier for applying an offset and/or a gain. The capacitor voltage is squared and given a negative offset in the first multiplier stage. The first stage output is multiplied in the second stage by the capacitor voltage and amplified to produce the cubic potential shown in Fig. 2.

Component values were $C=0.1$ μF, $L=0.12$ H, and $R=70$ Ω (inductor resistance alone) or 180 Ω (with an added 110-Ω resistor). A 50-kΩ trim pot was used for the offset voltage and a 10-kΩ trim pot for the gain circuit. The $\pm V_s$ voltages for the AD633 were from a ± 12-V potted supply.

With the sign conventions and variables as shown in Fig. 1, Kirchhoff's loop rule gives

$$v_0 \sin \omega t - \frac{q}{C} - Ri - L\frac{di}{dt} = av_c + bv_c^3, \tag{1}$$

where the first term represents the drive voltage and the right-hand side represents the voltage from the AD633 multipliers. The offset and gain pots were set once and gave $a=GV_0/10\text{ V}=-1.6$, and $b=G/100\text{ V}^2=0.08/\text{V}^2$.

Equation (1) can be cast in autonomous form as:

$$\frac{dq}{dt} = i, \tag{2}$$

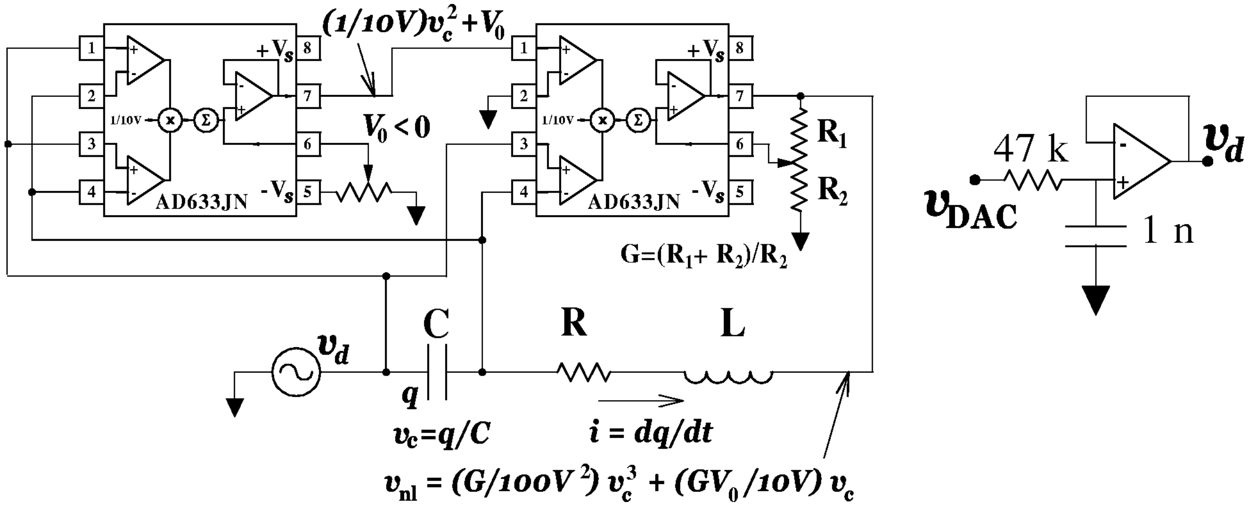

Fig. 1. Left: Duffing oscillator made from an LRC circuit and analog multipliers. Right: Drive circuit for the DAC-generated waveform.

$$\frac{di}{dt}=\alpha q-\beta q^3-\Gamma i+\epsilon\sin\theta, \tag{3}$$

$$\frac{d\theta}{dt}=\omega, \tag{4}$$

where

$$\alpha=-(a+1)/LC, \tag{5}$$

$$\beta=b/LC^3, \tag{6}$$

$$\Gamma=R/L, \tag{7}$$

$$\epsilon=v_0/L. \tag{8}$$

Equations (2)–(4) predict the dynamics for the three phase space variables, q, i, and θ.

With the drive off ($\epsilon=0$), the system has three fixed points—where $dq/dt=0$ and $di/dt=0$. Two at $q=q_\pm=\pm\sqrt{\alpha/\beta}$, $i=0$ are stable while one at $q=0$, $i=0$ is unstable. Expressing Eq. (3) as a first-order Taylor expansion about either stable fixed point then gives the damped harmonic oscillator equation:

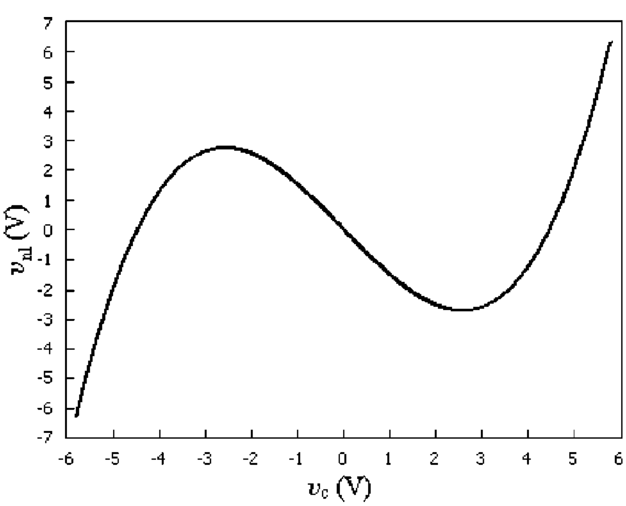

Fig. 2. Plot of the cubic voltage v_{nl} generated by the multiplier circuit at the top of Fig. 1.

$$\frac{di}{dt}=-2\alpha(q-q_\pm)-\Gamma i \tag{9}$$

and demonstrates that the resonant angular frequency for small oscillations about these points is $\sqrt{2\alpha}$. For the circuit parameters given, this corresponds to a frequency of 1.6 kHz. Chaotic behavior was obtained at several different drive frequencies including 1.6 kHz, which was used for all the data presented here.

The circuit was designed and its parameters were chosen to provide a good example with which to demonstrate the data acquisition technique and run it near the highest speed the hardware could accommodate. Relevant hardware characteristics and programming details will be presented by example with those used for this work. Variations needed for different hardware or a different chaotic system will hopefully be apparent.

III. DATA ACQUISITION SYSTEM

The hardware included a 500-MHz desktop PC, a National Instruments PCI-MIO-16E-4 (E-4) multifunction data acquisition board, a shielded cable, and a connector block.[4] The block connections to the E-4 were jumpered out to a breadboard where the circuit was built.

The E-4 has two 12-bit digital to analog converters (DAC0 and DAC1) that can operate in unipolar ($0\rightarrow+V_{fs}$) or bipolar ($-V_{fs}\rightarrow+V_{fs}$) mode. For further flexibility the full scale voltage V_{fs} can come from an internal 10-V reference or any 0- to 11-V signal applied to the board's external reference connection. There is also a 12-bit successive approximation analog to digital converter (ADC) that can operate in unipolar or bipolar mode. The ADC input circuitry includes two multiplexers allowing measurements on 16 single-ended or 8 differential inputs and a programmable gain instrument amplifier (PGIA) providing full scale ranges from 50 mV to 10 V.

The DACs have a maximum conversion rate of 1 MHz. The ADC's maximum rate is 500 kHz but the PGIA settling time can reduce the rate for full accuracy conversions to about 125 kHz particularly when switching from low to high gains. The ADC and DAC conversions can be triggered by pulses applied to selected board inputs or they can be derived from the board's 20-MHz master clock by dividing it down to the desired rate using the E-4's timer/counters.

All data acquisition and analysis programs were written with the LABVIEW software package,[4] and several figures in this paper are from those programs.

A. Drive generation

DAC0 operated in bipolar mode to generate a continuous sinusoidal drive signal. The process begins by constructing a 200-point integer array approximating one cycle of a sinusoid. The array is converted sequentially and repeatedly at a uniform rate determined by the DAC "update clock." Because the array is small enough to fit in the E-4's DAC buffer, once the conversions are started, they run solely within the E-4.

The drive current needed would be near the DAC limits of ± 5 mA and so the DAC output was buffered as illustrated in the circuit on the right in Fig. 1. The circuit consists of a unity gain op-amp with a low-pass filter on the input stage to smooth out the digitizing steps in the raw DAC output. The 3-dB frequency $1/(2\pi RC)$ was chosen around 3 kHz for minimal attenuation at the 1.6-kHz drive frequency while the digitizing steps at 320 kHz are attenuated nearly 99%.

The drive amplitude v_0 could be adjusted several ways. The method chosen gave the most accurate sine wave representation by keeping the amplitude of the sinusoidal array fixed at 2047—the maximum for a 12-bit signed integer. With DAC0 operating in external reference mode, the actual amplitude of the output was then determined by the voltage applied to the external V_{fs} input. This input was jumpered from the output of DAC1 (operating in internal $V_{\mathrm{fs}}=10$ V reference mode) so that the drive amplitude could be controlled in software.

B. ADC waveforms

The LRC circuit's capacitor and resistor are connected across two of the eight differential inputs with the positive terminal on the upstream side of the current flow. The measured voltages v_c and v_r are scaled to determine the charge $q=Cv_c$ and the current $i=v_r/R$.

Several steps are involved in making the measurements. A channel list is created giving the multiplexer inputs (channels) to be digitized and the order in which they should be digitized. A second list gives the PGIA gain settings that should be used. Once acquisition is started, the conversions run continuously with each pulse from the "scan clock" initiating a scan—a reading of all the channels in the list. The interchannel delay is controlled by a separate "channel clock" and was set to 5 μs for this work.

The phase of the drive voltage θ is the third dynamical variable, and its value—to within a constant offset—was made implicit in the array index of the ADC-measured variables as described next. The ADC scan clock and the DAC update clock are both divided down from the single 20-MHz master clock. A precise correlation is maintained between the ADC readings and the phase of the drive by programming the integer divisors for both clocks so that the same number of master clock ticks pass during one cycle of the DAC0 waveform generation as pass for a whole number of ADC scans.

For example, a 200-point waveform having a drive frequency of 1.6 kHz requires that the DAC conversions run at 320 kHz. With a 20-MHz clock, the nearest divisor would be 62 or 63. Choosing 62, each drive waveform is complete in $62\times 200=12\,400$ ticks of the 20-MHz clock. Ten ADC readings per cycle were desired and so a divisor of $12\,400/10=1240$ was used for the scan clock. With these values, exactly ten scans are read on each cycle of the drive. As the data show, there is no loss of correlation even after thousands of cycles.

A second method for obtaining the phase space variables q and i was also successfully applied. When this method was used, only the capacitor voltage v_c was digitized and the ADC used the same divisor as the DAC. Although the ADC conversions then run at 320 kHz, somewhat close to the maximum 500-kHz rate, the ADC accuracy remains high because only a single, smoothly varying voltage is being digitized and there is no multiplexer switching nor changes in the PGIA. With 200 readings per drive period, values for q and i were then determined using Savitsky–Golay filtering.[5] These filters are equivalent to a least squares fit to a polynomial at each desired point along the waveform based on an equal amount of data to each side. Thirty-three point, quartic filters were used, evaluating q and i at ten points per drive cycle. (Such a filter was also used to evaluate di/dt for use in one of the fitting procedures described later.) These filter parameters were found to work well for prior work on a driven chaotic pendulum[6] where data consisted of angular readings that were also taken at a rate of 200 per cycle.

The voltage v_c was measured on the ± 5 V range and v_r was measured on the ± 0.25 V full scale range. The voltage change corresponding to the least significant bit (lsb) of a bipolar 12-bit ADC is 1/2048 of the full scale range and the standard deviation of a $\pm 1/2$ flat distribution is $1/\sqrt{12}$. Consequently, a 1/2 lsb error in the digitizations translates to standard deviations in the charge and current given by $\sigma_q=0.07$ nC and $\sigma_i=0.32$ μA. The expected standard deviation of q, i, and di/dt values obtained from the Savitsky-Golay filters are 23 pC, 1.0 μA and 0.11 C/s^2, respectively, assuming the same 1/2 lsb digitizing error in v_c.

As they come in, the raw 12-bit ADC readings are stored in a large memory buffer via direct memory access. The buffered data are then saved to disk as 16-bit integers at regular intervals. A typical trajectory of 50 000 drive cycles takes about 30 s to collect and at 20–200 ADC readings per cycle results in file sizes from 2 to 20 Mbytes.

IV. ANALYSIS AND RESULTS

Analysis begins with the ADC-measured chaotic waveforms scaled or filtered to obtain a time series of phase points q_i, i_i at ten points per drive cycle for 50 000 cycles. This representation is illustrated by the front-facing two-dimensional data array in Fig. 3. The block from q_0, i_0 to q_9, i_9 represents points from the first cycle of the drive waveform. A similar block from q_{10}, i_{10} to q_{19}, i_{19} just below it represents points from the second cycle, and so on.

Since there are ten points per cycle, the indices $0, 10, 20, \ldots$ all correspond to values at the same point on the cycle, while $1, 11, 21, \ldots$ all correspond to a point one-tenth of a cycle further along. The tenth group, with the indices $9, 19, 29, \ldots$ and corresponding to a point nine-tenths of the way along the waveform, completes the data set. Figure 3 shows how the data blocks from each cycle can be

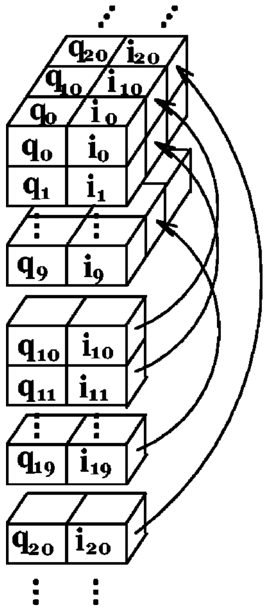

Fig. 3. Data redimensioning to produce Poincaré sections. The original data are in the front-facing vertical plane. The 10 Poincaré sections are the horizontal planes in the top block.

repositioned behind the block from the previous cycle thereby building up a three-dimensional array in which each horizontal layer contains phase points from only a single phase of the drive cycle. The data in these horizontal "slices" are Poincaré sections—all points q_i, i_i at a single phase θ of the drive. LABVIEW's "redimension array" operation converts between the time series and Poincaré representations while the "index array" operation slices out any of the ten available sections.

The two Poincaré sections of Fig. 4 were both obtained from the same circuit (including a 110-Ω discrete resistor) and both include data from 50 000 drive cycles. For (a), q and i were scaled (but not smoothed) from data sets in which v_c and v_r were digitized ten times per drive cycle. For (b), q and i were determined using Savitsky–Golay filters from data sets in which only v_c was digitized 200 times per cycle. For Fig. 4(a), and for the analyses to follow for that data set, the digitizations of v_c and v_r are assumed to be simultaneous. That is, the 5-μs interchannel delay (1/125th of the drive period) is neglected.

The data for Fig. 5 were obtained as for Fig. 4(b), but without the discrete resistor. The circuit resistance determines the damping parameter Γ, and the higher damping for the circuit with the 110-Ω resistor leads to a faster rate of contraction of occupied phase space volumes and produces more sharply peaked ridges in phase space density as evidenced in the Poincaré sections.

The analysis procedures to determine the system parameters, Lyapunov exponents, and fractal (capacity) dimensions have been described previously.[6] The results are displayed in Table I. The first two lines correspond to the data sets used for Figs. 4(b) and Fig. 5, respectively, while the third line corresponds to the data set used for Fig. 4(a).

The system parameters were determined from a least squares fit to Eq. (3) using Savitsky–Golay evaluated values of q, i and di/dt at 10 000 points on each of the ten Poincaré sections. All but one of the fitted parameters are within 15%

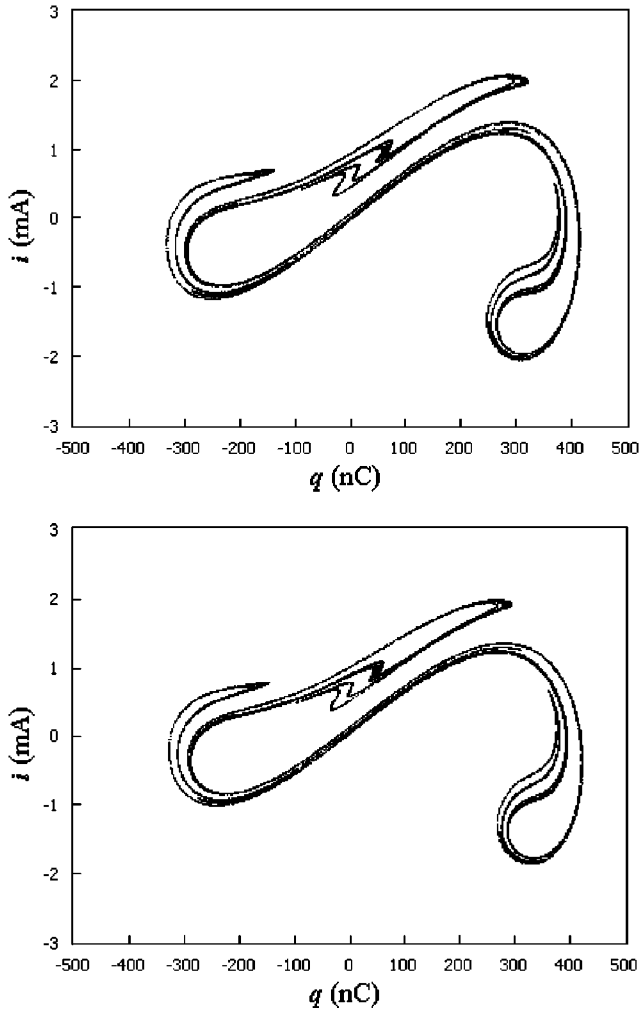

Fig. 4. Comparison of Poincaré sections for two methods of data acquisition. (a) Scaled from a data set with 10 digitizations of v_c and v_r per drive cycle. (b) From Savitsky–Golay filters based on a data set with 200 digitizations of v_c per drive cycle.

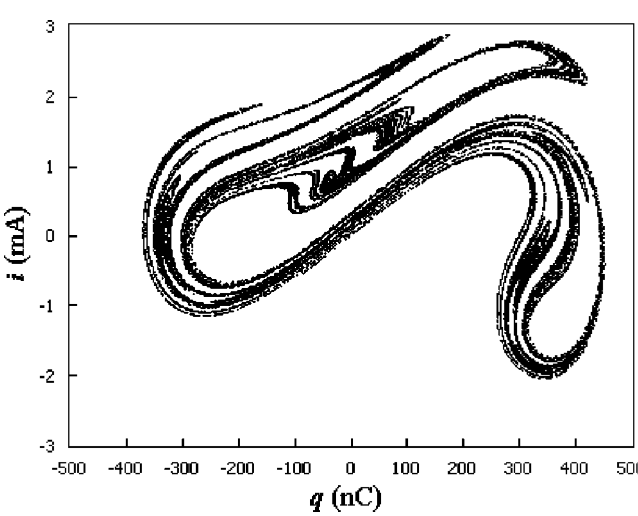

Fig. 5. Poincaré section obtained as for Fig. 4(b) but with the 110-Ω discrete resistor removed.

Table I. Fitted system parameters, capacity dimension d_0, Lyapunov exponents λ_i, and Lyapunov dimension d_L for two resistances.

R (Ω)	α (ms^{-2})	β ($ms^{-2}\ \mu C^{-2}$)	Γ (ms^{-1})	ϵ (mA/ms)	d_0	λ_1 (ms^{-1})	λ_2 (ms^{-1})	d_L
70	47	590	0.80	7.3	1.64	1.18	−2.02	1.58
180	48	590	1.70	7.4	1.46	0.92	−2.99	1.31
180					1.44	1.04	−2.78	1.37

of the values obtained from Eqs. (5) to (8) using R, L, C, a, b as given previously and $v_0 = 1.0$ V—the drive amplitude used for all three data sets. The rms deviations of the fits were 0.23 and 0.18 C/s^2 for $R=70$ and $R=180\ \Omega$ data sets, respectively, which compare well with the best case 0.11 C/s^2 uncertainty in di/dt based on a 1/2-lsb uncertainty in the ADC digitizations.

The capacity dimension d_0 was determined using the box counting algorithm[7] from a single Poincaré section of 50 000 cycles. The q,i plane is divided into a rectangular grid and the number of grid boxes N containing at least one phase point is determined as the linear size s of the rectangles is reduced. The capacity dimension is the slope of the $\log N$ vs $\log 1/s$ graph. The data and fit are shown in Fig. 6 for the two resistance values and demonstrates a near linear behavior as the grid was varied from 200 to 320 000 covering rectangles. With only 50 000 phase points, some of the smallest rectangles are unoccupied only because the trajectory is finite, which may account for the slight flattening out of the data for the finer grid settings. Consequently, the values in Table I are computed from only the eight points for the coarser grids. (The values decrease 0.03–0.05 when all twelve points are used.)

The Lyapunov exponents were determined using a modification of the Eckmann and Ruelle algorithm[8,9] from ten equally spaced Poincaré sections of 50 000 cycles. The algorithm followed a single fiduciary trajectory for at least 1000 cycles, examining the evolution of phase points in the neighborhood of that trajectory as they propagate from one Poincaré section to the next. Neighboring points (typically several hundred) were those found in an elliptical patch centered on the fiduciary and having major axes of 50 nC in q and 100 μA in i. The neighboring points' displacements from the fiduciary in q and i after evolving are fit to a quadratic formula in the starting displacements of q and i. The Lyapunov exponents are derived from the linear terms.

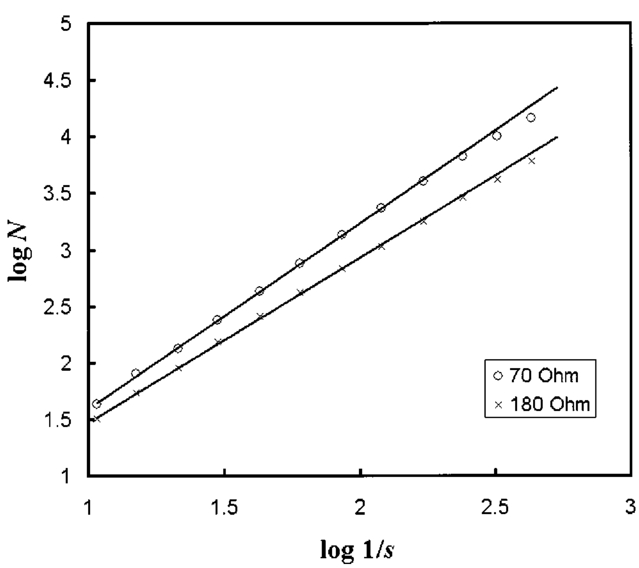

Fig. 6. A log–log plot of the number of grid boxes needed to cover a Poincaré section vs the inverse size of the grid boxes. The slope is the capacity dimension given in Table I.

The rms deviations for the Lyapunov fits give some indication of the accuracy of the phase points. When analyzing the data set of Fig. 4(a) where direct measurements of v_c and v_r were used, the rms deviations averaged around 0.12 nC for the fits to the displacements in q and around 0.9 μA for the displacements in i. These deviations compare reasonably well with the 1/2-lsb uncertainties in each point's coordinates of 0.07 nC and 0.32 μA. The rms fitting deviations were about 0.08 nC and 1.6 μA when analyzing the data sets of Figs. 4(b) and 5 where Savitsky–Golay filters were used. Here again, the deviations appear reasonable compared to and 1/2-lsb uncertainties of 0.023 nC and 1.0 μA.

Variations in the Lyapunov exponents over different 1000 cycle sections of the complete 50 000 cycle trajectories were typically around 5%, which can be taken as a rough estimate of their uncertainty.

Two theoretical checks on the Lyapunov exponents can be made. First, the Lyapunov dimension is defined by

$$d_L = 1 + \frac{\lambda_1}{|\lambda_2|} \tag{10}$$

and should be equal to the capacity dimension according to the Kaplan–Yorke conjecture.[10] The results are demonstrated in Table I. As a second check, the sum of the Lyapunov exponents is predicted to be equal to $-\Gamma$. For the 70-Ω data set, the sum is -0.84/ms, in good agreement with the Γ of 0.80/ms. For the two 180-Ω data sets, the Lyapunov sums are -2.07/ms and -1.74/ms, while the fitted Γ is 1.70/ms.

V. CONCLUSIONS

We have shown how chaotic attractors governing driven nonlinear systems can be obtained experimentally using a multifunction data acquisition system to perform synchronous waveform generation and waveform acquisition. The critical feature is the use of a common clock to trigger both the digital to analog and the analog to digital conversion processes. The technique was applied to a Duffing oscillator and data sets for ten Poincaré sections were collected.

Results for circuit parameters, fractal dimensions, and Lyapunov exponents showed a reasonable degree of self consistency. In addition, the rms deviations for the least-squares fits to determine circuit parameters and Lyapunov exponents agreed well with expectations based on the precision of the raw measurements.

The equipment needed to apply the technique is now fairly common and relatively inexpensive and with it the field of experimental nonlinear dynamics should become more accessible to undergraduate students. Many other studies could be performed with the hardware. The use of additional ADC channels would make possible the study of higher dimensionality systems. The second DAC might be used to vary a system control variable for studies in the control of chaos or for studies in the route to chaos. Or, the second DAC might be used to generate a second periodic waveform for studies in dual drive systems.

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