Generation of Second and Fourth Harmonic Signals Using a Balanced Colpitts Oscillator With a Patch Antenna

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***Abstract*—A Colpitts oscillator that generates signal at 589 GHz using both phase superposition and nonlinearities of components is demonstrated in a 0.12 μm SiGe BiCMOS process. This approach increases the ratio between fourth and second order harmonic power levels by more than 2 dB compared to that obtained using only linear phase superposition. The output power of this circuit with the highest operating frequency for transistor based signal generators is -37.7 dBm.**

***Index Terms*—Colpitts oscillator, on-chip patch antenna, SiGe.**

I. Introduction

THE uses of terahertz portion of spectrum (300 GHz–3 THz) for radars, remote sensing, advanced imaging, and bio-agent and chemical detection [1], [2] have been extensively studied. The terahertz frequencies provide several advantages for sensing and communication systems such as high spatial resolution and a wide bandwidth for increased communication rate. A key component of these systems is a low-cost and reliable signal source. Use of silicon technology can reduce costs of terahertz systems and has the potential to open up this part of spectrum to moderate and high volume applications. This letter reports a 0.12 μm SiGe BiCMOS Colpitts oscillator, extracting the fourth harmonic signals of 589.35 GHz using a combined method of phase superposition and nonlinearity of the transistors [3]–[7], achieving the highest frequency obtained from a monolithic integrated circuit known to date.

II. Design

The circuit schematic of Colpitts oscillator is shown in Fig. 1. The schematic is the same as that for a push-push oscillator

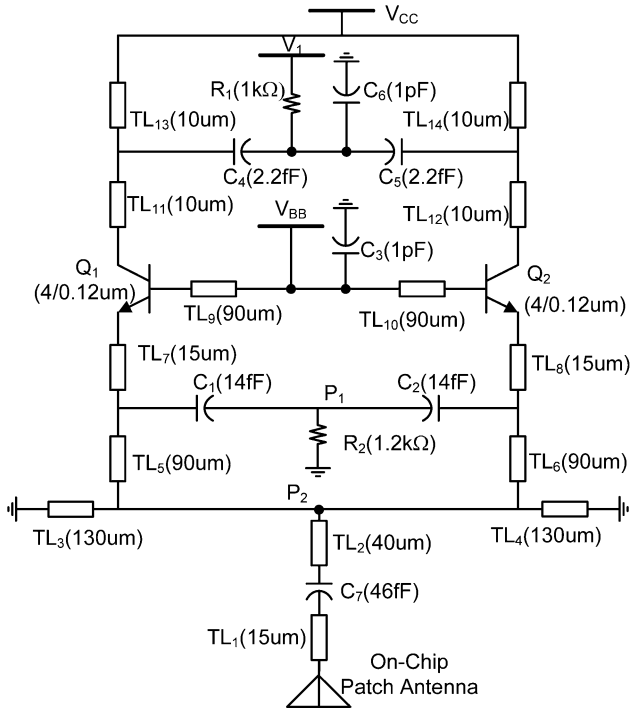

Fig. 1. Schematic of a THz antenna-loaded oscillator at quadruple order.

that uses linear phase superposition of two phases with 180° difference [5], [6] to increase the output frequency of circuits beyond the unity available power gain frequency (f_{max}). The fundamental resonators operate at one half of the normal desired output frequency, which increases the quality factors of both inductor and varactor. This lowers phase noise and increases power higher efficiency. The common collector series resonator topology efficiently generates negative resistance at millimeter-wave frequencies [8]. Transmission line, TL_9, C_1, base-emitter junction capacitance of transistor Q_1, transmission line TL_{10}, C_2 and base-emitter junction capacitance of transistor Q_2 determine the resonant frequency of fundamental oscillation. At the center point P_1, the fundamental odd mode components is canceled, which makes the point (P_2) virtual ground. The second and fourth harmonics can be extracted from P_2. The resistor R_2 is larger than the even mode negative resistance due to the transistors, and suppresses the even mode oscillation. When the collector currents are increased by increasing the base-emitter voltage, the transistors Q_1 and Q_2 can enter into the saturation region during parts of an oscillation cycle. The

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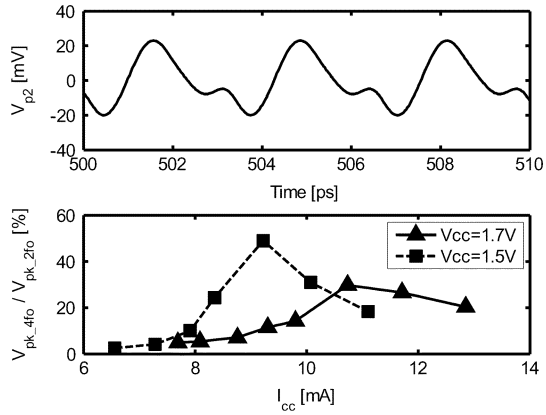

Fig. 2. Simulated waveform (Top) at P_2 when $V_{CC} = 1.5$ V and $I_{CC} = 10.0$ mA, and the ratio between the fourth and second harmonic (bottom) of the voltage at P_2.

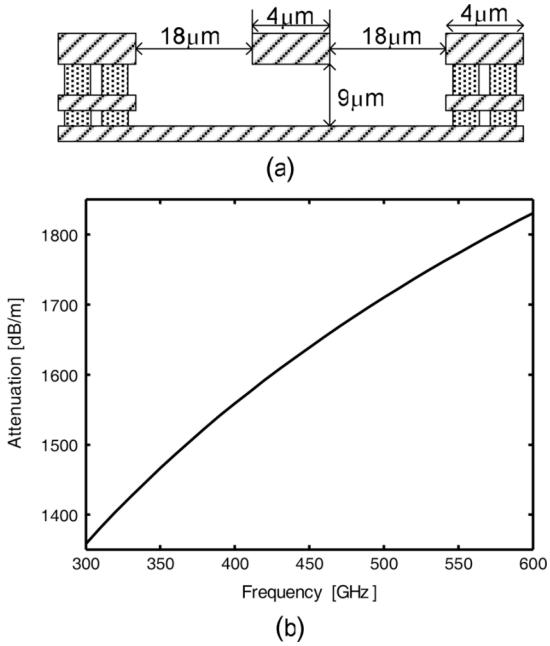

Fig. 3. Cross section (a) and attenuation of transmission line (b).

non-linearity associated with this generates the fourth order harmonic at the common mode nodes. Fig. 2 shows the simulated waveform (top) at P_2 when $V_{CC} = 1.5$ V and $I_{CC} = 10.0$ mA.

Fig. 2 also shows the simulated ratios between the voltages for the second and fourth order harmonics (bottom). The power level of fourth order harmonic can be as high as ~6 dB below that for the second order push-push output. This is ~2 dB higher than that can be generated using the ideal line are phase superposition [3], [4].

III. Fabrication and Measurements

The circuits were implemented using a 0.12 μm SiGe HBT foundry process. This process supports a high performance n-p-n HBT with f_T of 200 GHz, f_{max} of 240–290 GHz. The emitter length and width of transistors Q_1 and Q_2 are 4 and 0.12 μm. The transmission line structure for matching is shown in Fig. 3. The ground plane is formed with multiple metal layers with total thickness of ~0.4 μm. The thick top metal layer is used as the signal line to minimize losses. The thickness of dielectric layer between the signal line and ground plane is about 9 μm. The width of the signal line is 4 μm and the characteristic impedance is 66 Ω. The HFSS simulated attenuation constants of the transmission lines are about 1400 dB/m at 300 GHz and 1800 dB/m at 600 GHz. The on-chip patch antenna consists of a patch space and a ground plane. The ground plane shields the antenna from the lossy silicon substrate and makes the antenna

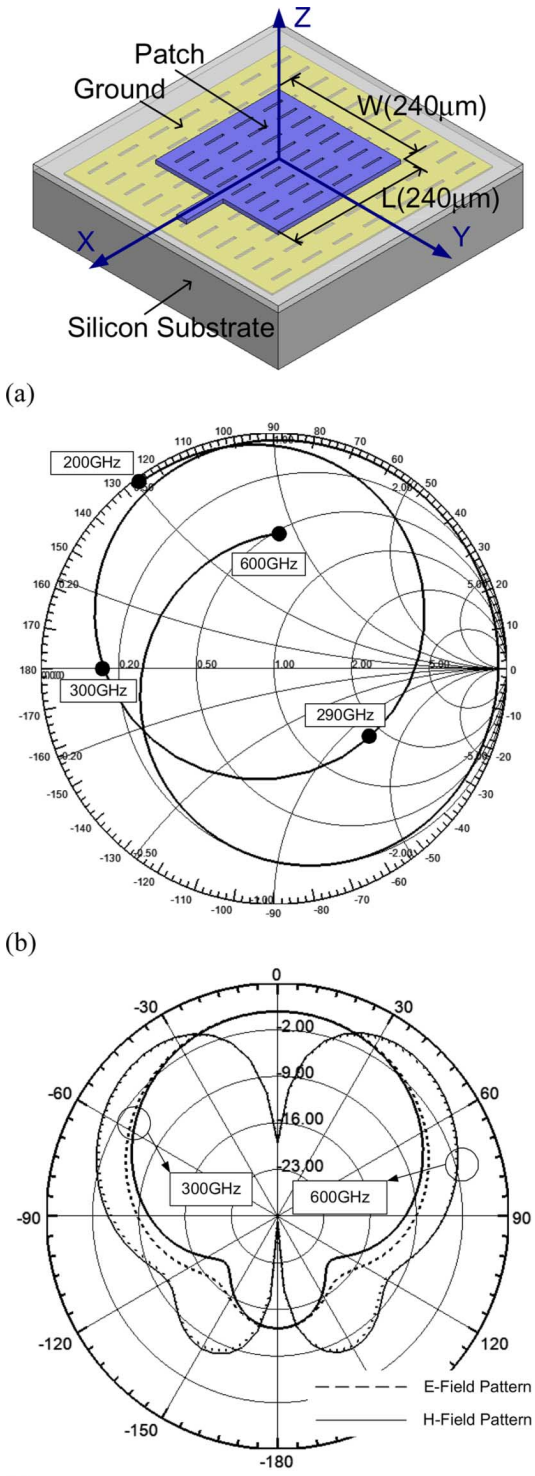

Fig. 4. Patch antenna (a), antenna input impedance (b), antenna gain at 300 and 600 GHz (c).

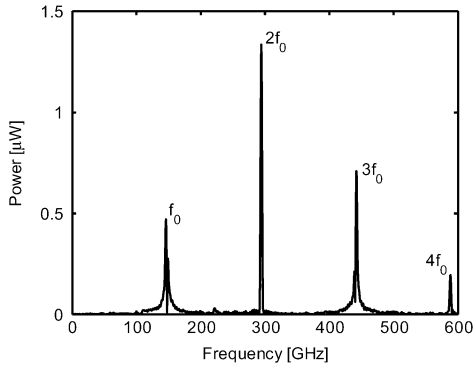

Fig. 5. Output spectrum measured using an FTIR when $\mathrm{V_{CC}} = 1.7$ V and $\mathrm{I_{CC}} = 8$ mA.

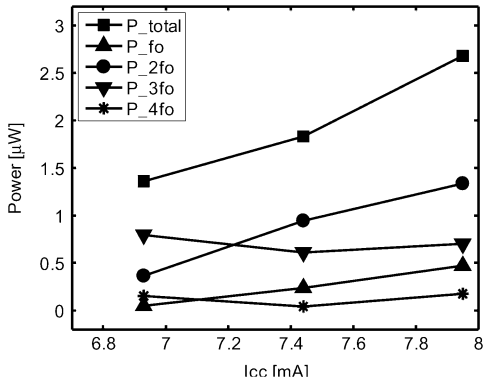

Fig. 6. Measured output power versus bias current.

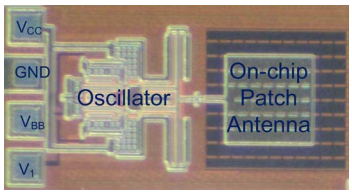

Fig. 7. Die photograph.

characteristics less dependent on nearby metal structures. The patch length is about half wavelength at 294 GHz. The patch size is $240 \times 240\ \mu\mathrm{m}^2$ (Fig. 4(a)). The thick top metal layer is used to form the patch. The total metal thickness for the ground plane is about 1.2 μm. The separation between the patch and ground plane is about 4 μm. Slots are added to satisfy the design rules, and metal layers shunted with vias are used to minimize loss caused by the slots. Overlapping of slots on adjacent metal layers is avoided to increase shielding. The simulated peak gain of patch antenna is about 0.8 dB and efficiency is 20% around 300 GHz. Near 600 GHz, the antenna performance is also reasonable because 240 μm is approximately a wavelength. The peak gain is 1.7 dB and efficiency is 42%. The input impedances at 300 and 600 GHz are 8 and 26 Ω. The Patch antenna is simulated using the Ansoft High Frequency Structure Simulator (HFSS). The simulated radiation patterns at 300 and 600 GHz are shown in Fig. 4(c). A Bruker 113 V Fourier transform infrared spectroscopy (FTIR) system has been used for the characterization of oscillators [5]. A silicon bolometer and 5 mil Mylar beam splitters are used to increase the sensitivity of the interferometer. For the absolute power measurement, the circuit is placed directly at the input of the bolometer. The optical responsivity of the silicon bolometer (HD-3) from Infrared Laboratories is 1.1×10^4 V/W. Fig. 5 shows the measured spectrum. The circuit was measured at $\mathrm{V_{CC}} = 1.7$ V and $\mathrm{I_{CC}} = 8$ mA or power consumption of 13.6 mW. The corresponding power levels for the second order (294.72 GHz) and fourth order (589.35 GHz) harmonics are -28.8 dBm and -37.7 dBm.

The measured power efficiency is 0.01 and 0.0013% for the second and fourth harmonics. Despite the fact that the antenna gain perpendicular to the patch is low at 600 GHz, because of the measurement configuration, the power transmitted off-axis is detected by the bolometer.

The spectrum also includes power at the third order harmonic frequency (441.99 GHz). Presently, its origin is not well understood. However, its output power level is -31.5 dBm. Fig. 6 shows the measured output power versus the supply current, $\mathrm{I_{CC}}$. When the bias current changes from 7 to 8 mA, the second order harmonic power changes from -34.4 to -28.8 dBm. The power of fourth harmonic at 589.35 GHz varies from -40.4 to -37.7 dBm. The third harmonic output power is relatively constant around -33 to -31 dBm over the same current range. At low current levels, the third order harmonic power is higher than that of the second order. Fig. 7 shows a die photograph of the circuit. The area of the circuit is $500 \times 940\ \mu\mathrm{m}^2$. The matching at $\mathrm{P_2}$ and the antenna can be better optimized to improve the output power at 589 GHz and to attenuate the other harmonics.

IV. Conclusion

A Colpitts oscillator fabricated in a 0.12 μm SiGe BiCMOS technology generates signals at 589.35 GHz using a combination of phase superposition and nonlinearities of circuit elements (saturation of transistors). This can increase the ratio between fourth and second order harmonic power levels by more than 2 dB compared to that obtained using linear phase superposition. The output power level is -37.7 dBm and 589.35 GHz is the highest frequency for signals generated by transistor circuits in any process technologies.

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