553-GHz Signal Generation in CMOS Using a Quadruple-Push Oscillator*

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Abstract

A 553-GHz quadruple-push oscillator is demonstrated using low leakage transistors in 45-nm CMOS. The currents of coupling transistors of a quadrature oscillator were summed up to implement quadruple pushing. Quasi-optical measurements showed that the circuit generates 4th harmonic signal at 553 GHz with the power level of 220 nW, while suppressing unwanted harmonic signals. The circuit consumes 64 mW from a 1.4 V supply.

Keywords: CMOS, sub-millimeter wave, quadruple-push, quadrature, oscillator, and on-chip antenna.

Introduction

The sub-millimeter wave portion of electromagnetic spectrum (0.3-3 THz) has a wide range of potential applications in imaging, sensing, and communication [1]. The recent advances of high frequency performance for CMOS (Complementary Metal Oxide Semiconductor) have made it possible to consider CMOS as a new means to overcome the limitations of cost and integration level of conventional sub-millimeter wave systems. N-push techniques have been employed to generate signals above the unity maximum available gain frequency (f_{max}) of devices [2]-[5]. Recently, a 1.3-THz signal has been generated in CMOS using the 6th harmonic of a 4-push oscillator [5]. The signal is one of the unexpected harmonics. None of the power levels of the circuit were available. In addition, the fourth order output power level was lower than those of the first three harmonics.

This paper reports a quadruple-push oscillator fabricated using low leakage transistors of a 45-nm CMOS technology with improved 4th harmonic current generation and suppression of unwanted harmonics. It radiates 220nW of power at 553 GHz . The output power is ~4× that radiated at 410 GHz in [3] which has been the highest radiated from a CMOS circuit at frequencies above 400 GHz.

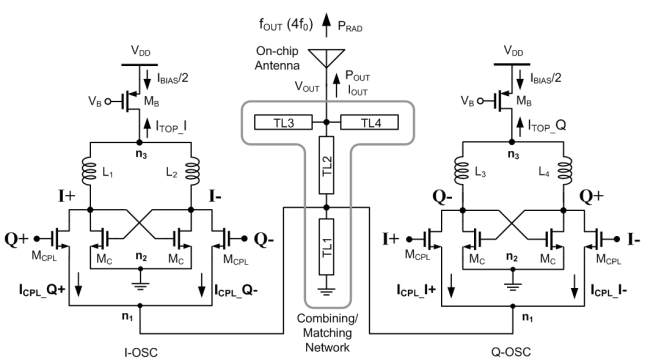

Fig. 1 Schematic of quadruple-push oscillator schematic with an on-chip patch antenna.

*This work is supported by SRC and TxACE (Task ID: 1836.036).

Circuit Design

Fig. 1 shows the schematic of proposed quadruple-push (4-push) oscillator with an on-chip antenna. The oscillator is based on a quadrature oscillator with cross-coupled core transistors (M_C) and coupling transistors (M_{CPL}). The harmonic currents I_{CPL} in M_{CPL} are added by a transmission line based passive combining network. Instead of using a separate linear phase combiner [4], this circuit utilizes the quadrature coupling transistors in the oscillator core as the combiner. This reduces the capacitive loading of the *LC* tanks by the gates of phase combiner circuit, which in turn allows the size of transistors in the quadrature oscillator core to be increased for higher output power. Furthermore combining the currents of coupling transistors (I_{CPL}'s) at the sources (n_1 node) instead of common mode currents at the top (I_{TOP}'s) as in [5], increases the 4th order voltage level by ~2× and suppresses unwanted harmonics. This is due to the fact that the currents of core transistors and coupling transistors are not in phase and destructively interfere.

All transmission lines are implemented using grounded coplanar waveguide (GCPW) [3] with characteristic impedance of ~45 Ω. Single-turn circular symmetric inductors using Metal 7 layer were employed for the *LC* tanks. The sources of M_{CPL} (n_1 node) are terminated with a transmission line matching network to maximize the power generation at the 4th harmonic frequency. The node n_2 is potentially another node at which 4th order harmonic could be generated. The core transistor width (W_C) is larger than the coupling transistor width (W_{CPL}). For this reason, the node n_2 has larger source to body capacitance. Simulations showed that the 4-push harmonic combining at this node results 30% lower output swing than that generated at the node n_1.

Fig. 2(a) shows simulated individual current through M_{CPL}, and their total. They contain higher order harmonics due to the nonlinearities in the oscillator. In the quadruple-push oscillator,

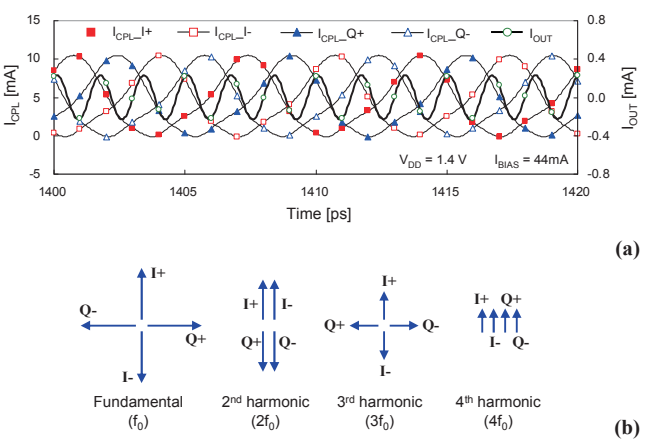

Fig. 2 (a) Simulated current waveforms in the oscillator. (b) Quadruple-push operation.

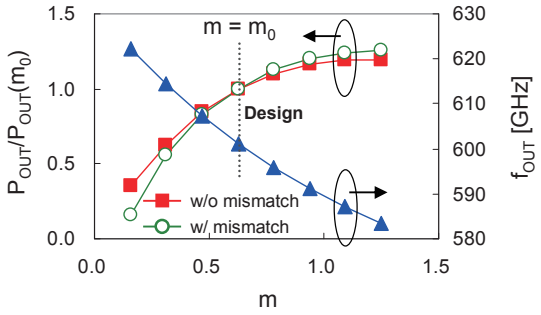

Fig. 3 Simulated normalized output power ($P_{OUT}/P_{OUT}(m_0)$) and frequency (f_{OUT}) versus m ($m = W_{CPL}/W_C$).

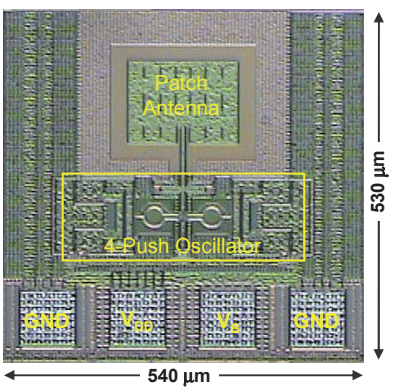

Fig. 4 Quadruple-push oscillator die photograph.

in addition to the linear phase combining, the 4n-th (n = 1, 2, 3, …) order harmonics are constructively combined as illustrated in Fig. 2(b).

Increasing the coupling transistor width raises output power and lowers output frequency because of increased *LC* tank capacitance. Fig. 3 shows the tradeoff between P_{OUT} (power delivered to the on-chip antenna) and f_{OUT} as function of W_{CPL} to W_C ratio, m. The output power (P_{OUT}) saturates as m approaches one. m is set to ~0.6. Various mismatches introduce phase errors in a quadrature oscillator. The phase errors reduce 4-push output power. The effect of mismatch in the tank resonant frequency of the I- and Q-oscillators on P_{OUT} is simulated. The output power degrades less than 2% for m higher than 0.5 and the resonant frequency mismatch of 2%.

The on-chip antenna was implemented using a microstrip patch antenna [3]. The simulated directivity and efficiency of the antenna is 3.4 and 28%, respectively. An inset-feed structure is used for input impedance matching. The patch size is 160×120 µm^2. Fig. 4 shows a die photograph of the fabricated oscillator. The layout was optimized for symmetry to minimize mismatches. The overall chip size is 540×530 µm^2 including bond pads.

Measurement Results

It is challenging to detect sub-microwatt signals above 500 GHz using electronic instrumentation due to excessive loss [4]. In this work, a quasi-optical measurement was employed using the on-chip antenna and a Fourier transform infrared (FTIR) spectrometer (Bruker 113) [3]. A 23-µm thick Mylar beam splitter was used in the FTIR. Fig. 5 plots the measured output spectrum and radiated power (P_{RAD}). The oscillator generated an output signal at 553 GHz with the power level of 220 nW.

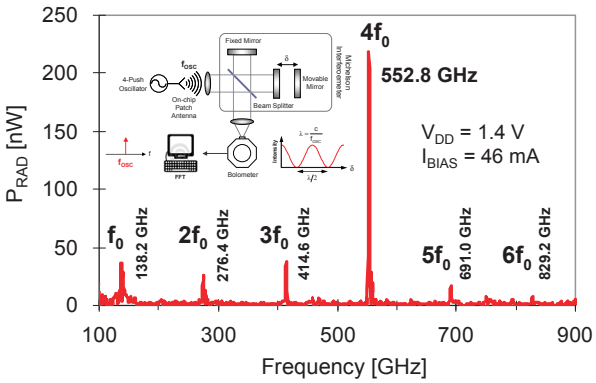

Fig. 5 Measured spectrum of the radiated power. The FTIR setup is illustrated in the inset.

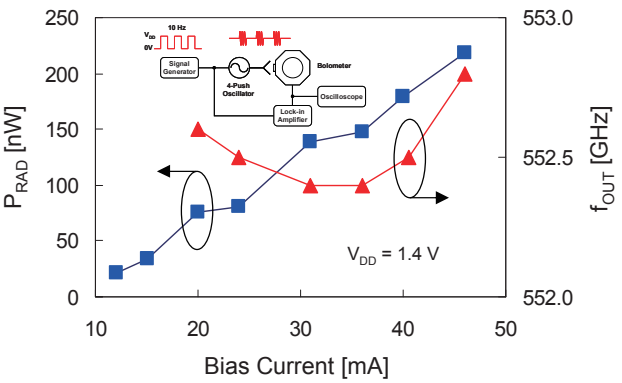

Fig. 6 Measured radiated power (P_{RAD}) and output frequency (f_{OUT}) versus bias current. The measurement setup is illustrated in the inset.

Harmonics up to 6th order (829.2 GHz) were observed. The power levels of all unwanted harmonics are suppressed below 50 nW. The oscillator draws 46 mA of current from a 1.4-V supply. The output power is measured using an IR Labs HD-3 bolometer with responsivity of 4.0×10^4 V/W. The oscillator was powered by 10-Hz square wave from a signal generator to modulate the radiated power. The output signal from the bolometer was observed using a lock-in amplifier (Ithaco 393). Fig. 6 plots the measured radiated power and frequency versus bias current. The circuit starts to oscillate at 12 mA and the radiated power monotonically increases with the bias current. The output frequency varied ~0.5 GHz over the bias range.

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