CHAPTER

THz power generation beyond transistor f_{max}

17

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CHAPTER OUTLINE

The sub-terahertz (sub-THz) region is typically defined as the portion of an electromagnetic spectrum in the frequency range of ~100 GHz to ~1 THz. The electromagnetic fields and wave propagation in this frequency range have remarkable properties, particularly suitable for sensing, imaging, and communication applications [1,2]. Until recently, however, the frequency region has remained as a part of the last unexplored spectrum (the so-called 'THz gap') due to the lack of low-cost, integrated source and detector technology. With advances in photonic and electronic components, this part of the spectrum is progressively becoming more accessible and newer applications for imaging, medical, industry, security, and communication are emerging.

Existing sub-THz spectroscopy systems rely on discrete electronic components coupled together using a bulky waveguide assembly or complex assemblies of optical components (Figure 17.1) [3]. As a result, these systems can be very expensive and non-portable, which makes its application space very limited.

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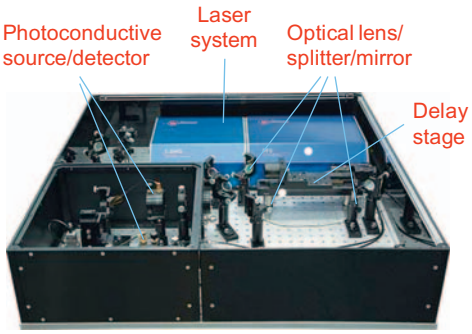

FIGURE 17.1

Conventional optoelectronic spectrometer [3].

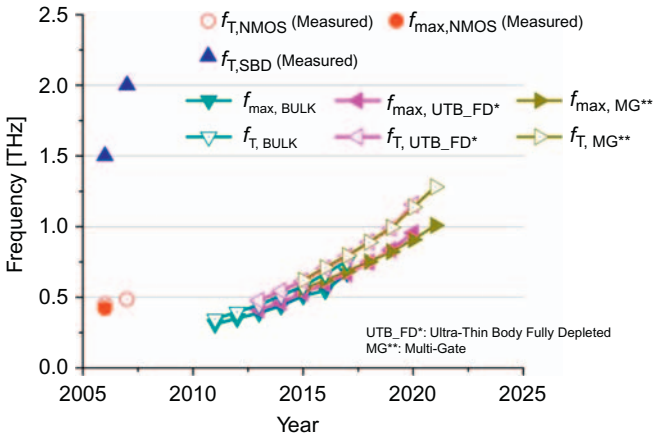

FIGURE 17.2

Projected performance requirements of NMOS transistors from 2011 International Road Map for Semiconductors [5] and the data from the literature.

The use of CMOS technology to implement highly integrated sub-THz systems can radically lower the cost and size by eliminating the costly optical and discrete electronic components opening up a new range of potential applications not accessible due to cost and size limitation.

While traditionally digital CMOS technologies have not been used for sub-THz frequency applications, in recent years, significant improvement in high-frequency performance of CMOS technology have made it possible to consider CMOS as an alternate means for implementing sub-THz wave systems. The scaling of CMOS technology has resulted in transistor cutoff frequency (f_T) and unity maximum available power gain frequency (f_{max}) reaching up to 360 and 450 GHz, respectively [4]. Figure 17.2 shows the projected f_T's and f_{max}'s for NMOS transistors predicted by the 2011 International Roadmap for Semiconductors [5]. By 2016, the projected NMOS unity power gain frequency (f_{max}) is expected to reach

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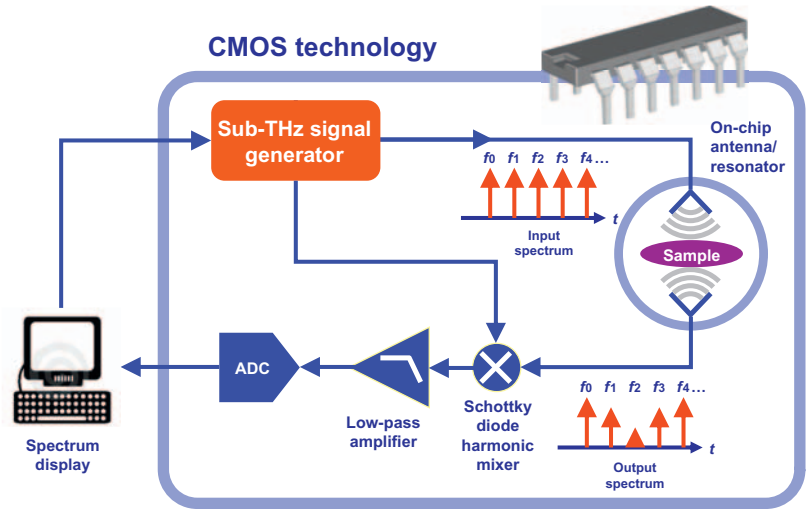

FIGURE 17.3

Conceptual diagram of the sub-THz on-chip spectrometer in CMOS [7].

~600 GHz. Such transistors will provide greater flexibility to implement and improve circuits and systems operating at sub-THz frequencies.

The integration of efficient transmitters, detectors, and on-chip antennas [6] as well as baseband digital signal processing (DSP) circuits in CMOS can enable single-chip realization of compact and affordable THz systems. This can lead to the emergence of moderate-to-high-volume and low-to-moderate-cost sub-THz applications for a wide range of fields. As an example, a single-chip sub-THz spectrometer conceptually illustrated in Figure 17.3 could be implemented using a CMOS technology for critical application in sensing, quality control and security. In order to enable spectral analysis in the sub-THz range, the transmitter consists of a tunable sub-THz-frequency generator and an on-chip antenna (or resonator) while the receiver includes an on-chip antenna, a detector, or a mixer followed by a low-noise amplifier/filter and an A/D converter (ADC).

One of the key components for sub-THz systems is, therefore, the signal generator or oscillatory source on chip. This chapter describes the implementation of sub-THz CMOS oscillators using multiple-push techniques to extract power at frequencies beyond f_{max} [8,9]. Detailed design considerations and measurement results will be discussed for a 410-GHz push-push oscillator and a 553-GHz quadruple-push (four-push) oscillator in CMOS.

17.1 MULTIPLE-PUSH OSCILLATORS

The design approaches in Figure 17.4 illustrate the typical techniques for on-chip signal generation in the mm-Wave and sub-THz frequencies. The first approach

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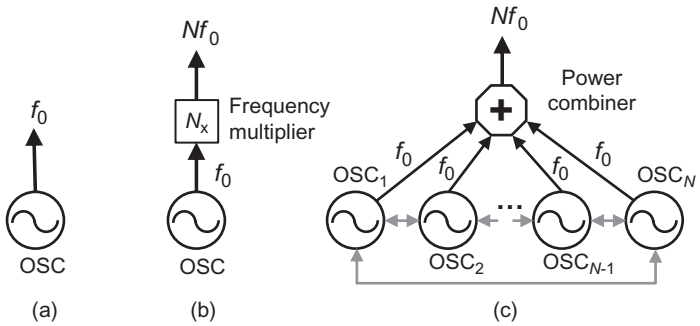

FIGURE 17.4

Design approaches for mm-Wave and sub-THz oscillators: (a) fundamental oscillator, (b) oscillator with a frequency multiplier, and (c) multiple-push (N-push) oscillator.

in Figure 17.4a is that of a fundamental oscillator operating at the desired frequency. While this is straightforward, there are oscillatory conditions which need to be satisfied in order to sustain the autonomous oscillatory mechanism at such frequencies. More specifically, the maximum available power gain (MAG) of the device has to be greater than one at the frequency of the self-sustaining oscillator. Therefore, no single-frequency autonomous oscillation is possible at frequencies beyond f_{max}. In order to extract power above f_{max}, another approach is to use nonlinear devices to frequency multiply the fundamental oscillator output (Figure 17.4b). Therefore, while the oscillator is operating at fraction of the output frequency, signals above f_{max} could be harnessed. However, this approach increases the circuit size and complexity due to additional requirements for harmonic filtering and amplification. A multiple-push (N-push) oscillator in Figure 17.4c consists of N fundamental oscillators each operating at 1/N of the a desired output frequency [10]. The unit oscillators are coupled to each other and oscillate with a relative phase difference of 360°/N with respect to each other for a loop phase of 360°. This allows the N^{th} harmonic of all the oscillators to add in phase at thee output, while the rest cancel out due to the phase relationship among them. Therefore, multiple-push oscillator has a compact size since unwanted harmonics are canceled out without additional filtering networks. This technique also makes it possible to extract signals at frequencies substantially above f_{max} of a device. In addition, it is difficult to achieve a wide tuning range for a fundamental frequency oscillator due to the excessive loss of a tuning element (i.e., low-quality factor of a varactor) which demands larger transistors to sustain the oscillation, thereby increasing (C_{tran}/C_{var}). This implies that a unit oscillator of a multiple-push oscillator can have a wider tuning range. A sub-THz oscillator with wide tuning should be possible using a multiple-push oscillator configuration.

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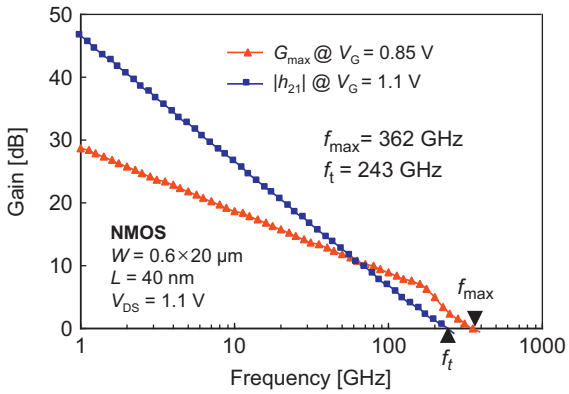

FIGURE 17.5

Simulated frequency response of G_{max} and $|h_{21}|$.

17.2 SUB-TERAHERTZ CMOS PUSH-PUSH OSCILLATOR

17.2.1 DESIGN CONSIDERATIONS

A maximum operation frequency of an oscillator is limited by the unity maximum available power gain frequency (f_{max}) of a transistor [11]. Figure 17.5 shows the simulated frequency response of the maximum available power gain (G_{max}) and unity current gain ($|h_{21}|$) of a 45-nm CMOS transistor model used for the design of oscillators. The peak f_{max} and cutoff frequency (f_t) of the device, under optimal biasing conditions, are estimated to be 362 and 243 GHz, respectively. Therefore, a fundamental frequency oscillator can oscillate upto lower sub-THz frequencies below 200 GHz in order to have enough margin to satisfy loop gain conditions. A multiple-push oscillator overcomes this limitation by boosting the output frequency substantially above f_{max} to cover a significant portion of the sub-THz frequency region.

As an example, a push-push VCO operating up to 192 GHz has been demonstrated in a 130-nm CMOS technology with the fundamental frequency of oscillation being 96 GHz [12,13]. The output frequency of a push-push oscillator can be further increased with CMOS technology with higher f_{max}. A 410-GHz push-push oscillator is implemented in 45 nm CMOS node with 205 GHz as the fundamental frequency of oscillation. Figure 17.6 shows the schematic of the 410-GHz push-push oscillator. The cross-coupled transistor pair generates differential signals at 205 GHz and at the center tap of the inductor, the second harmonic is constructively combined and radiated out, while the differential fundamental signals are canceled out (virtual ground).

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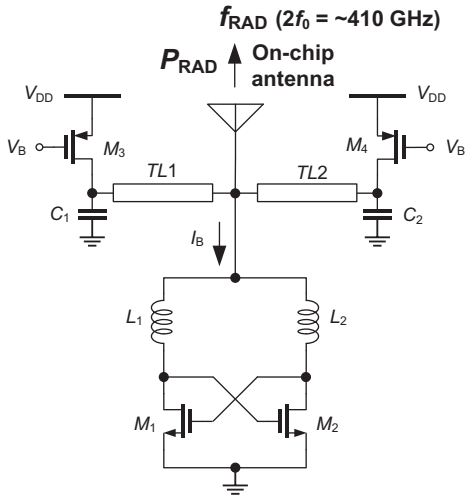

FIGURE 17.6

Schematic of the push-push VCO with an on-chip microstrip patch antenna [8].

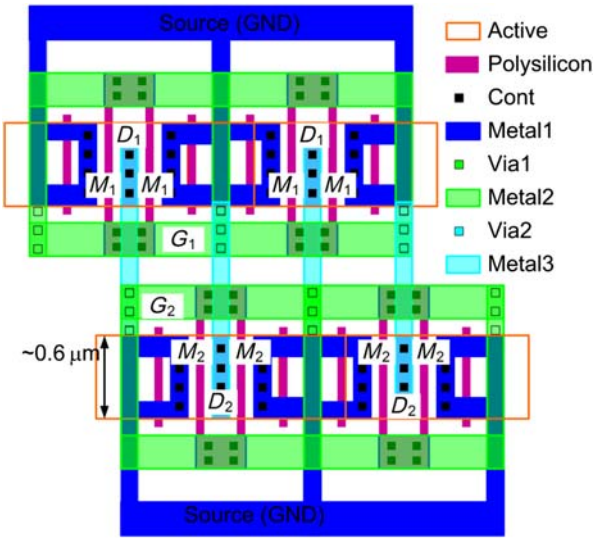

FIGURE 17.7

Layout of cross-coupled transistors [8].

The width of the cross-coupled transistors is about 10 μm. Figure 17.7 shows the layout of cross-coupled transistors. The layout of the core oscillator devices need to be optimized to reduce parasitic resistance and capacitance. The transistor M_1 is shown at the top and M_2 at the bottom in Figure 17.7. Transistor gates are contacted on both ends and folded into multiple fingers.

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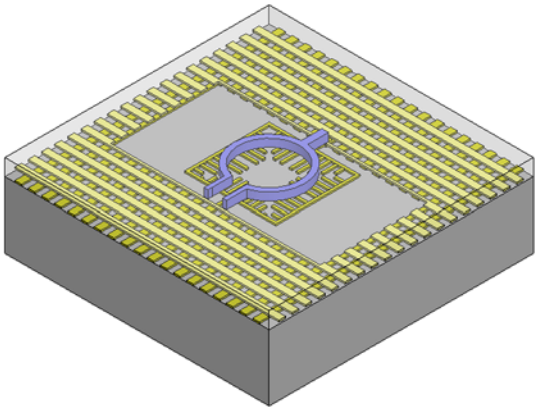

FIGURE 17.8

Structure of circular inductor for the 410-GHz oscillator [8].

The resistance of a contact is about 60 Ω. To decrease the parasitic resistance, multiple contacts on the transistor gates are employed. Each finger has two contacts on each side and connected using Metal 2. The sources are connected together using the Metal 1 layer. The transistors are directly cross-connected from the drain to gate using the Metal 2 and Metal 3 layers. The top metal layer thickness is about 2 μm and has larger fringing capacitance than the lower metal layers. The lower metal layers are used to connect the transistor gates. The width of each finger is about 0.6 μm. Polysilicon dummy gates are employed for each finger to meet design rules.

Figure 17.8 shows the differential circular inductor used in the push-push oscillator. To reduce the parasitic capacitance to substrate, only the top metal layer is used. The top metal layer is a 2 μm thick copper metal layer located a few microns above the silicon substrate. The inductor is designed to have a diameter of 20 μm with a metal width of 1.6 μm. This is to ensure that the metal width is about 10 times the skin depth of copper at 200 GHz which is approximately 0.16 μm. The polysilicon layer is used to form a patterned ground shield (PGS) to minimize substrate losses due to eddy currents. In addition, metal layers 1 and 2 are used to form ground grids. The pitch is kept at 2.5 μm and width of each metal layer is about 1 μm. Accurate simulation and characterization of the inductance and its quality factor are important to properly set the operating frequency of the oscillator and the output power. The effective inductance ($\mathrm{Imag}(Z_{11})/\omega$) and quality factor ($\mathrm{Imag}(Z_{11})/\mathrm{Real}(Z_{11})$) are estimated to be of $\sim$40 pH and $\sim$8, respectively from HFSS simulations. The low-quality factor is primarily due to the skin effect and substrate losses.

The operating frequency of the oscillator is determined by the capacitance of the cross-coupled transistor and the circular inductor. The capacitance can be estimated by the following equation [14]:

$$C_{\mathrm{total}} = C_{\mathrm{gs}} + 4C_{\mathrm{gd}} + C_{\mathrm{db}}$$

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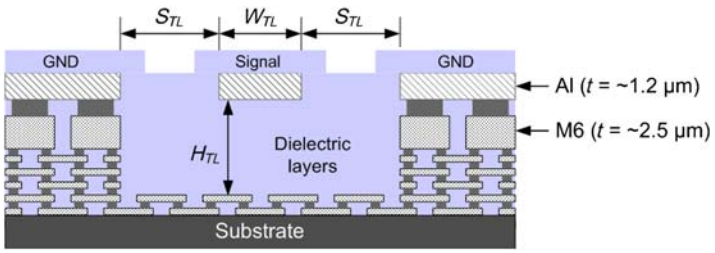

FIGURE 17.9

Cross-section of grounded coplanar waveguide (GCPW).

where C_{gs} is gate-to-source capacitance, C_{gd} is gate-to-drain capacitance, and C_{db} is drain-to-body capacitance of transistors. The extracted capacitances C_{gs}, C_{gd}, and C_{db} from Cadence simulations are 3.8, 2.3, and 3.0 fF, respectively. Therefore, the operating frequency $f_{osc} = 1/(2\pi\sqrt{(LC)})$ of the oscillator can be determined to be 205 GHz with a 40-pH inductor.

The quarter-wavelength transmission lines (t-lines) at the second harmonic frequency, *TL*1 and *TL*2, are employed to provide the bias current without loading the push-push node by the impedance transformation [15]. Two pairs of a t-line and PMOS transistor are used for symmetry to minimize mismatches. The t-line is formed using a grounded coplanar wave guide (GCPW) structure, which confines fields in a relatively small area and shows stable characteristic impedance over a wide frequency range [16]. A GCPW has an additional ground plane at the bottom to isolate the signal line from the lossy silicon substrate and to reduce coupling to other circuits. Figure 17.9 shows the cross section of GCPW. The signal line width (W_{TL}) is 6 μm and the gap (G_{TL}) between the signal line and ground line is 4 μm. The loss of GCPW is estimated to be ~2.5 dB/mm at 400 GHz from EM simulations. The shunt bypass capacitors, C_1 and C_2 in Figure 17.6, are implemented with metal-oxide-metal structures to provide low impedance to the ground at the output frequency [17].

The on-chip antenna is implemented using a microstrip patch antenna as shown in Figure 17.10 [8]. Microstrip patch antennas are popular with antenna engineers since they are relatively inexpensive to manufacture and easy to design because of the simple two-dimensional physical geometry [18]. In CMOS processes, the antenna configuration has an important advantage that the loss caused by the conductive silicon substrate can be avoided due to the ground metal plane between the patch and silicon substrate. In addition, the ground plane reduces the impact of nearby metal structures on the antenna characteristics. The rectangular patch antenna is approximately a half wavelength long section of rectangular microstrip t-line. The microstrip patch antenna belongs to the class of resonant antennas, and its resonant characteristic is responsible for the narrow bandwidth [18]. The small thickness of the dielectric layer which limits the patch and the ground plane spacing can further limit the efficiency of the patch antenna

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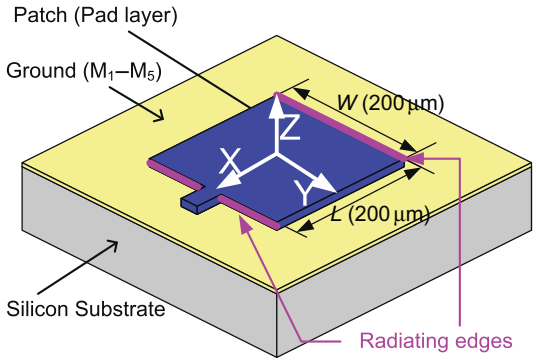

FIGURE 17.10

On-chip microstrip patch antenna [8].

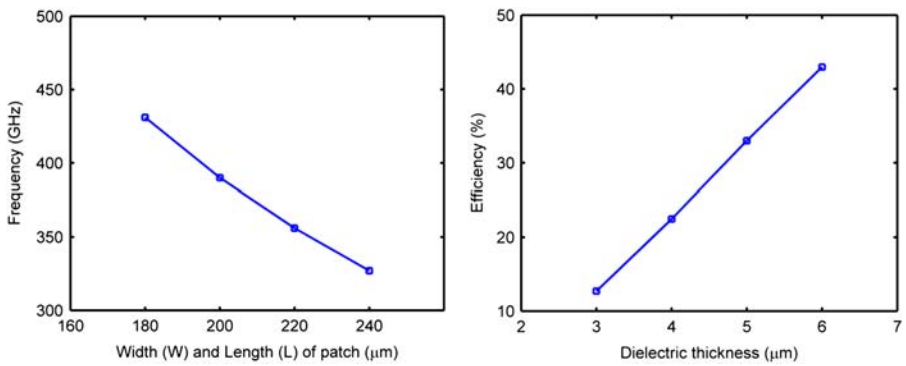

FIGURE 17.11

(a) Simulated resonant frequencies of the antennas for various patch sizes in square ($W = L$). (b) Simulated efficiency for various dielectric thicknesses between the patch and ground plane.

in CMOS [7]. The radiation from microstrip antennas occurs from the fringing fields between the edge of the patch conductor and ground plane. The fringing fields act to extend the effective length of the patch. Thus, the length of a half-wave patch antenna is slightly less than the half wavelength.

The aluminum pad layer is used to realize patch and Metal 1−5 layers shunted together are used as the ground plane to reduce ohmic losses. The dielectric thickness between the patch and the ground is 4 μm. The designed patch size of the antenna is $200 \times 200\ \mu m^2$. Figure 17.11a shows the simulated resonant frequencies of the on-chip microstrip patch antennas for varying sizes of a square-shaped patch antenna. The resonant frequency increases from 320 to 430 GHz when the

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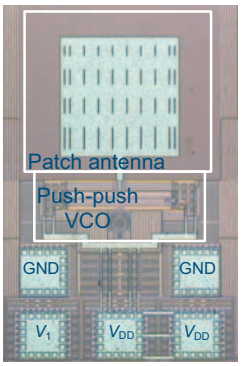

FIGURE 17.12

Die microphotograph of push-push oscillator [8].

patch size decreases from 240 to 180 μm. The simulated antenna efficiency against dielectric thickness is plotted in Figure 17.11b. In order to increase the dielectric thickness for higher efficiency, the aluminum pad layer is used for the microstrip patch instead of the top metal layer (Metal 6). An antenna with a smaller patch size has better efficiency at a given dielectric thickness. The simulated maximum directivity is 7 dBi in the broadside direction perpendicular to the patch. The oscillator is fabricated in a 45-nm logic CMOS technology. A die microphotograph of the push-push oscillator is shown in Figure 17.12. The overall chip size is $390 \times 640\ \mu m^2$ including bond pads.

17.2.2 QUASI-OPTICAL MEASUREMENT

It is challenging to detect sub-microwatt signals above 400 GHz using electronic instrumentation due to excessive loss [19]. For example, the conversion loss of a harmonic mixer for G-band (140−220 GHz) is ∼60 dB. Waveguide probes at the sub-THz frequency range are costly, which makes the measurement even more difficult. These issues can be resolved by employing a quasi-optical measurement technique using an FTIR (Fourier transform infrared) spectrometer and an on-chip antenna [8,9,34]. The FTIR system consists of a source, Michelson interferometer, and silicon bolometer. Figure 17.13 shows a photograph of the FTIR system used for the measurement. The FTIR system identifies a relative output power spectrum radiated from the on-chip antenna (Figure 17.14).

A bolometer was invented in 1878 by Samuel Pierpont Langley. It measures the energy of incident electromagnetic radiation. A bolometer is among the most sensitive detectors for sensing radiation including visible light, infrared radiation, and ultraviolet radiation, in amounts as small as one millionth of an erg [20]. It consists of an absorptive element connected to a heat sink through a thermal link. Changes in radiation cause changes in the electrical resistance of the

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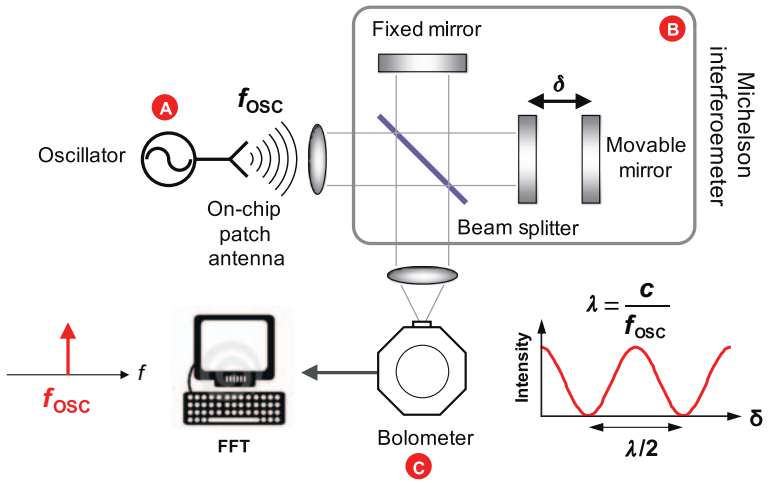

FIGURE 17.13

Schematic diagram of FTIR setup for the output spectrum measurement.

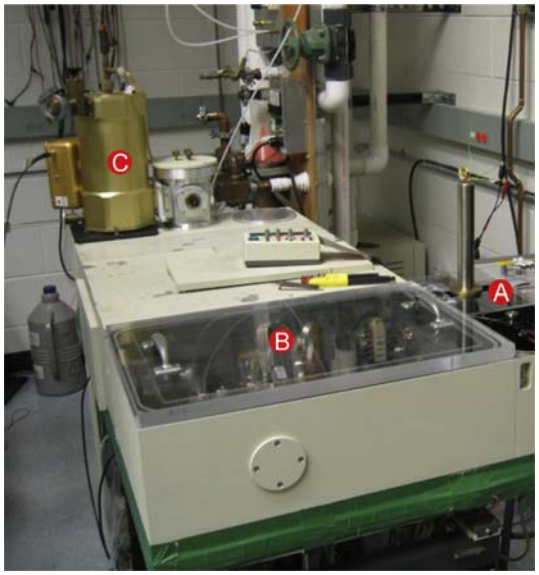

FIGURE 17.14

FTIR system used for the output spectrum measurement (Bruker ISF 113v).

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absorptive element. The absorptive element may be a platinum strip, a semiconductor film, or any other substance whose resistance is altered by slight changes in the amount of incident radiation falling on it [20]. The incident radiation is coupled to the absorptive element through a Winston cone in the bolometer [21]. Most bolometers use semiconducting or superconducting absorptive elements rather than metals. These devices are operated at cryogenic temperatures, significantly enhancing sensitivity.

The Michelson interferometer is an instrument that divides an incident beam into two distinct paths and then recombines the two beams [22]. A beamsplitter is located between the fixed mirror and the movable mirror. The beamsplitter divides the input beam of radiation into two beams. When the two beams are recombined, a condition is created under which interference can take place. The variation in the intensity of the beams seen by the detector is a function of the path difference and a plot of this intensity is known as an interferogram. The interferogram is converted to the desired spectral information using Fourier transform in an FTIR system.

The fabricated oscillators with the on-chip antenna are wire-bonded and mounted on a test board. This is placed in a holder for a source lamp of the FTIR system. A radiated output spectrum is scanned while the oscillator is operating. To de-embed the background radiation, a background spectrum is taken while the oscillator is turned off.

An absolute radiated power level is measured using the setup shown in Figure 17.15. An oscillator is placed immediately adjacent to the bolometer window. Noise and drift in the output signal of the bolometer make it difficult to identify a real signal, especially when the incident power level is low. The output signal of bolometer is measured using a lock-in amplifier, which can extract a small signal in an extremely noisy environment [23]. The oscillator is switched on and off by modulating its supply voltage using a signal generator. A reference signal for the lock-in amplifier is also provided by the signal generator.

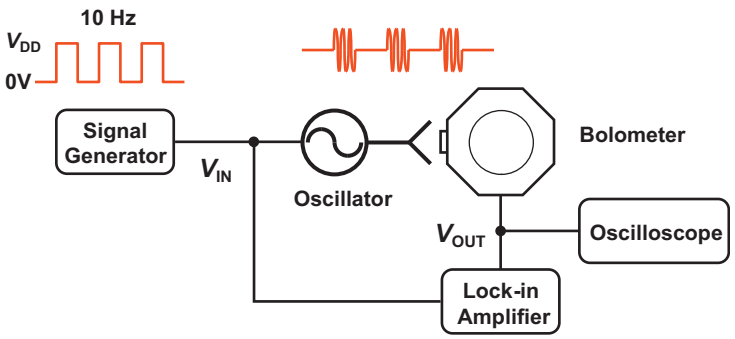

FIGURE 17.15

Output power measurement setup.

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The bolometer generates a modulated output signal proportional to the modulated incident radiation into the bolometer. An oscilloscope is connected to observe the modulated output signal from the bolometer. The output signal (voltage) is converted to a radiated power level using the responsivity of the bolometer provided by the manufacturer.

17.2.3 EXPERIMENTAL RESULTS

Figure 17.16 shows the spectrum of the radiated signal from the push-push oscillator chip measured using an FTIR system (Bruker ISF 113v) under normal atmospheric pressure at room temperature. A strong second harmonic component at 405 GHz and a weaker fundamental signal at 205 GHz are observed. A 5-mil Mylar beamsplitter is used to increase the sensitivity of the interferometer at 400 GHz.

The second harmonic power measured with the setup in Figure 17.15 is about −49 dBm. The radiated power is measured using a liquid helium-cooled Si bolometer (Infrared Laboratories HD-3) with responsivity of 4.0×10^4 V/W. The oscillator was powered by a 10-Hz square wave from a waveform generator to modulate the radiated power. The output signal from the bolometer was measured using a lock-in amplifier (Ithaco 393). The low measured power is likely due to the low gain of transistors at the operating frequency and interconnect losses due to the thin metal layers and dielectrics. There may be additional losses due to the mismatch between the resonant frequency of the on-chip antenna and oscillator output frequency. The circuit draws ∼11 mA from the supply voltage of 1.5 V. The oscillation frequency of oscillator decreases from 413 to 410 GHz with the increase of bias current from 11 to 7 mA (Figure 17.17).

The effect of inductor quality factor and substrate resistance on the output power is analyzed using Cadence simulations. Figure 17.18a shows the simulated second harmonic power at the push-push node. The output power increases

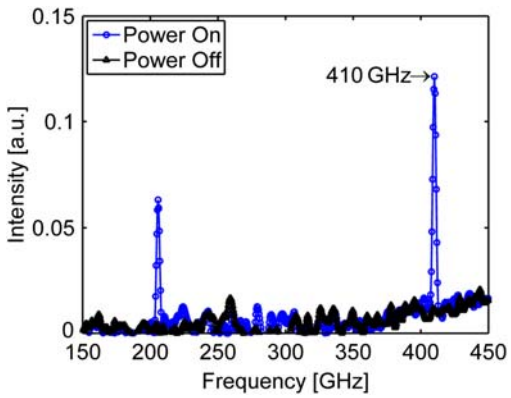

FIGURE 17.16

Spectrum of the 410-GHz push-push oscillator measured using an FTIR [8].

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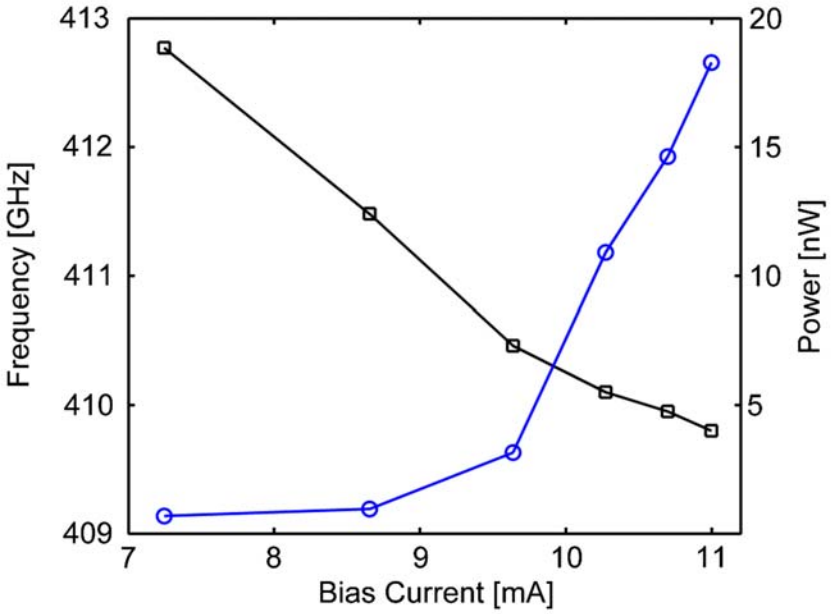

FIGURE 17.17

Frequency and power of push-push oscillator at varying bias currents [8].

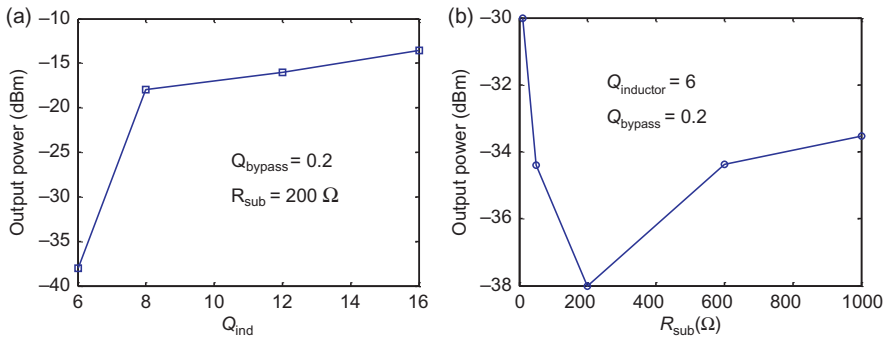

FIGURE 17.18

(a) Simulated second harmonic output power at the push-push node (a) for various quality factors of the inductor (Q_{ind}) and (b) for various substrate resistances (R_{sub}).

from -38 to -14 dBm as the quality factor of inductor (Q_{ind}) increases from 6 to 15. The quality factor of bypass capacitor (Q_{bypass}) and the substrate resistance of transistor (R_{sub}) is assumed to be 0.2 and 200 Ω, respectively. The oscillator stops oscillation when Q_{ind} is 4. Figure 17.18b shows the variation of the second

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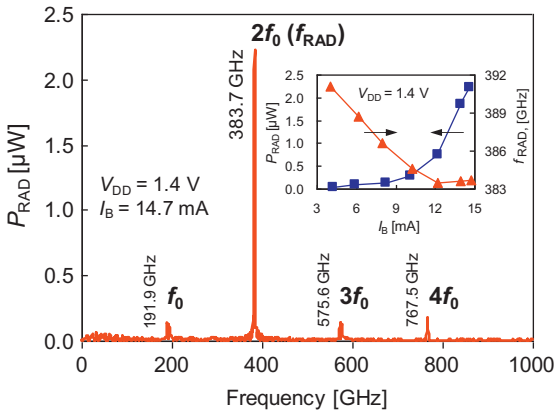

FIGURE 17.19

Measured spectrum of frequency doubled output near 390 GHz. (Inset) Measured radiated power (P_{RAD}) and radiation frequency (f_{RAD}) versus bias current (I_B) [24].

harmonic power with various substrate resistances with Q_{ind} of 6 and Q_{bypass} of 0.2. The second harmonic power increases while the substrate loss decreases for a small or large value of R_{sub} and is simulated to be -38 dBm for R_{sub} of 200 Ω. Figure 17.18a suggests that the quality factor of the inductor (Q_{ind}) is critically important for the second harmonic power and the output power can be increased up to -15 dBm by improving the quality factor using a better backend process. The efficiency of the antenna would also be enhanced by a thicker dielectric layer provided by a better backend process.

The design parameters of the oscillator have been tuned to obtain more output power at a similar frequency [24]. Figure 17.19 plots the measured spectrum of frequency-doubled output using the quasi-optical technique. The radiated power through the on-chip antenna connected to the oscillator is 2.2 μW at 383.7 GHz. This is more than 100× higher than that of the 410-GHz oscillator. This is due to better tuning of the antenna to the radiation frequency (f_{RAD}), ∼30% higher bias current (I_B), and use of metal-oxide-metal bypass capacitors instead of MOS capacitors. The unwanted harmonics are suppressed to more than 10 dB below the intended second-order harmonic output. The inset shows the measured radiated power and frequency variations against bias current. The oscillator consumes 21 mW from a 1.4-V supply. The radiated power of 2.2 μW is sufficient for rotational spectroscopy applications [25].

17.3 QUADRUPLE-PUSH OSCILLATOR IN CMOS

Higher harmonics of an oscillator can be extracted much beyond f_{max} of a device using a quadruple-push (four-push) technique. Recently two sub-THz CMOS

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oscillators have been reported based on a quadrature oscillator. A 324-GHz oscillator has been reported using a linear superposition of four phase-shifted fundamental signals at one-fourth of the output frequency (81 GHz) in Ref. [19]. However, the active linear combiner circuit for the superposition adds capacitive loading to the oscillator core which can reduce the operation frequency and increase power consumption of the circuit. A 1.3-THz signal has been generated in CMOS using the sixth harmonic of a quadruple-push oscillator using a negative resistance resonator in Ref. [26]. However, the signal is one of the unexpected and the fourth-order output power level was lower than those of the first three harmonics.

This section describes a quadruple-push oscillator fabricated using low-leakage transistors of a 45-nm CMOS technology (seven metal layers). The oscillator shows improved fourth harmonic current generation and suppression of unwanted harmonics. It radiates 220 nW of power at 553 GHz.

17.3.1 DESIGN CONSIDERATIONS

The quadruple-push signal generator is based on a quadrature oscillator [27]. Figure 17.20 shows a linear model of the quadrature oscillator. G_m and G_{mc} are the transconductance of cross-coupled core transistors (M_C) and coupling transistors (M_{CPL}), respectively. Due to the combination of direct and inverted connection between two oscillators, the output signals should have a quadrature phase offset to satisfy the Barkhausen criteria. Figure 17.21 shows the schematic of proposed quadruple-push oscillator with an on-chip antenna. The harmonic currents I_{CPL} in M_{CPL} are added by a passive combining network implemented with t-lines. Instead of using a separate linear combiner [19], this circuit utilizes the quadrature coupling transistors in the oscillator core as the combiner. This reduces the capacitive loading of the LC tanks by the gates of linear combiner

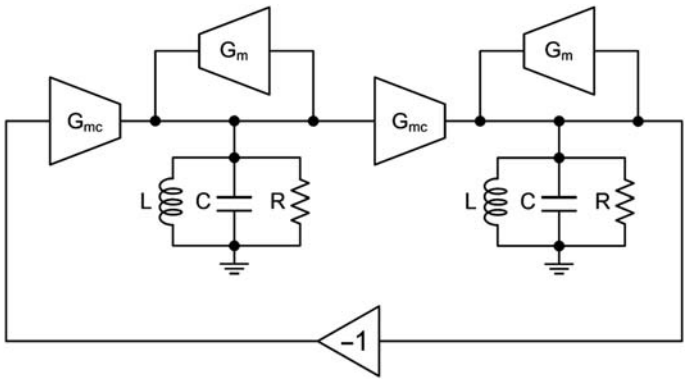

FIGURE 17.20

Simplified linear model of a quadrature oscillator [27].

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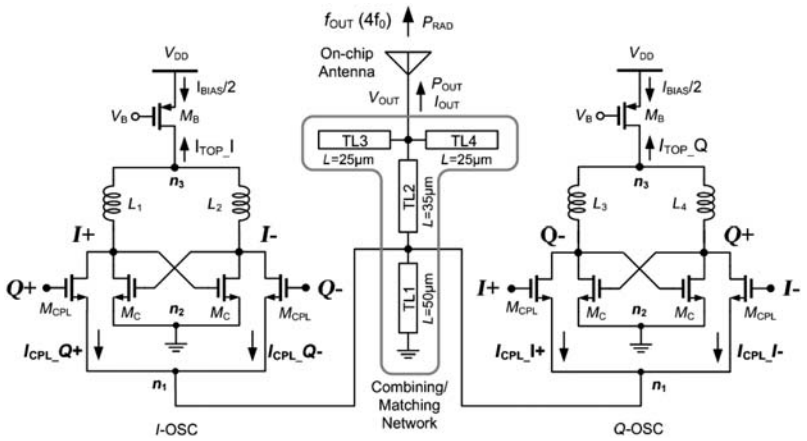

FIGURE 17.21

Schematic of quadruple-push oscillator schematic with an on-chip antenna [9].

circuit, which in turn allows the size of transistors in the quadrature oscillator core to be increased for higher output power.

All t-lines are once again implemented using a grounded coplanar waveguide (GCPW) structure with characteristic impedance of $\sim 45\ \Omega$ [16]. The width of the signal line (W_{TL}) is $\sim 6\ \mu$m, and the gap between the signal line and ground plane (G_{TL}) is $\sim 3.5\ \mu$m. The signal line is formed using the Al bond pad layer with thickness of $\sim 1.2\ \mu$m, and Metal 1 to Metal 3 layers are shunted together for the bottom ground plane. Three dimensional EM simulations using HFSS show that the GCPW has an effective permittivity (ε_{eff}) of 3.2 with 3-dB/mm loss at 600 GHz.

A single-turn circular inductor using the ~ 2.5-μm thick Metal 7 layer (M7) is employed for the LC tanks. The inductor has an outer diameter (d_L) of $\sim 30\ \mu$m and width (w_L) of $2.8\ \mu$m. In modern CMOS technologies, metal dummy fills are used to achieve a uniform metal density for the chemical mechanical polishing (CMP) process. Dummy fills adjacent to an inductor line have a strong impact on quality factor and self-resonant frequency of the inductor [28]. A custom dummy filling technique is employed to block out dummy fills near the inductor line. The inductor has a higher-density region around the center to meet the metal density rules. Poly-silicon dummy fills are uniformly spread under the inductor. Each dummy fill element has a minimum area allowed by design rules. The size and density of the dummy fills in Metal 1−6 layers is $0.4 \times 0.4\ \mu\text{m}^2$ and $\sim 30\%$, respectively. HFSS simulations show the differential inductance (L_{diff}) of 56 pH and quality factor (Q_{diff}) of 14 at 150 GHz [29]. Figure 17.22 shows the layout of the core inductor.

The sources of M_{CPL} (n_1 node) are terminated with a t-line matching network to maximize the power output at the fourth harmonic frequency. The nodes n_2

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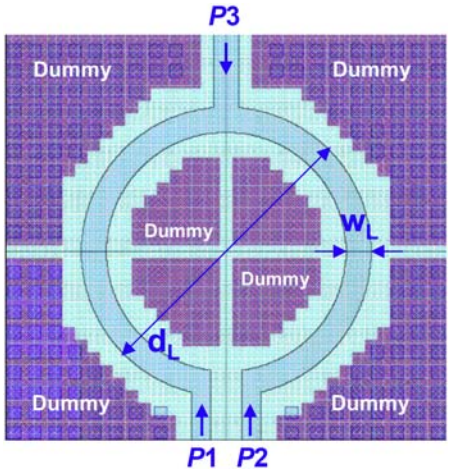

FIGURE 17.22

Core inductor of the quadruple-push oscillator.

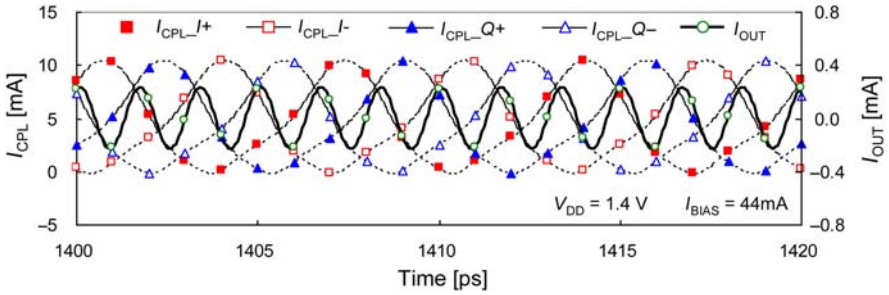

FIGURE 17.23

Simulated current waveforms in the oscillator [9].

and n_3 are potentially other nodes from which the fourth-order harmonic could be extracted. Simulations showed that the quadruple-push harmonic combining at the node n_2 and n_3 results in $\sim$30 and $\sim$50% lower output power, respectively, than that generated at the node n_1. The node n_3 would need long interconnects to the combining network in a typical symmetric layout of a quadrature oscillator to keep core and coupling transistors close together. The interconnects introduce additional losses and increase the layout complexity of the circuit.

Figure 17.23 shows simulated individual current waveform through M_{CPL} and the output node. They contain higher-order harmonics due to the nonlinearities in the oscillator. In the quadruple-push oscillator, only $4n$-th ($n = 1, 2, 3, \ldots$) order harmonics are constructively combined while other harmonics cancel as illustrated in Figure 17.24.

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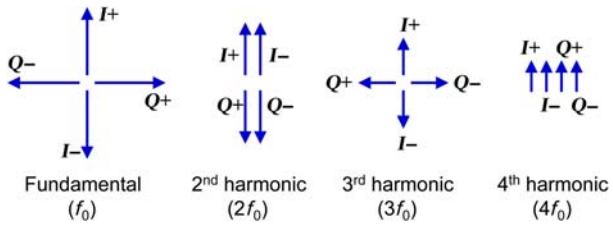

FIGURE 17.24

Quadruple-push operation [9].

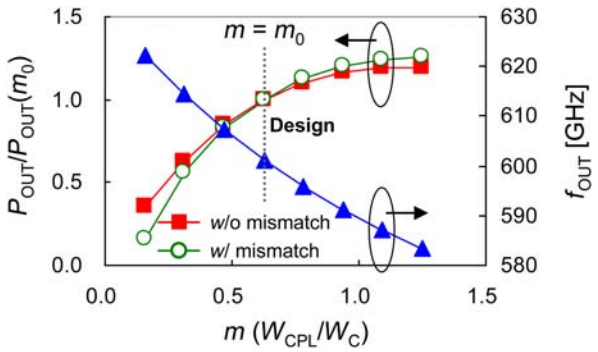

FIGURE 17.25

Simulated normalized output power ($P_{OUT}/P_{OUT}(m_0)$) and frequency (f_{OUT}) versus m (W_{CPL}/W_C) [9].

Increasing the coupling transistor widths can enhance the output power, but can also lower output frequency because of increased LC tank capacitance. Figure 17.25 shows the tradeoff between P_{OUT} (power delivered to the on-chip antenna) and f_{OUT} as function of the ratio between W_{CPL} and W_C as designed by 'm' The output power (P_{OUT}) saturates as m approaches one. The width of M_C and M_{CPL} is set to be $\sim$12 and $\sim$7.5 μm, respectively with the minimum gate length of 40 nm. Device mismatches, parasitic inductive coupling, and layout asymmetries lead to departure from the ideal quadrature generation in a quadrature oscillator [30]. The phase error degrades image suppression capability of a wireless receiver with an image-reject architecture. In the case of a quadruple-push oscillator, the phase error reduces the wanted fourth output power as well as loses the ability to suppress the unwanted harmonic powers. To analyze the effect of phase error on the output power, additional simulations are performed for the oscillator with 2% mismatch in the tank resonant frequency of the I- and Q-oscillators. The output power degrades less than 2% for m higher than 0.5 as shown in Figure 17.25. The level of frequency mismatch in real quadrature

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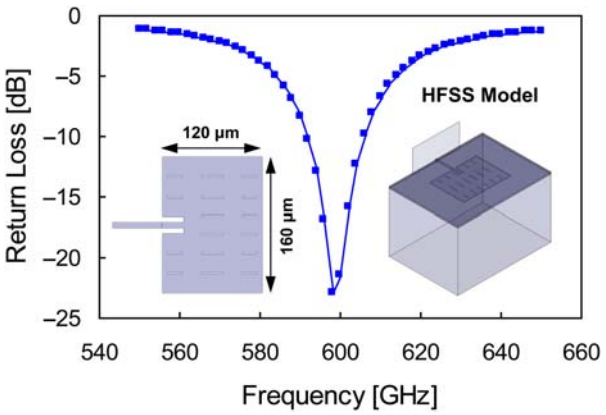

FIGURE 17.26

Simulated return loss of the on-chip microstrip patch antenna [9].

oscillators is expected to be $<0.1\%$. The quadruple-push oscillator should have an outstanding immunity to the phase error.

The on-chip antenna was once again implemented using a microstrip patch antenna [8]. The aluminum pad layer is used to form the patch. The ground plane is formed by shunting the Metal 1 to Metal 6 layers. The thickness of each metal layer is $\sim 0.2\ \mu m$. The separation between the patch and ground plane is $\sim 4\ \mu m$. HFSS simulations were performed to analyze antenna performance. The antenna exhibits a good input match around 600 GHz as shown in Figure 17.26. The peak gain and efficiency of the antenna are -0.2 dB and 28%, respectively, around 600 GHz. An inset-feed structure is used for input impedance matching. The patch size is $160 \times 120\ \mu m^2$. Figure 17.27 shows a die photograph of the fabricated oscillator. The layout was optimized for symmetry to minimize mismatches. The overall chip size is $540 \times 530\ \mu m^2$ including bond pads.

17.3.2 MEASUREMENT RESULTS

The chip is measured using the quasi-optical setup with on-chip antenna and a Fourier transform infrared spectrometer (Bruker ISF 113v) as described before [8]. A 23-μm-thick Mylar film is used for the beamsplitter. The oscillator spectrum is measured under normal atmospheric pressure at room temperature. Due to the intense molecular rotational transitions of water molecules, THz signals exhibit a strong atmospheric attenuation at some frequencies [31,32]. The attenuation is corrected using the Mercury arc lamp spectrum data measured in the atmosphere and vacuum. A strong attenuation is observed at the typical water vapor absorption lines at ~ 558, ~ 753, and ~ 989 GHz [33]. The atmosphere attenuation is measured to be $\sim 50\%$ at the 553-GHz output frequency of the oscillator.

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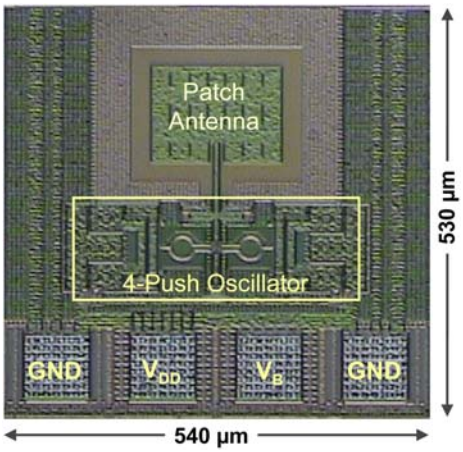

FIGURE 17.27

Quadruple-push oscillator die photograph [9].

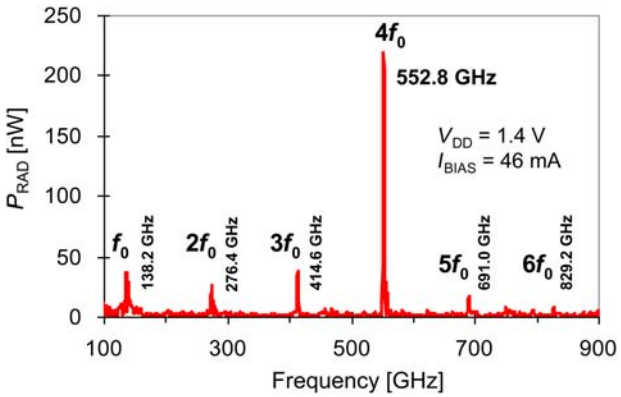

FIGURE 17.28

Measured spectrum of the radiated power [9].

Figure 17.28 plots the measured output spectrum and radiated power (P_{RAD}). The oscillator generated an output signal at 553 GHz with the power level of 220 nW. As can be seen, harmonics up to sixth order (829.2 GHz) were observed and the power levels of all unwanted harmonics are suppressed below 50 nW. However, the target operating frequency of the on-chip antenna is ~47 GHz higher than the measured output frequency of the oscillator. The frequency mismatch degrades input return loss and the overall efficiency of the antenna. The oscillator draws 46 mA of current from a 1.4-V supply. The radiated power is measured using the same set up used to measure the 410-GHz signal

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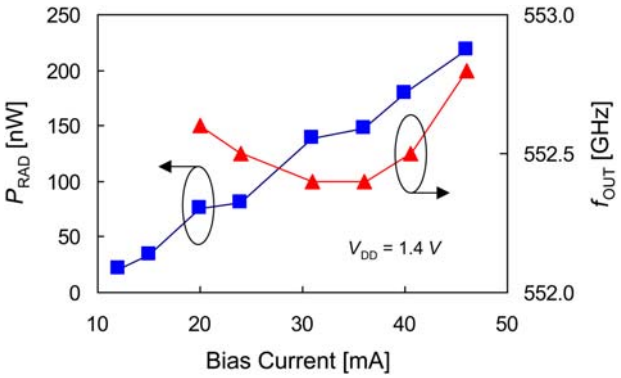

FIGURE 17.29

Measured radiated power (P_{RAD}) and output frequency (f_{OUT}) versus bias current [9].

generation circuit. Figure 17.29 plots the measured radiated power and frequency versus bias current. The circuit starts to oscillate at 12 mA and the radiated power monotonically increases with the bias current.

17.4 SUMMARY

This chapter describes the design considerations and measurement results for two sub-THz multiple-push oscillators to extract signals at frequencies much above f_{max} of the device technology. A 410-GHz push-push oscillator was implemented in a 45-nm logic CMOS process. The second harmonic is constructively combined while the differential fundamental signals are canceled. A quasi-optical measurement technique using an FTIR and an on-chip antenna is employed to characterize the output power spectrum. The output signal is coupled to an optical instrument by the antenna to detect −49 dBm radiated power at 410 GHz. The design parameters of the oscillator have been tuned to achieve more output power of 2.2 μW at 383.7 GHz.

A 553-GHz continuous wave signal was generated by a CMOS quadruple-push oscillator. Since the fourth harmonic current in a quadrature oscillator is directly added up by an embedded combining network, the oscillator does not need a separate active linear combiner. The oscillator generated an output signal at 553 GHz with the power level of 220 nW. The well-suppressed unwanted harmonic powers suggest that sufficient quadrature accuracy has been achieved in the oscillator.

These works demonstrate the feasibility of using a mainstream foundry logic CMOS process to fabricate oscillators that operate at sub-THz frequency. The oscillator would be readily integrated with digital circuits for DSP to implement practical and affordable sub-THz systems. This, however, is just the beginning

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and numerous technical challenges need to be overcome for the realization of practical CMOS sub-THz systems. The challenges include low output power of CMOS oscillators, uncertainties in characterization and modeling of the devices, and performance degradation of passive devices with the technology scaling. Further research and development for mitigating these issues should lead to the emergence of affordable sub-THz systems for security, healthcare, industrial, defense, and communication applications.

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