

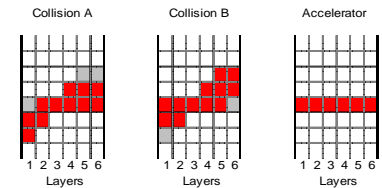
GENERAL COMMENTS ON ALCT OPERATION

TRIGGER

The algorithm is pipelined. All times and logic steps are based on 25 ns clock. Shown below are the steps of this pipeline.

1. One-shots. One-shots detect rising edges of signal on each of the ALCT inputs and start output pulses at that moment. The output pulse duration is 6 clocks (150 ns), which allows for coincidences of pulses in presence of drift time variations.

2. Pattern detectors. The outputs of the one-shots are supplied to the pattern detectors. Patterns of hits are searched for each key wire group, KeyWG (wire group in plane 3). Pattern detectors work independently for each KeyWG and can detect one of the two Collision muon patterns (C_A or C_B) and/or the Accelerator muon pattern (A). Collision patterns can be programmed by imposing mask bits starting from the *same* pattern envelope (see example in Figure: pattern envelope shown in red and grey, enabled patterns in red). Each block of 8 KeyWGs can have its own set of C_A - and C_B -patterns. The A-pattern is fixed. The two collision patterns have the following top-down Priorities: C_A , C_B .



- **nph_thresh** is a min number of planes hit for Pre-Trigger (common for all patterns, ranges from 0 to 6, default is 2). If the board detects nph_thresh or more layers hit in collision or accelerator patterns for a particular KeyWG, the pattern detection process starts for this WG. This event is called “pretrigger”. Pretrigger tags the time of when the track passed through the chamber (albeit some fixed delay).
- **nph_pattern** is the min number of planes (common for all patterns, default 4) required in the pattern after **drift_delay** time (default 4) to call it an ALCT. This check is done only if there was a pretrigger.
- Each pattern detector reports ALCT patterns with a 2-bit Quality: $Q = N_{hit} - nph_pattern + 1$, where N_{hit} is the actual number of hit layers in the pattern. Q takes values 1, 2, 3 (max). $Q=0$ in data format is used to signal that no corresponding ALCT (ALCT0 or ALCT1) is found and bits reserved for it in the data format contain no information.
- One or two of three patterns possibly found per KeyWG is reported, depending on the preset **trig_mode** parameter¹:
 - trig_mode=0:** The only mode that allows two patterns per KeyWG be reported. If only one of C_A - or C_B -patterns is found, it is reported. If both C-patterns are found, the best one, C_{best} , is selected—the pattern with the highest Quality; or C_A , if Quality bits are the same. The A-pattern, if found, is also reported independently of C-patterns.
 - trig_mode=1:** A-pattern only (C_A - and C_B -patterns are ignored)
 - trig_mode=2:** C_{best} -pattern only (A-pattern, if present, is ignored)
 - trig_mode=3:** C_{best} -pattern when there is not an A-pattern. However, if an A-pattern of any quality is present on the same KeyWG, the C-pattern is suppressed, and the A-pattern is reported.

3. Ghost Buster. A single muon passing through a chamber can be registered by two or more pattern detectors. To suppress extra patterns, a Ghost Cancellation Logic (GCL) is implemented. GCL analyzes the pattern detector outputs (collision and accelerator patterns are treated completely independently) and removes suspected ghosts, if:

- there is a pattern in the neighboring (± 1) KeyWG and in the same clock or up to 4 clocks before the pattern in question,
- this neighboring pattern is in the KeyWG of a larger number and has an equal or better quality than the ghost candidate,
- this neighboring pattern is in the KeyWG of a lower number and has a better quality than the ghost candidate.

4. ALCT0 and ALCT1 selector. The outputs of the Collision-GCL are connected to the best track selector that simply selects the Best Collision Pattern in a chamber (the pattern with the highest Quality; and larger KeyWG, if Q-bits are the same). Similarly, the Best Accelerator Pattern is selected from all A-patterns in a chamber. Then, one of these two Best Patterns, if both are present, is selected and reported as ALCT0 according to the **alct_amode** configuration variable:

alct_amode=0,1: report Best Collision Pattern if found, otherwise—Best Accelerator Pattern;

alct_amode=2,3: report Best Accelerator Pattern, if found, otherwise— Best Collision Pattern.

The ALCT1 pattern is picked after masking out the ALCT0 and repeating steps of this section.

DATA

An ALCT Board samples delay chip outputs (40 ns long) every 25 ns clock and stores 1/0 bits in the Output Buffer. For each time sample, ALCT0 and ALCT1 data are also stored in the Output Buffer. On arrival of L1A, the ALCT board checks if it had at least one ALCT within 3-BX wide window² properly aligned with respect to L1A. If yes, DAV signal is transmitted to DMB and, then, a data block of certain depth is extracted from the output buffer and pushed to DMB according to the following format.

¹ ALCT2001_spec.pdf note mistakenly refers to this suppression apparently being done earlier at the time of the pre-trigger coincidence.

² Window size is tunable up to 16 BXs (preset by the L1A_window parameter).

ALCT DATA FORMAT

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ALCT Header Data	0	1	1	0	0	Board_ID(3)			CSC_ID(4)			L1A(4)				hex: 6xxx	
	Reserved: 0				NotUsed				Tbins(5)			FIFO Mode					
	Reserved: 0				BXN(12)												
	0	Res0				Active_LCT_chips(7)				Readout_LCT_chips(7)							
	ALCT0(14:0)																
	ALCT0(29:15)																
ALCT1(14:0)																	
ALCT1(29:15)																	
Anode Raw Hit Data	0	LCT chip	Tbin=0				Ly0(7:0)										
		LCT chip	Tbin=0				Ly0(15:8)										
		LCT chip	Tbin=0				Ly1(7:0)										
		LCT chip	Tbin=0				Ly1(15:8)										
		LCT chip	Tbin=0				Ly2(7:0)										
		LCT chip	Tbin=0				Ly2(15:8)										
		LCT chip	Tbin=0				Ly3(7:0)										
		LCT chip	Tbin=0				Ly3(15:8)										
		LCT chip	Tbin=0				Ly4(7:0)										
		LCT chip	Tbin=0				Ly4(15:8)										
		LCT chip	Tbin=0				Ly5(7:0)										
		LCT chip	Tbin=0				Ly5(15:8)										
		LCT chip	Similar data for all other Tbins in readout (12 frames per Tbin)														
Similar blocks for all other chamber sections ("LCT chips")																	
ALCT data Trailer	1	1	0	1	0	22-bit CRC (lowest 11 bits)											hex: Dxxx hex: Dxxx hex: DE0D hex: Dxxx
	1	1	0	1	0	22-bit CRC (lowest 11 bits)											
	1	1	0	1	1	1	0	0	0	0	0	0	1	1	0	1	
	1	1	0	1	a	0	10-bit ALCT Frame Count (# of 16-bit words)										
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

ALCT0 and ALCT1 bits (0:29)	
Bits	Description
29:17	Reserved
12:16	Five low bits of BXN counter tagged by the ALCT
11:5	Key wire group the ALCT is associated with
4	if bit4=1 and bit3=0, this is CollisionB pattern; if bit4=0 and bit3=0, this is CollisionA pattern
3	if bit3=0, this is either CollisionA or CollisionB pattern; if bit3=1, this is Accelerator pattern
2:1	Quality of a pattern
0	if bit0=1, there is a valid ALCT (the above bits are meaningful)

Event size with FIFO Mode =1 (full readout³). The number Tbins here runs from 1 to 32.

Event Size = (4 + 4 + N*Tbins*12 + 4) words			
ALCT Type	N	Event Size (Tbins=8)	Event Size (Tbins=32)
ALCT-288	3	300	1164
ALCT-384	4	396	1548
ALCT-672	7	684	2700

³ For FIFO mode=0, the size is 12.

Board_ID(3)	Programmable via JTAG, configuration register bits [55:53], the meaning is to be defined by user								
CSC_ID(4)	always 0, the meaning is to be defined by user								
L1A(4)	L1A number								
NotUsed	<table> <tr> <td>bit 7: L1A</td> <td>always 1</td> </tr> <tr> <td>bit 8: Ext</td> <td>always 0</td> </tr> <tr> <td>bit 9: 1st</td> <td>always 0</td> </tr> <tr> <td>bit10: 2nd</td> <td>always 0</td> </tr> </table>	bit 7: L1A	always 1	bit 8: Ext	always 0	bit 9: 1st	always 0	bit10: 2nd	always 0
bit 7: L1A	always 1								
bit 8: Ext	always 0								
bit 9: 1st	always 0								
bit10: 2nd	always 0								
Tbins(5)	number of time samples of raw anode hit dump								
FIFO Mode(2)	=0, no Anode Raw Hit Data (only Header + D-Trailer) =1, full readout with raw data hits (as shown) =2, local readout (not implemented)								
BXN(12)	BXN at time of L1A arrival minus the preset L1A_delay								
Active_LCT_chips (7)	ALCT288: 0000111, ALCT384: 0001111, ALCT672: 1111111 (all numbers are binary)								
Readout_LCT_chips (7)	ALCT288: 0000111, ALCT384: 0001111, ALCT672: 1111111 (all numbers are binary)								
ALCT0(30) and ALCT1(30)	—two earliest ALCTs from the L1A_window (see footnote on page 1). Note that there may be up to two ALCTs per each BX in the window---only the two earliest ones will be reported.								
LCT chip(2)	counts chamber sections (1 section = 16 wire groups per plane). For historical reasons these sections are called “LCT chips”. They are counted from the narrow end of a chamber. N = 3 for ALCT-288 (ME1/1, ME1/3) N = 4 for ALCT-384 (ME234/2, ME1/2) N = 7 for ALCT-672 (ME234/1). Data format reserves only two bits for “LCT chip”, so its value runs as 0, 1, 2, 3, 0, 1, 2. Unused sections in ME1/3 and ME3/1, ME4/1 have zeros for non-existent wire group channels.								
a=1 or 0	TMB counts CRC sum for ALCT data and checks it against CRC reported in the ALCT trailer. If there is a match, a=1 (good data transmission). If there is a mismatch, a=0. This feature is introduced since October 2004 Test Beam (before that it was always 0).								

Rev 1 References:

- Corrections and clarifications per private communications with A. Madorsky, June 2004
- http://www-collider.physics.ucla.edu/cms/trigger/alct2001/alct2001_spec.pdf (last updated 14 April 2003)

Rev 2 References:

- Bit *a* is introduced in the ALCT trailer—private communication with M. von der Mey, October 6, 2004
- Table with ALCT event sizes is corrected (A. Korytov)

Rev 3 References:

- Correction of a typo in Bit4 description of the ALCT pattern bits, August 26, 2005