

## GENERAL COMMENTS ON DDU OPERATION

Note that there are some difference in data formats between the DDU used in the May-June 2004 Beam Tests (DDU-2003) and the new DDU revision (DDU-2004) to be used since September 2004. These differences are explicitly spelled out in this note. The primary reason for the changes is to comply with the new CMS requirements on Header/Trailer formats (see <http://cmsdoc.cern.ch/cms/TRIDAS/horizontal/RUWG/>). Also as of September 2004, DMB data format as it appears in the data stream will be different: so-called “9”-words no longer will be suppressed by the DDU-2004. The sequence of four 16-bit “9”-words will be changed as well (the DMB note will be updated accordingly). The so-called “lone” DMB words (or “8”-words) will continue to be suppressed.

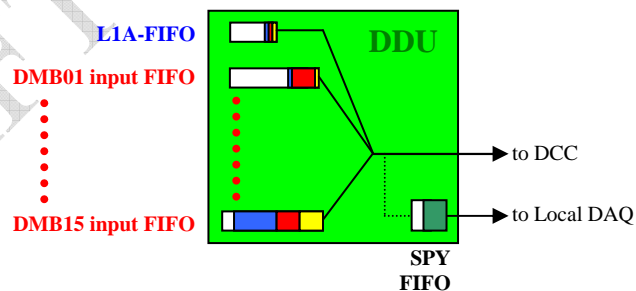
DDU receives L1A (L1A and BXN numbers are recorded in a dedicated L1A-FIFO) and expects to receive either DMB\_DAV words from DMBs with data (four 16-bit words with 1001 for bits 15-12) or DMB lone words from DMBs without data (four 16-bit “8”-words with 1000 for bits 15-12). In due time but asynchronously, all DMBs with data start pushing data in DMB INPUT FIFOs (see DMB data format). There is a timeout cut-off: if data did not arrive or transmission did not end from one of DMBs that reported DAV words, timeout error will be generated by DDU. In this case, a reset will be required.

DDU pulls out data from DMB INPUT FIFOs and L1A-FIFO, merges them in one event (16-bit DMB words are stacked to make 64-bit DDU words), and pushes the event data further down the chain via S-Link (DDU-2004) or via DCC data path (DDU-2004). In principle, the receiving side must be able to digest the expected data flow rate. If the receiving side is not ready, it may request DDU to stop sending data (note that this may lead to filling up the input FIFOs—see next paragraph).

If any of the input FIFOs ever gets full<sup>1</sup>, even temporarily, then the system synchronization is likely to be lost and the whole system must be reset. Otherwise, data corruption may occur (e.g., DDU events may become assembled from DMB events originating from different L1As, DMB records may get truncated, etc.).

In addition, DDU puts the same event in the Giga-Bit Ethernet SPY FIFO, from where the stored events are pulled out, Ethernet-formatted, and pushed to a local DAQ PC. Since the Ethernet link is much slower, it cannot keep up with the maximum DDU data flow rate. To avoid conflicts, DDU checks the status of the SPY FIFO and stops sending data into it when the FIFO is nearly full (the threshold is tunable).

And finally, DDU makes a number of checks on its own status as well as on the status of an event it assembles and adds ERROR\_STATUS bits to the header and the trailer (see DDU data format). Based on these checks, DDU can also communicate to FMM requests for resets and various status conditions.



<sup>1</sup> E.g., because of high input rate or because of a request from the receiving side to stop sending data...



**Header 1<sup>2</sup>**

0101:	CMS directive, marks Beginning-Of-Event (it is not a unique combination!--it can and does occur inside the DMB data stream)
EVT_TYPE(4):	CMS Directive
L1A(24)	DDU L1A counter
BXN(12)	BX number at L1A (reset on every LHC orbit) as read out from the DDU L1A Counter <sup>3</sup> .
SOURCE_ID(10+2):	10 bits must unambiguously identify the source board (CMS directive) +2 bits left for sub-detector internal use
Format_Rev(4)	Data format version (currently, =5, 4, 3 for DDU-2005, -2004, -2003 formats).
free(4):	CMS Directive (S-Link status, not fully defined yet; see <a href="http://cmsdoc.cern.ch/cms/TRIDAS/horizontal/RUWG/">http://cmsdoc.cern.ch/cms/TRIDAS/horizontal/RUWG/</a> for more details)
x	x's mark reserved, but not yet defined bits (not available for EMU)

**Header 2**

hex 8000.0001.8000.****	Unique pattern near the start of the event packet.
DMB_FIFO_FULL_STATE(15):	Shows which DMB FIFOs (on DDU inputs) reached FULL state (=1, if full). <b>Reset is required.</b>

**Header 3**

DDU_COONNECTED_INPUTS(15):	DDU inputs physically connected to DMBs.
DMB_DAV(15)	Marks all DMBs that have data
DMB_Active(4)	Counts how many DMBs have data (up to 15)
<b>DDU_OUTPUT_STATUS(16):</b>	
<b>EVT_BEGIN_STATUS(7):</b>	
<b>DDU_TTS(4):</b>	

**Trailer-2**

hex 8000.FFFF.8000.8000	Unique pattern near the end of the event packet.
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**Trailer-1**

DDU_ERROR_STATUS (32):	See summary below. The status is evaluated at the time of transmitting this word.
CSC_ERROR_STATE(15)	Marks all DDU inputs corresponding to CSCs sending corrupted data (see below)
CSC_WARNING_STATE(15)	Marks all DDU inputs corresponding to CSCs reporting warnings (see below)

**Trailer<sup>4</sup>**

1010:	CMS directive, marks End-Of-Event
DDU_WORD64_COUNT(24)	Actual count of 64-bit words in this event fragment, including Header 1 and Trailer.
DDU_CRC(16)	DDU CRC 16-bit word
EVT_STATUS(8):	CMS Directive: sub-detectors should provide status of event and hardware; no details yet. Currently, =
<b>DDU_TTS(4):</b>	see Header comments
free(4):	see Header comments
x	see Header comments

<sup>2</sup> At the moment, the Header 1 and Trailer in this format are made to match the CMS DAQ requirements for sub-detector data formats. However, DDUs are no longer the last EMU boards before the Global CMS DAQ—Data Concentration Card (DCC) takes this role by packing data from up to 9 DDUs and sending them via S-LINK64 to CMS DAQ. Therefore, changes in DDU headers/trailers are possible in future.

<sup>3</sup> May be changed to be BXN as recorded by either DMB, TMB, LCT (matching with DDU BXN is required)

<sup>4</sup> See footnote for the Header 1 description

**DDU\_OUTPUT\_STATUS(16) in DDU-2005 Format:**

**EVT\_BEGIN\_STATUS(7) in DDU-2005 Format:**

**DDU\_STATUS\_ERROR(32) in DDU-2005 Format:**

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**DDU\_STATUS\_ERROR(32) in DDU-2004 Format**

Note 1: In the table below, grouping and order of bits are based on their logical meaning. The error checks are expected to change as often as needed.

Note 2: Y/N in columns H and T indicates whether a particular DDU\_STATUS\_ERROR bit can/cannot be updated in Header3 and Trailer-2, respectively.

Note 3: Kinds of RESET (sync, hard) and on whether it happens on a single or multiple error occurrences are to be defined later.

Note 4: The most notable change wrt DDU-2003 Format: Bit37 has been completely redefined (and moved to another group of bits in this note).

	Bit	Short Description	Comments	H	T	Event S-link	Integrity SPY	RESET Req'd <sup>5</sup>
Input Data Transmission Errors/Warnings	56	No Live Fibers	No DDU fibers are physically connected.	Y	Y	no data	no data	Status Only
	34	Lost/New Fibers	Lost/New DDU fiber physical connections wrt the status after last Reset.	Y	Y	BAD	BAD	Reset Req'd
	55	One Event Bit-Vote Error	First event with a bit-vote failure per 64-bit word on an input fiber channel.	Y	Y	BAD	BAD	Status Only
	36	Second Bit-Vote Error	Second event with a bit-vote failure per 64-bit word on the same input channel.	Y	Y	BAD	BAD	Reset Req'd
	43	Hardware Bit Errors	Bit error detected in de-serializing hardware.	Y	Y	BAD	BAD	Reset?
	38	Timeout Error	Data from a fiber input either never started or never finished.	N	Y	BAD	BAD	Reset Req'd
DDU FIFO Errors & Warnings	44	INPUT FIFO Near Full	One or more DMB INPUT FIFOs or L1-FIFO are nearly full.	Y	Y	OK	OK	Status Only
	35	INPUT FIFO Full	One or more DMB INPUT FIFOs or L1-FIFO are full. Data/Sync. may be lost.	Y	Y	BAD	BAD	Reset Req'd
	58	L1A-FIFO Full	L1A-FIFO is full. Some triggers/events may be lost or garbled.	Y	Y	BAD	BAD	Reset Req'd
	57	Data Stuck in FIFO	One or more INPUT FIFOs have data, but no trigger was received.	Y	Y	BAD	BAD	Reset Req'd
	63	DDU Output Constricted	Any of input FIFO going full because of a request from DCC not to send data.	Y	Y	BAD	BAD	Reset Req'd
FPGA	42	Control FPGA Clock-DLL Error	DDU lost its clock for some time; some S-Link and SPY data may have been lost.	Y	Y	OK?	OK?	Reset Req'd
DMB Event Structure/Content Errors & Warnings	59	Wrong First Word	First word for at least one FIFO is inconsistent with the first word signature	Y	Y	BAD	BAD	Status Only
	39	Corrupted Control Word Sequence	Detected wrong control word sequence, probable fatal data loss or mixed event data <sup>6</sup>	N	Y	BAD	BAD	Reset Req'd
	40	Missing Control Words	Failed to find expected control words within an event <sup>7</sup>	N	Y	BAD	BAD	Status Only
	33	DMB-DDU L1A Mismatch	DMB-DDU L1A event numbers mismatch for at least one CSC	Y	Y	BAD	BAD	Reset?
	37	TMB/ALCT CRC Error	TMB/ALCT CRC check failed	N	Y	BAD	BAD	Reset?
	48	TMB/ALCT-DDU L1A Mismatch	TMB/ALCT-DDU L1A numbers mismatch for at least one CSC	N	Y	BAD	BAD	Reset?
	49	TMB/ALCT Word Count Error	TMB/ALCT word count inconsistent	N	Y	BAD	BAD	Reset?
	50	ALCT Error	ALCT DAV exists, but: (no ALCT Trail).or.(ALCT-DDU L1A error).or.(CRC-error).or.(Word Count error)	N	Y	BAD	BAD	Reset?
	51	TMB Error	TMB DAV exists, but: (no TMB Trail).or.(TMB-DDU L1A error).or.(CRC-error).or.(Word Count error)	N	Y	BAD	BAD	Reset?
	32	CFEB CRC Error	CRC-error for ADC time-sample data on one or more CFEBs	N	Y	BAD	BAD	Reset?
41	CFEB Lost Samples	B-code encountered in at least one DMB/CFEB (SCA Full Condition)	N	Y	BAD	BAD	Status Only	
OR	45	DDU Single Event Warning	Problem detected, possibly not bad or fatal error (can be modified, now set to be OR of bit55, bit42)	Y	Y	OK?	OK?	Status Only
	46	DDU Single Event Error	OR of all possible "bad event" cases.	Y	Y	BAD	BAD	Reset?
	47	DDU Critical Error	OR of all possible "RESET required" cases.	Y	Y	BAD	BAD	Reset Req'd
S-link Errors	52	S-Link Not Ready	No active S-link connection, no will be sent via S-Link (bit52=1 can be seen only in SPY data; SPY data are OK)	Y	Y	no data	OK	Status Only
	53	S-Link Full Bit Present	Data will not be sent if "active S-link" is present (bit53=1 can be seen only in SPY data steam)	Y	Y	no data	OK	Status Only
SPY-ing Errors	54	SPY FPGA Clock-DLL Error	SPY FPGA lost its clock for some time; some SPY data may have been lost/wrong.	Y	Y	OK	OK?	Status Only
	60	SPY Fiber Error	Fiber connection is not present. Does not affect S-Link data flow.	Y	Y	OK	no data	Status Only
	61	SPY FIFO Near Full	Giga-Bit Ethernet FIFO is close to being full.	Y	Y	OK	OK	Status Only
	62	SPY FIFO Full	Cannot get full if DDU operates properly. Does not affect S-Link data flow.	Y	Y	OK	BAD	Status Only

<sup>5</sup> Error bits resulting in RESET REQUIRED persist until the RESET occurs. Questionable cases (in gold) are for mitigation of recurring errors. TBD: sync/hard reset distinctions.

<sup>6</sup> Found inside an event at least one of the following: Extra DMB\_Header1, Extra DMB\_Header2, Lone Word, Extra TMB/ALCT\_Trailer, Extra DMB\_Trailer1, DMB\_Trailer2

<sup>7</sup> Missing TMB/ALCT\_Trailer word, missing DMB Header word, Wrong First word, or Extra Control words.

**Rev 3**            Drastic changes in DDU Header/Trailer Formats as of September 2005

**References:**    <http://www.physics.ohio-state.edu/~cms/ddu/ddu2.html> (last updated 19 April 2004)  
private communications with J. Gilmore and J. Gu (April 2004)  
checked and updated by J. Gilmore (August 2004)

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