

GENERAL COMMENTS ON DMB OPERATION

Up to 5 CFEBs, ALCT, and TMB boards (further to be referred to as FEBs) in first approximation communicate with DMB independently from each other¹.

If an L1A signal is in coincidence with an LCT on a FEB, the board does two things:

- Sends DAV signal to DMB (DAV signal is synchronized with L1A)
- Starts pushing data into a corresponding FIFO on DMB (at the end of transmitting all data corresponding to one event, a special marker is placed in the FIFO)

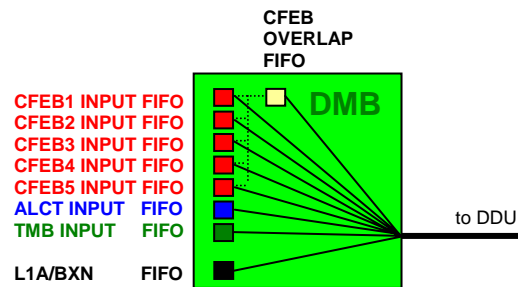
On each arriving L1A (L1A and BXN are counted and stored in L1A/BXN FIFO), DMB checks if any of the FEBs have sent DAV signal.

If none of the boards reported DAV signal within 3-BX window² around a properly delayed³ L1A signal, DMB sends four so-called lone 16-bit words (with 1000 for bits 15-12) to DDU—see Fig.1 for its format.

If some FEB-DAV signals arrived within the 3-BX window, DMB first sends DMB-DAV signal to DDU (four 16-bit words with 1001 for bits 15-12, also known as *Header1*), then pulls out data from corresponding input FIFOs, assembles an event, and finally sends it to DDU—see Fig.2 for format.

DMB pulls out all the data from FIFO until it sees the special tag marking the end of the event. As DMB assembles an overall event, it does not try to correlate BXN, L1A numbers in the data pulled out from different FIFOs. Overflow of any of the input FIFOs (e.g., at very large rate of incoming data) will break synchronization between FEBs and DMB, which will result in:

- corrupted data, i.e. more than one event buffer may be readout when end-of-event tags are lost,
- CFEB, ALCT, TMB data from different events may start getting assembled together.



Note: If the DAV×L1A coincidence window is mistuned on DMB, then for each new event FEB will be sending DAV signals and pushing data in its INPUT FIFO on DMB, but DMB, not seeing a DAV×L1A coincidence, will not pull out the data for this L1A. The INPUT FIFO will soon get filled. Also, no data for this FEB will ever appear in the data stream.

CFEB specifics: In the case when some SCA samples overlap between two events separated by short time, these samples are tagged as overlapped at the time of pushing the earlier event. After assembling the first event, the overlap-tagged samples are not disposed of, but rather stored in OVERLAP FIFO. When DMB assembles the second event, it first pulls out the stored samples from the OVERLAP FIFO, and then complements them with remaining new samples from CFEB INPUT FIFO. There is only one OVERLAP FIFO for all 5 boards. The OVERLAP FIFO is sufficiently large (can contain one full 16-sample event from 5 CFEBs) and therefore under no circumstances can get full as long as the board works properly.

¹ Technically, this is not true: ALCT and TMB use the same FIFO_WRITE_CLOCK. Also, ALCT data are de-multiplexed on TMB.

² The window size for matching DAV signals from CFEBs/ALCT/TMB with L1A signal is tunable. Strictly speaking, since all DAV signals are synchronized with L1A, one can require their coincidence within a single BX. The 3-BX window is effectively the same at LHC due the CMS rule of no more than 1 L1A signal per 3 BXs.

³ The window position for matching DAV must be tuned for all chambers to accommodate the differences in cable length and muon times of flight.

DMB-2005 DATA FORMAT (as of September 2005)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMB lone word	8	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	0	0	0	DMB_LA1(11:0)											
		1	0	0	0	DMB_LA1(23:12)											
		1	0	0	0	DMB_BXN(11:0)											

this DMB lone word will be suppressed by DDU

Fig. 1. If no data are available for a given L1A (neither of 5 CFEBs nor ALCT nor TMB reported DAV signal within 3-BX window around L1A signal), DMB sends a so-called lone word (actually, four 16-bit words).

DMB-2005 Production Data Format

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
9	1	0	0	1	DMB_LA1(11:0)													
	1	0	0	1	DMB_LA1(23:12)													
	1	0	0	1	a	b	CFEB_ACTIVE(5)					CFEB_DAV(5)						
	1	0	0	1	DMB_BXN(11:0)													
A	1	0	1	0	a	c	b	c	a	c	b	CFEB_DAV(5)						
	1	0	1	0	DMB_CRATE(8)							DMB_ID(4)						
	1	0	1	0	CFEB_MOVL(5)					DMB_BXN(7)								
	1	0	1	0	DMB-CFEB_Sync(4)				DMB_L1A(8)									
	0	ALCT data																
	0	TMB data																
	0/1	CFEB data																
F	1	1	1	1	DMB_BXN(4)				DMB_LA1(8)									
	1	1	1	1	CFEB_MOVL(5)					d	e	CFEB_FIFO_HALF(5)						
	1	1	1	1	DMB_L1_PIPE(8)										f	g	h	i
	1	1	1	1	CFEB_ENDTIMEOUT(5)					j	k	CFEB_STARTTIMEOUT(5)						
E	1	1	1	0	l	m	CFEB_FIFO_FULL(5)					CFEB_FIFO_EMPTY(5)						
	1	1	1	0	DMB_CRATE(8)							DMB_ID(4)						
	1	1	1	0	n	22-bit CRC (lower 11 bits: 10:0)												
	1	1	1	0	o	22-bit CRC (higher 11 bits: 21:11)												
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

repeat 12 bits of Header 6

Fig. 2. If data are available for a given L1A (at least one of CFEBs or ALCT or TMB reported DAV signal within 3-BX window around L1A signal), DMB waits certain time to collect data and then sends the data in this format.

B-WORDS

Normally, data blocks have bit 15 = 0. However, words with B-signature (bits 12-15 = 1011) can appear in CFEB data block. They are intended to signal problems with CFEB data (see the note on CFEB data format for details).

C-WORDS

Words with C-signature (bits 12-15 = 1100) can be used to help re-align data format if one or more boards send corrupted data.

DMB-2005 DATA FORMAT COMMENTS

DMB_L1A(varies)	L1A Event Number (redundant copies from the same DMB counter)
DMB_BXN(varies)	Bunch Crossing Number corresponding to L1A (redundant copies from the same DMB counter)
a TMB_DAV	=1, if TMB data exists for this event, i.e. there was a DAV signal from TMB matching current L1A.
b ALCT_DAV	=1, if ALCT data exists for this event (same as above, but for ALCT)
CFEB_DAV(5)=xxxxx	tags CFEBs that will send data to DMB (same as above, but for CFEBs)
CFEB_ACTIVE(5)=zzzzz	CFEBs that should send data as judged by the TMB board: CLCT(s) was (were) found and matched L1A within ± 1 BXs window ⁴
c CFEB ACTIVE-DAV mismatch=1,	if 5-bit segments CFEB_ACTIVE(5) and CFEB_DAV(5) do not match
CFEB_MOVLP(5)=xxxxx	if a bit corresponding to a particular CFEB is 1, some time sample(s) for this event would have multiple (>2) overlaps with samples from previous events. In this case: CFEB data for this event are NOT sent at all. CFEB_DAV signal is NOT sent either. <i>Note: CFEB_MOVLP=1 can be only in events with CFEB_DAV=0 for this board</i> <i>Note: Due to the CMS trigger rule of no more than two L1A signals within 625 ns, CFEB_MOVLP=1 can occur at LHC only for 16-sample CFEB readout mode (see the note on CFEB data format).</i>
DMB_CRATE(8)	peripheral crate ID from DMB (mapping to actual sectors/stations is not yet set)
DMB_ID(4)	position of DMB in the crate = (slot number in the crate)/2; allowed values: 1, 2, 3, 4, 5, -, 7, 8, 9, 10
DMB-CFEB-Sync(4)	4-bit counter of BXs from last SyncReset to L1A. Can be used to check DMB-CFEB synchronization: The least significant bit of TRIG_TIME(8) + L1A_phase(1) on CFEBs make similar 4-bit counters (albeit for some constant offset, e.g. due to various cable lengths)
DMB_L1_PIPE(8)	number of L1As backed-up in the DMB (yet to be send to DDU, not counting the one being sent now) $N = \text{bits}(7:1) \times 8^{\text{bits}(8)}$, i. e. $N_{\text{max}} = 63 \times 8 = 504$ <i>Note: expect to be 0 at low rates</i> <i>Note: the data waiting to be sent to DDU are backed up in the INPUT FIFOs</i> <i>Note: It takes ~20 full events to fill up INPUT FIFOs; so 8-bit counter appears to be much too deep.</i> <i>However, at LHC we expect only 5% of chambers reporting DAV signals per L1A. Therefore, INPUT FIFOs can absorb as many ~400 L1As before getting full—it is this number that drives the 8-bit depth of the L1PIPE counter.</i>
d ALCT_FIFO_HALF	=0, if ALCT INPUT FIFO is more than HALF FULL (warning); =1 if less than half-full (OK)
e TMB_FIFO_HALF	=0, if TMB INPUT FIFO is more than HALF FULL (warning); =1 if less than half-full (OK)
CFEB_FIFO_HALF(5)	=0, if CFEB INPUT FIFO on the DMB is more than HALF FULL (warning); =1 if less than half-full (OK)
f ALCT_FIFO_EMPTY	=1, if ALCT INPUT FIFO on the DMB is empty (OK), “not empty” is the first sign of high rate
g TMB_FIFO_EMPTY	=1, if TMB INPUT FIFO on the DMB is empty (OK), “not empty” is the first sign of high rate
CFEB_FIFO_EMPTY(5)	=1, if CFEB INPUT FIFO on the DMB is empty (OK), “not empty” is the first sign of high rate <i>Note: No events beyond the one being read out—being empty is OK; one must expect 1 at low rates.</i>
l ALCT_FIFO_FULL	=1, if ALCT INPUT FIFO on the DMB is full (bad! – re-sync will be required)
m TMB_FIFO_FULL	=1, if TMB INPUT FIFO on the DMB is full (bad! – re-sync will be required)
CFEB_FIFO_FULL(5)	=1, if corresponding CFEB INPUT FIFO on the DMB is full (bad! – re-sync will be required) <i>Note: it takes ~20 events to fill up INPUT FIFOs (CFEBs with 8-sample readout, ALCT, TMB)</i> <i>Note: FIFO Status bits correspond to the moment when this particular word is being transmitted.</i>
h ALCT_START_TIMEOUT	=1, if the start of ALCT data was not detected within the start time-out periods
i TMB_START_TIMEOUT	=1, if the start of TMB data was not detected within the start time-out periods
CFEB_STARTTIMEOUT(5)	=1, if CFEB(i) did not start sending data within the start time-out period.
j ALCT_END_TIMEOUT	=1, if the end of ALCT data was not detected within the end time-out periods (bad! – re-sync will be required)
k TMB_END_TIMEOUT	=1, if the end of TMB data was not detected within the end time-out periods (bad! – re-sync will be required)
CFEB_ENDTIMEOUT(5)	=1, if CFEB(i) did not finish sending data within end time-out period (bad! – re-sync will be required) <i>Note: Start/End time-out periods are the same for all boards</i>
CRC(0:11), CRC(12-22)	CRC bits for DMB data
n CRC_PARITY1	=1/0 if sum of CRC(0:11) bits is odd/even
o CRC_PARITY2	=1/0 if sum of CRC(0:11) bits is odd/even

⁴ In principle tunable, but should never be wider than ± 1 BX

FIFO FULL status:

- (a) some data may be lost,
- (b) FIFO FULL condition breaks synchronization in assembling CSC event: even if FIFO FULL condition goes away, CFEB, ALCT, TMB data from different events may continue to be mixed up together...

One must reset DMB and its FEBs (~1 μ s Sync Reset or ~15 ms Hard Reset?)

FIFO FULL bits *must* persist until the board is reset. Is it implemented already?

TIMEOUT status

Indicates a serious readout problem; DMB-FEBs may need to be resynchronized. These bits may need to be made persistent as well. Is it implemented already?

Rev 6 Changes and References:

- Many changes in DMB Header and Trailer bits (per J. Gu's e-mails from Aug 25, 2005)
- New bits, missing in earlier firmware versions, are now present

Rev 5 Changes and References:

- As of May 6, 2004 Firmware revision, DMB input CFEB_FIFO_FULL and ALCT_FIFO_FULL conditions are tagged by setting corresponding bits to be 0---not 1, as described in the earlier documentation versions (per J. Gu's e-mails from June 14, 2005).

Rev 4 Changes and References:

- As of September 2004, 16-bit words in LoneWord and Header1 are reordered and Header1 is no longer suppressed by the DDU (per J. Gu's e-mails from September XX, 2004).

Rev 3 Changes and References:

- Correction: bit9 in the first A-Header word is not what it was described to be (ACTIVE_DAV_Mismatch). J. Gu confirms in e-mails from June XX, 2004 that this bit currently just repeats TMB DAV.

Rev 2 Changes and References:

- DMB format modifications: Trailer 2 and Trailer 5 bits redefined (J. Gu e-mails from May 28, 2004)
- J. Gu's comments on the previous draft are incorporated (comments received May 18, 2004)

Rev 1 References:

- More recent updates (private communications with J. Gu., S. Durkin, J. Gilmore, April 2004)
- <http://www.physics.ohio-state.edu/~cms/ddu/ddu.html> (last updated 1 May 2003)
- http://www.physics.ohio-state.edu/~cms/dmb/dataformat_ddu.html (last updated 16 Jan 2003)

APPENDIX 1: DMB-2004 DATA FORMAT (September 2004 – August 2005)

Note: In comparison to the previous format, words in Header 1 and LoneWord are reordered and Header 1 is no longer suppressed by DDU.

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
DMB lone word	8	1	0	0	0	DMB_LA1(11:0)												
		1	0	0	0	DMB_LA1(23:12)												
		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	0	0	0	DMB_BXN(11:0)												

this DMB lone word will be suppressed by DDU

Fig. 1. If no data are available for a given L1A (neither of 5 CFEBs nor ALCT nor TMB reported DAV signal within 3-BX window around L1A signal), DMB sends a so-called lone word (actually, four 16-bit words).

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Header 1	9	1	0	0	1	DMB_LA1(11:0)														
		1	0	0	1	DMB_LA1(23:12)														
		1	0	0	1	a	b	CFEB_ACTIVE(5)					CFEB_DAV(5)							
		1	0	0	1	DMB_BXN(11:0)														
Header 2	A	1	0	1	0	a	b	c	a	b	a	b	CFEB_DAV(5)							
		1	0	1	0	DMB_CRATE(8)								DMB_ID(4)						
		1	0	1	0	CFEB_MOVL(5)					DMB_BXN(7)									
		1	0	1	0	DMB-CFEB_Sync(4)				DMB_L1A(8)										
ALCT data Trailer	D	0	ALCT data																	
		1	1	0	1	0	22-bit CRC (lowest 11 bits)													
		1	1	0	1	0	22-bit CRC (lowest 11 bits)													
		1	1	0	1	1	1	1	0	0	0	0	0	0	1	1	0	1		
		1	1	0	1	0	0	10-bit ALCT word count (# of 16-bit frames)												
TMB data Trailer	D	0	TMB data (includes CLCT)																	
		1	1	0	1	1	22-bit CRC (lowest 11 bits)													
		1	1	0	1	1	22-bit CRC (lowest 11 bits)													
		1	1	0	1	1	1	1	0	0	0	0	0	1	1	1	1			
		1	1	0	1	1	11-bit TMB word count (# of 16-bit frames)													
Trailer 1	F	0/1	CFEB data																	
		1	1	1	1	a	b	CFEB_ACTIVE(5)					CFEB_DAV(5)							
		1	1	1	1	CFEB_MOVL(5)					d	e	CFEB_HALF(5)							
		1	1	1	1	DMB_L1_PIPE(8)								DMB_BXN(4)						
		1	1	1	1	DMB_CRATE(8)								DMB_ID(4)						
Trailer 2	E	1	1	1	0	f	CFEB_FULL(5)					g	CFEB_MT(5)							
		1	1	1	0	h	CFEB_ENDTIMEOUT(5)					i	CFEB_STARTTIMEOUT(5)							
		1	1	1	0															
		1	1	1	0															

hex D.E0D

hex D.E0F

repeat word 9a

repeat previous word

repeat previous word

Fig. 2. If data are available for a given L1A (at least one of CFEBs or ALCT or TMB reported DAV signal within 3-BX window around L1A signal), DMB waits certain time to collect data and then sends the data in this format. The TMB and ALCT trailers shown in Fig.2 are actually a part of TMB and ALCT data format and generated by TMB/ALCT boards—DMB does not touch them.

B-WORDS

Normally, data blocks have bit 15 = 0. However, words with B-signature (bits 12-15 = 1011) can appear in CFEB data block. They are intended to signal problems with CFEB data (see the note on CFEB data format for details).

C-WORDS

Words with C-signature (bits 12-15 = 1100) are not used.

APPENDIX 2: DMB-2003 DATA FORMAT (prior to September 2004)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMB lone word	8	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	0	0	0	DMB_LA1(11:0)											
		1	0	0	0	DMB_LA1(23:12)											
		1	0	0	0	DMB_BXN(11:0)											

this DMB lone word will be suppressed by DDU

Fig. 1. If no data are available for a given L1A (neither of 5 CFEBs nor ALCT nor TMB reported DAV signal within 3-BX window around L1A signal), DMB sends a so-called lone word (actually, four 16-bit words).

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Header 1	9	1	0	0	1	a	b	CFEB_ACTIVE(5)					CFEB_DAV(5)							
		1	0	0	1	DMB_LA1(11:0)														
		1	0	0	1	DMB_LA1(23:12)														
		1	0	0	1	DMB_BXN(11:0)														
Header 2	A	1	0	1	0	a	b	c	a	b	a	b	CFEB_DAV(5)							
		1	0	1	0	DMB_CRATE(8)								DMB_ID(4)						
		1	0	1	0	CFEB_MOVL(5)					DMB_BXN(7)									
		1	0	1	0	DMB-CFEB_Sync(4)				DMB_L1A(8)										
ALCT data Trailer	D	0	ALCT data																	
		1	1	0	1	0	22-bit CRC (lowest 11 bits)													
		1	1	0	1	0	22-bit CRC (lowest 11 bits)													
		1	1	0	1	1	1	1	0	0	0	0	0	0	1	1	0	1		
		1	1	0	1	0	0	10-bit ALCT word count (# of 16-bit frames)												
TMB data Trailer	D	0	TMB data (includes CLCT)																	
		1	1	0	1	1	22-bit CRC (lowest 11 bits)													
		1	1	0	1	1	22-bit CRC (lowest 11 bits)													
		1	1	0	1	1	1	1	0	0	0	0	0	1	1	1	1			
		1	1	0	1	1	11-bit TMB word count (# of 16-bit frames)													
Trailer 1	F	0/1	CFEB data																	
		1	1	1	1	a	b	CFEB_ACTIVE(5)					CFEB_DAV(5)							
		1	1	1	1	CFEB_MOVL(5)					d	e	CFEB_HALF(5)							
		1	1	1	1	DMB_L1_PIPE(8)								DMB_BXN(4)						
		1	1	1	1	DMB_CRATE(8)								DMB_ID(4)						
Trailer 2	E	1	1	1	0	f	CFEB_FULL(5)					g	CFEB_MT(5)							
		1	1	1	0	h	CFEB_ENDTIMEOUT(5)					i	CFEB_STARTTIMEOUT(5)							
		1	1	1	0	repeat previous word														
		1	1	1	0	repeat previous word														

hex D.E0D

hex D.E0F

repeat word 9a

Fig. 2. If data are available for a given L1A (at least one of CFEBs or ALCT or TMB reported DAV signal within 3-BX window around L1A signal), DMB waits certain time to collect data and then sends the data in this format. The TMB and ALCT trailers shown in Fig.2 are actually a part of TMB and ALCT data format and generated by TMB/ALCT boards—DMB does not touch them.

B-WORDS

Normally, data blocks have bit 15 = 0. However, words with B-signature (bits 12-15 = 1011) can appear in CFEB data block. They are intended to signal problems with CFEB data (see the note on CFEB data format for details).

C-WORDS

Words with C-signature (bits 12-15 = 1100) are not used.

APPENDIX 3: DMB-2004 and DMB-2003 DATA FORMAT COMMENTS

a	TMB_DAV	=1, if TMB data exists for this event, i.e. there was a DAV signal from TMB matching current L1A.
b	ALCT_DAV	=1, if ALCT data exists for this event (same as above, but for ALCT)
	CFEB_DAV(5)=xxxxx	tags CFEBs that will send data to DMB (same as above, but for CFEBs)
	CFEB_ACTIVE(5)=zzzzz	CFEBs that should send data as judged by the TMB board: CLCT(s) was (were) found and matched L1A within ± 1 BXs window ⁵
c	= a	Earlier intended to be ACTIVE-DAV-Mismatch , but in reality this has never been implemented....
	DMB_L1A(varies)	L1A Event Number (redundant copies from the same DMB counter)
	DMB_BXN(varies)	Bunch Crossing Number corresponding to L1A (redundant copies from the same DMB counter)
	DMB_CRATE(8)	peripheral crate ID from DMB (mapping to actual sectors/stations is not yet set)
	DMB_ID(4)	position of DMB in the crate = (slot number in the crate)/2; allowed values: 1, 2, 3, 4, 5, -, 7, 8, 9, 10
	DMB-CFEB-Sync(4)	4-bit counter of BXs from last SyncReset to L1A. Can be used to check DMB-CFEB synchronization: The least significant bit of TRIG_TIME(8) + L1A_phase(1) on CFEBs make similar 4-bit counters (albeit for some constant offset, e.g. due to various cable lengths)
	DMB_L1PIPE(8)	number of L1As backed-up in the DMB (yet to be send to DDU, not counting the one being sent now) <i>Note: expect to be 0 at low rates</i> <i>Note: the data waiting to be sent to DDU are backed up in the INPUT FIFOs</i> <i>Note: It takes ~20 events to fill up INPUT FIFOs; so 8-bit counter appears to be much too deep.</i> <i>However, at LHC we expect only 5% of chambers reporting DAV signals per L1A. Therefore, INPUT FIFOs can absorb as many ~400 L1As before getting full—it is this number that drives the 8-bit depth of the L1PIPE counter.</i>
	CFEB_MOVL(5)=xxxxx	some time sample for this event would have multiple (>2) overlaps with samples from previous events: CFEB data for this event are NOT sent at all CFEB_DAV signal is NOT sent either <i>Note: CFEB_MOVL=1 can be only in events with CFEB_DAV=0 for this board</i> <i>Note: Due to the CMS trigger rule of no more than two L1A signals within 625 ns, CFEB_MOVL=1 can occur at LHC only for 16-sample CFEB readout mode (see the note on CFEB data format).</i>
	CFEB_HALF(5)	=0, if CFEB INPUT FIFO on the DMB is more than HALF FULL (warning)
d	ALCT_HALF	=0, if ALCT INPUT FIFO is more than HALF FULL (warning)
e	TMB_HALF	=0, if TMB INPUT FIFO is more than HALF FULL (warning)
	CFEB_FULL(5)	=0, if corresponding CFEB INPUT FIFO on the DMB is full (bad! – re-sync will be required)
f	ALCT_FULL	=0, if ALCT INPUT FIFO on the DMB is full (bad! – re-sync will be required) <i>Note: it takes ~20 events to fill up INPUT FIFOs (CFEBs with 8-sample readout, ALCT, TMB)</i>
	CFEB_MT(5)	=1, if CFEB INPUT FIFO on the DMB is empty (OK)
g	ALCT_MT	=1, if ALCT INPUT FIFO on the DMB is empty (OK) <i>Note: No events beyond the one being read out—being empty is OK; one must expect 1 at low rates.</i> <i>Note: FIFO Status bits correspond to the moment when this particular word is being transmitted.</i>
	CFEB_STARTTIMEOUT(5)	=1, if CFEB(i) did not start sending data within the start time-out period.
	CFEB_ENDTIMEOUT(5)	=1, if CFEB(i) did not finish sending data within end time-out period
h	ALCT_TIMEOUT	=1, if the start and/or end of ALCT data was not detected within the start/end time-out periods
i	TMB_TIMEOUT	=1, if the start and/or end of TMB data was not detected within the start/end time-out periods <i>Note: Start/End time-out periods are the same for all boards</i> <i>Note: In future, TMB and ALCT TIMEOUTs will be split into START and END TIMEOUTs</i>

FIFO FULL status:

- (a) some data may be lost,
 (b) FIFO FULL condition breaks synchronization in assembling CSC event: even if FIFO FULL condition goes away, CFEB, ALCT, TMB data from different events may continue to be mixed up together...
 One must reset DMB and its FEBs (~1 μ s Sync Reset or ~15 ms Hard Reset?)
FIFO FULL bits must persist until the board is reset. Not implemented at the moment—to be fixed in future.

TMB FULL and TMB MT: These bits fell between cracks; hopefully, the next format revision will have it fixed**TIMEOUT status**

Indicates a serious readout problem; DMB-FEBs may need to be resynchronized. These bits may need to be made persistent as well.

⁵ In principle tunable, but should never be wider than ± 1 BX