

JTAG ERROR

A basic JTAG communications tests. EPROM and Virtex chips are placed in bypass mode. Bits are shifted through and checked that they come back to the computer unchanged.

Quick Fixes

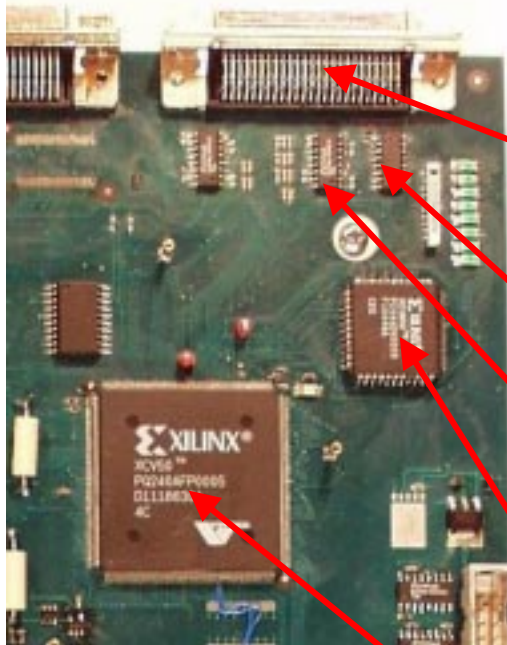
1. Check power is on.
2. Check cabling.

ERROR File

Readback file gives bits shifted down and bits returned

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JTAG  
expect 0x806a1500 ← shifted down  
got    0x806a1500 ← received back
```

Scope Debugging



FEB->Motherboard Connector
TMS - pin 13 TDI - pin 15 TCK- pin 17 TDO- pin 19
TMS + pin 14 TDI + pin 16 TCK+ pin 18 TDO+ pin 20

TTL-> LVDS TDO+ pin 10
 TDO - pin 11
 TDO pin 9

LVDS->TTL
TCK + pin 2 TMS+ pin 14 TDI + pin 6
TCK - pin 1 TMS- pin 15 TDI- pin 7
TCK pin 3 TMS pin 13 TDI pin 5

EPROM
TDI pin 9 TDO pin 37 TMS pin 11 TCK pin 13

VIRTEX
TDI pin 183 TMS pin 2 TDO pin 181 TCK pin 240

- 1) Check signals after LVDS->TTL converters.

- 2) Check signals into the EPROM
- 3) Check signals into the Virtex
- 4) Check signals into the TTL->LVDS converters.