

## **Graphite based Schottky diodes on Si, GaAs, and 4H-SiC**

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This article demonstrates the formation of Schottky diodes on silicon (Si), gallium arsenide (GaAs), and 4H-silicon carbide (4H-SiC) using the semimetal graphite. The forward bias characteristics follow thermionic emission theory, and the extracted Schottky barrier heights closely follow the Schottky-Mott relation. Due to the properties of graphite and Schottky junctions, the graphite/semiconductor junction is a good predictor of a graphene/semiconductor junction. Also, the graphite/semiconductor Schottky diode is extremely applicable to high power, frequency, and temperature devices.

### **Introduction**

In Dr. Hebard's lab, we formed Schottky junctions on three major industry semiconductors, Si, GaAs, and SiC, using graphite instead of the traditional metal. Graphite offers several advantages, namely that the Schottky junction should be valid at higher temperatures without the graphite diffusing into the semiconductor. Also, by doping the graphite, we can change the Fermi energy and thus change the barrier height, which is not possible with a conventional metal. The height of the graphite/semiconductor Schottky barrier could be changed based solely on the doping level of the graphite instead of the specific metal/semiconductor combination. Additionally, the Fermi level of graphite is very low and at high temperatures, its electrons act as a Boltzmann gas and offer a variety of physical effects.

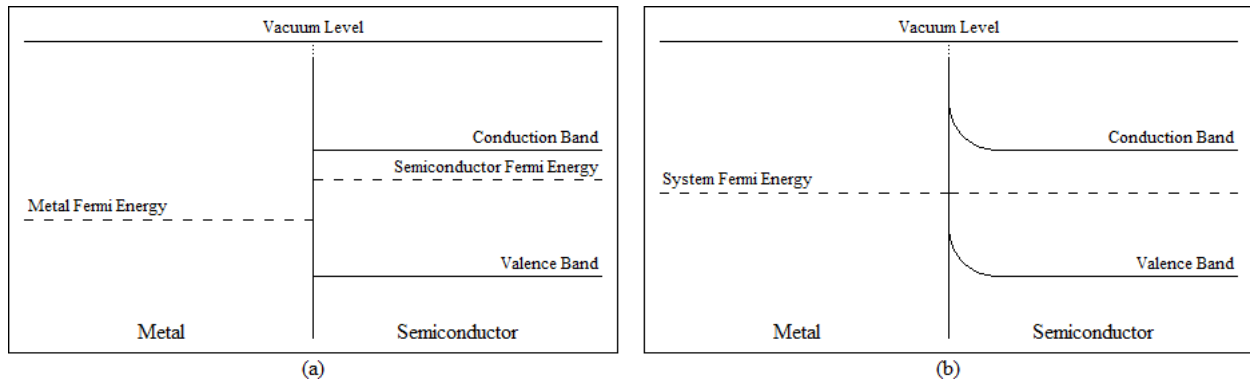
We demonstrate through both I-V and C-V measurements that the graphite/semiconductor junction forms a Schottky barrier and that the barrier is robust at high voltages. The three semiconductors used were chosen because they have technological applications in today's computing industry. Silicon is used in essentially every computer chip, not only in personal computers, but also in most commercially available electronic devices. Gallium Arsenide is famed for its durability at higher temperatures, being more applicable to the space industry where the operating temperature range needs to be much greater. On the same note, Silicon Carbide commands a large sector of research for applications in high power, frequency, and temperature devices.

A Schottky barrier is first and foremost a diode. In fact, it offers several advantages over the traditional PN diode. The Schottky diode dissipates a smaller voltage in the forward bias direction which directly leads to a higher efficiency. Also, the Schottky diode does not require the large "cool down" or relaxation time to resettle the minority carriers as required by the PN diode. The absence of this delay makes the Schottky diode much more effective in today's industry where the goal is to go as fast as possible.

This research also offers a look into the realm of graphene. Graphene is being studied as a possible high power substrate upon which circuit boards can be built. Based on the properties of graphite and Schottky barriers, the Schottky junctions formed by graphite/semiconductor junctions should be very similar to graphene/semiconductor junctions.

## Background and Theory

A Schottky is typically formed by putting a metal in contact with an n-doped semiconductor. If the Fermi energies of the two materials differ, the system must reach a constant Fermi energy across the metal/semiconductor junction to be in thermal equilibrium. To do this, electrons from the semiconductor will diffuse into the metal to lower their energies. This diffusion leaves behind positively charged donor atoms on the semiconductor side of the junction. On the metal side, the excess electrons have a high mobility and are therefore able to disperse throughout the metal, causing no barrier formation. The positively charged donor atoms in the semiconductor cause an upwards shift in both the conduction band and valence band of the semiconductor. Electrons passing through that area will need more energy to pass the positive charges that want to hold them. Figure 1 demonstrates the energy band structure of the system prior to diffusion of electrons into the metal and the resulting band structure after the electrons have diffused.

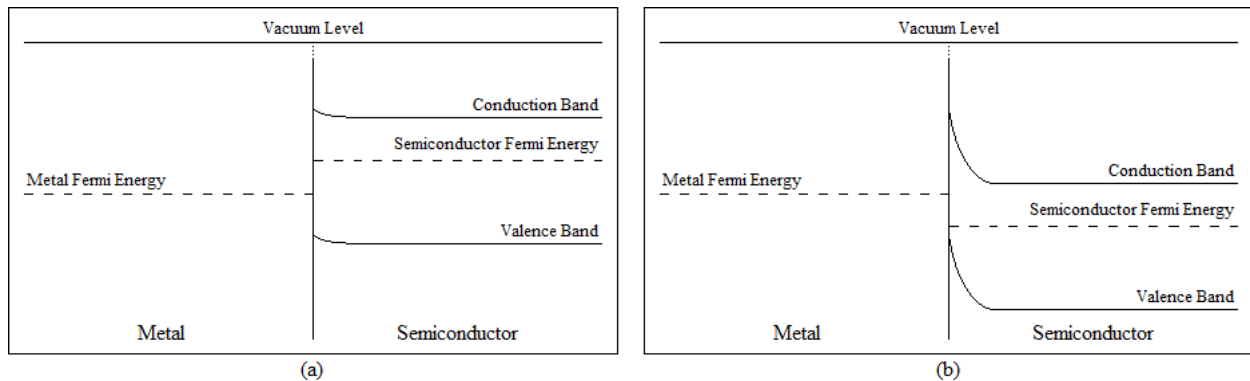


**Figure 1** (a) Band structure prior to contact between metal and semiconductor (b) Band structure after contact between metal and semiconductor

The result of this barrier is a diode effect, appropriately named the Schottky diode. When an electric potential is applied across this barrier, the dynamic resistance of the junction will increase or decrease based on the direction in which the potential is applied. If the semiconductor is positively, or reverse, biased, the Fermi energy of the semiconductor will drop, along with the conduction and

valence bands. Since a metal can be seen as a “vast sea of electrons,” its Fermi energy is fixed. Therefore, the energy that the electrons would need to pass over the barrier is greatly increased. The result is that current does not pass from the semiconductor to the metal (electrons will not pass from the metal to the semiconductor).

When a negative, or forward, bias is applied to the semiconductor, the Fermi energy of the semiconductor will increase along with the conduction and valence bands. This causes the energy that the electrons need to overcome the barrier to decrease drastically, again because the Fermi energy of the metal is fixed. Therefore, current will flow easily from the metal to the semiconductor. Figure 2 displays the change in the band structure of the Schottky junction under forward and reverse biases.



**Figure 2** (a) Band structure with a forward bias (b) Band structure with a reverse bias

This behavior is typical of a diode: current will flow in one direction, but not the other. However, this diode would be useless if it were not possible to create a non-Schottky junction between a metal and a semiconductor. Back-to-back Schottky barriers would hinder the flow of electrons in both directions and offer no rectifying behavior in the relationship between current and voltage. The solution to this is an ohmic contact, named for its ohmic nature. An ohmic contact is a layer of metal, or several metals, which does not accept electrons from the semiconductor. Metals with

work functions similar to the electron affinity of the semiconductor usually are less willing to accept electrons from the semiconductor and are therefore chosen to be the contact metal for ohmic contacts. A metal which does not oxidize is then deposited on top of the contact layer to prevent any unwanted interactions with the atmosphere. After the metal deposition, the entire contact is annealed to a high temperature to allow the contact metal to partially diffuse into the semiconductor, creating the low resistance aspect of the contact. The result is a junction which does not rectify, but instead obeys Ohm's Law.

The electron transport process of Schottky barriers is mainly dominated by thermionic emission: electrons will only overcome the barrier if they have sufficient energy. Thermionic emission involves no tunneling or other similar shortcuts around the barrier. This process can be described by a modified form of Richardson's equation for general thermionic emission:

$$I = I_s \left[ \exp\left(\frac{qV}{\eta k_b T}\right) - 1 \right] \quad (1)$$

where  $I_s = AA^*T^2 \exp\left(\frac{-q\phi_b}{k_b T}\right)$  is the saturation current density,  $q\phi_b$  is the Schottky barrier height,  $A^*$  is the Richardson constant,  $T$  is the absolute temperature in Kelvin, and  $V$  is the applied voltage across the junction. With forward biases greater than  $3k_b T/q$ , the trailing 1 in equation (1) can be neglected and Richardson's equation becomes a pure exponential of the form:

$$I = I_s \exp\left(\frac{qV}{\eta k_b T}\right) \quad (2)$$

Linearity in the semi-logarithmic plot of current versus voltage is strong evidence that the Schottky junction is obeying thermionic emission. Furthermore,  $I_s$  can be extracted by fitting the linear section of the semi-logarithmic plot and extending the fit to zero voltage. Once  $I_s$  is known,

the Schottky barrier height can be extracted, independent of contact area, by dividing by  $T^2$  and taking the natural logarithm of both sides:

$$\ln\left(\frac{I_s}{T^2}\right) = \ln(AA^*) - \left(\frac{q\phi_b}{k_b T}\right) \quad (3)$$

By taking I-V curves at different temperatures where thermionic emission is the dominant transport process,  $\phi_b$  can be extracted from the slope of a linear fit to a semi-logarithmic plot of  $\frac{I_s}{T^2}$  versus  $\frac{1}{T}$  since  $q$  and  $k_b$  are known. This process is useful if the area of the Schottky junction is not known or if other factors may affect the effective area of the contact.

A similar method can be used to extract the Schottky barrier height from capacitance versus voltage data in the reverse bias direction. The junction capacitance can be calculated by the same equation as that for a PN junction:

$$C' = \left[ \frac{e\epsilon_s N_d}{2(V_{bi} + V_R)} \right]^{1/2} \quad (4)$$

where  $C'$  is the capacitance per unit area,  $N_d$  is the doping density of the semiconductor,  $\epsilon_s$  is the permittivity of the semiconductor,  $V_{bi}$  is the built-in potential barrier, and  $V_R$  is the reverse bias voltage. Using algebraic manipulation, this equation becomes:

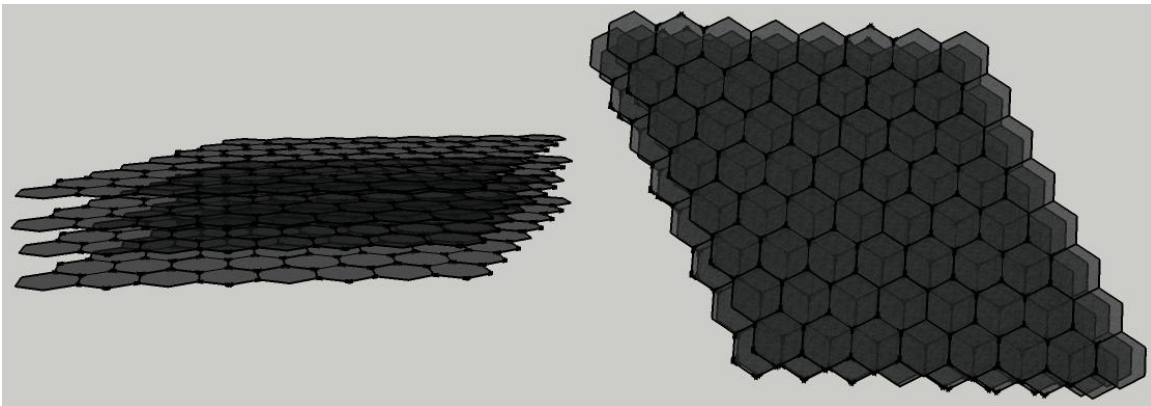
$$\left(\frac{1}{C'}\right)^2 = \frac{2(V_{bi} + V_R)}{e\epsilon_s N_d} = \frac{2V_{bi}}{e\epsilon_s N_d} + \frac{2V_R}{e\epsilon_s N_d} \quad (5)$$

By plotting  $\left(\frac{1}{C'}\right)^2$  as a function of  $V_R$ , both the doping density,  $N_d$ , and the built-in potential barrier,  $V_{bi}$ , can be extracted from the slope and the intercept respectively. The Schottky barrier height can be extracted from the built-in potential barrier by the following relationship:

$$V_{bi} = \phi_b - \phi_n \quad (6)$$

in which  $\varphi_n$  is the difference between the conduction band and the Fermi energy of the semiconductor. These two methods can be used to verify the Schottky barrier height for any particular Schottky junction [1].

Graphite is a semimetal consisting of three very strong double carbon-carbon bonds per atom. These bonds form by  $sp^2$  hybridization and the carbon atoms align themselves into a single layer of carbon (graphene) in which the bonds between carbon atoms form hexagons, three bonds per carbon atom. These graphene layers are “stacked” on top of each other with a shift such that half of the carbon atoms in one layer are directly above the center of the hexagon of carbon below it as shown in Figure 3. Since carbon has a small Bohr radius and the carbon atoms are double bonded to each other, a sheet of graphene has the highest tensile strength of all known materials [2]. Also, these bonds cause graphite to have an extremely high melting temperature of  $3550^\circ\text{C}$ , making it applicable to high temperature devices.



**Figure 3** Side and top-down views of layered graphite

Being a semimetal means that graphite has both electrons and holes as electrical carriers. The concentrations of each of these carriers are less than those of metals, but higher than those of intrinsic semiconductors. As a result, the conduction band and valence band of graphite overlap.

This overlap causes the electrical properties of graphite to be partially metallic and partially like a semiconductor.

The Fermi energy of graphite is very low, 25 meV compared to the 5 eV of gold. This allows the electrons of graphite to act as a Boltzmann gas at higher temperatures. When the energy associated with a specific temperature becomes greater than the Fermi energy of the graphite, the electrons follow the ideal gas law. Therefore, not only is a Schottky junction between graphite and a semiconductor at high temperatures technologically applicable, but it is also physically interesting [3].

Since graphite consists of stacked layers of graphene, the contact surface on both the top and bottom of a piece of graphite (oriented with the C axis on the Z plane) will be a single layer of graphene. Bond polarization theory implies that only this single layer of graphene will interact with the semiconductor and form the Schottky barrier. Also, the bonding between planes of graphene is small and easily overcome ( $\sim 0.3$  eV) at higher temperatures [4]. Therefore, the first layer of graphene only interacts with the single layer of graphene above it. These two facts suggest that graphite will predict the behavior of graphene in Schottky junction applications.

Graphite and graphene are being enthusiastically researched for applications in electronics by today's leading computer hardware companies. A graphene sheet would provide a highly conductive surface that could be etched using photoresist. This technology could then be used to create the traditional two-dimensional circuit boards, but more interestingly, could lay the foundation for three-dimensional devices. Computer chips could start extending into the third dimension and not be limited by the two-dimensional surface they must sit on.



## Procedures

In Dr. Hebard's lab, I worked in conjunction with Sefaattin Tongay to create Schottky barriers using the semimetal graphite instead of the traditional metal. Graphite, which has a low Fermi energy and relatively few free carriers per atom, was an ideal candidate for a Schottky contact "metal." We limited the tested semiconductors to those which were already in development or being researched for practical applications: silicon (Si), gallium arsenide (GaAs), and silicon carbide (SiC). The graphite contacts caused very little damage to the surface of the semiconductors due to the weak Van der Waals forces as well as the high impenetrability of the graphene sheets.

The graphite used was highly oriented pyrolytic graphite (HOPG) and acted as the metal in the Schottky junction with the three semiconductors. The Schottky junctions were formed in three different ways: physically pressing bulk HOPG to the surface of the semiconductor, Van der Waals adherence of cleaved HOPG flakes, and "painting" graphite contacts. The first contact method was accomplished by gently clamping a relatively large ( $\sim 1 \text{ mm}^2$ ) piece of HOPG to the surface of the semiconductor. To perform the cleaving technique, we cut  $0.5^\circ$  FWHM bulk HOPG and allowed the resulting flakes to fall on the semiconductor surface. Occasionally, a relatively large flake ( $\sim 0.5 \text{ mm}^2$ ) would stick to the semiconductor via Van der Waals attraction. The rest of the graphite flakes were collected and sonicated in residue-free 2-butoxyethyl acetate and octyl acetate. We applied this "paint" to the surface of the semiconductors and allowed it to air dry to form the third contacts. The three contact methods showed similar electrical results when measured, so we used the painting method exclusively after the initial tests, due to the relative ease of fabrication. Similarly, x-ray diffraction testing (XRD) yielded similar results between all three contact methods.

The silicon samples were doped with  $3 \times 10^{15} \text{ cm}^{-3}$  phosphorus. They were initially cleaned using buffer hydrofluoric acid to remove any native oxide on the surface. To create the ohmic contact, we

deposited 1500 Å of aluminum followed directly by 150 Å of titanium to prevent the aluminum from oxidizing. The ohmic contact was then annealed to 590°C for 3 minutes using rapid thermal annealing to ensure non-rectifying behavior [5].

The gallium arsenide samples were doped with  $3 \times 10^{16} \text{ cm}^{-3}$  silicon. They were initially cleaned using 3:1:50 HNO<sub>3</sub>:HF:H<sub>2</sub>O. We then deposited 100 Å of palladium, 250 Å of germanium, and 2500 Å of gold without exposing the sample to atmosphere. Using rapid thermal annealing, we annealed the samples to 460°C for 1 minute [6].

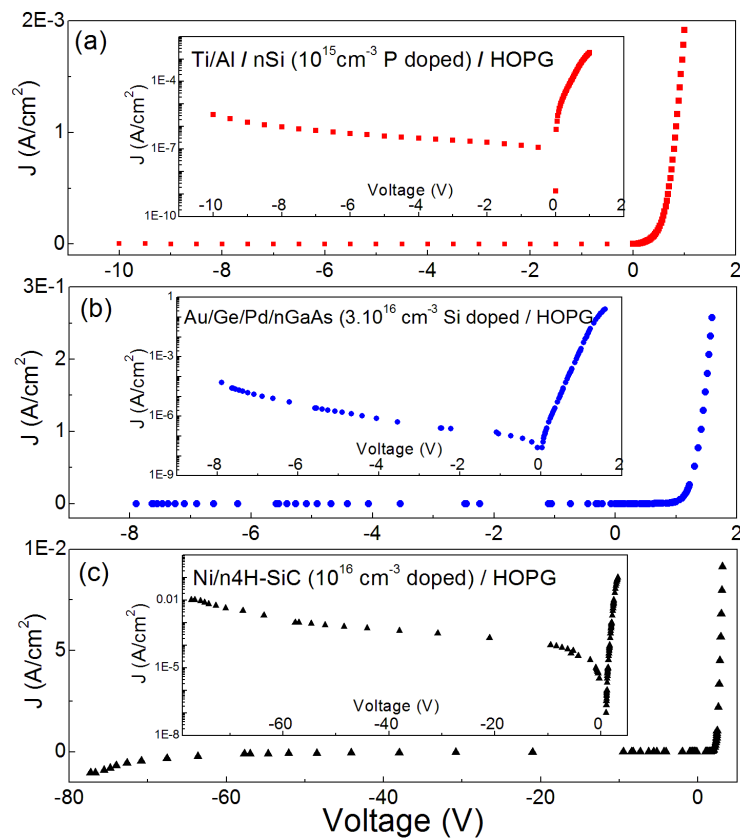
The silicon carbide samples consisted of a 5 μm epilayer of 4H-SiC doped with  $3 \times 10^{15} \text{ cm}^{-3}$  aluminum on top of insulating 4H-SiC. These samples were cleaned using acetone and isopropyl alcohol. The ohmic contact consisted of 1000 Å of nickel on the surface of the SiC. The ohmic contact was then annealed to 1000°C for 5-7 minutes using rapid thermal annealing to ensure ohmic behavior [7].

Initially, we roughly measured voltage with respect to current in both the forward and reverse bias directions to verify that the Schottky contact was indeed rectifying. Once we observed the rectification, we measured voltage with respect to current in both forward and reverse bias over seven decades of current. We measured at every 10K from 330K to 250K (to show thermionic emission) and every 50K down to 20K where the ohmic contact was no longer valid. These measurements were used to extract the Schottky barrier heights of the contacts.

To verify the Schottky barrier heights, we also measured capacitance versus voltage in the reverse bias direction. Then using the method described in the background section, we extracted the Schottky barrier height from these data.

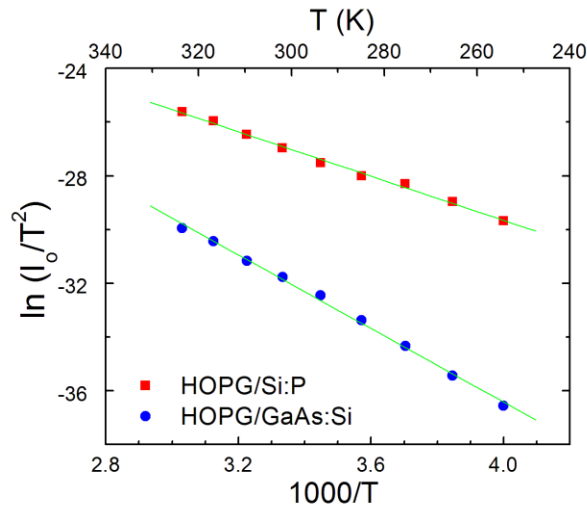
## Results

First and foremost, each method of graphite deposition formed a Schottky barrier of similar height on each of the three semiconductors tested. Additionally, each of the Schottky barriers exhibited a high degree of rectification, with the graphite/silicon carbide junction extending to our maximum measuring capability before showing any signs of breaking down. Figure 4 displays both the linear and semi-logarithmic relationship between voltage and current density for the graphite Schottky junction on each semiconductor.



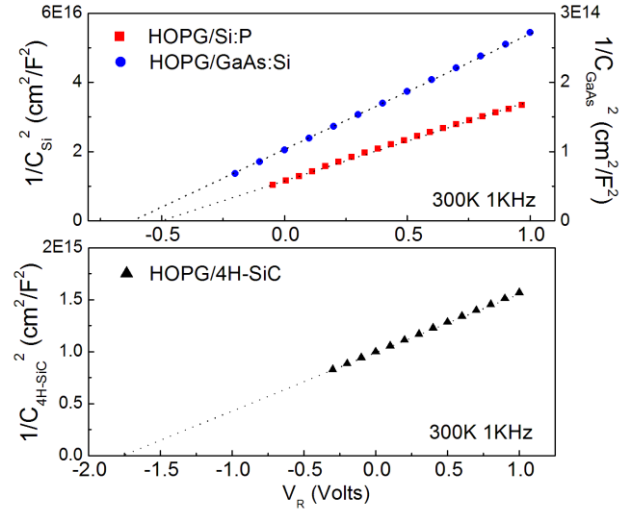
**Figure 4** Linear current versus voltage plots with semi-logarithmic plots as the insets

We used the linear portions of the forward bias of the semi-logarithmic plots to extract the saturation current density. Then, using the modified Richardson equation, we extracted the Schottky barrier heights for the individual graphite/semiconductor Schottky junctions. Figure 5 shows the  $\ln\left(\frac{J_s}{T^2}\right)$  versus  $1000/T$  plots used to extract the Schottky barrier heights, and Table 1 shows the extracted Schottky barrier height values.



**Figure 5** Plots used to extract Schottky barrier heights

We then measured capacitance versus voltage in the reverse bias direction to verify the Schottky barrier heights. The intercept of a linear line fitted to  $1/C^2$  vs.  $V_{\text{reverse}}$  data contains the Schottky barrier height for the Schottky junction. Figure 6 shows the  $1/C^2$  vs.  $V_{\text{reverse}}$  plots, and Table 1 shows the extracted Schottky barrier heights.



**Figure 6** Capacitance-voltage plots used to extract Schottky barrier heights

Using the plots in Figure 6, the carrier densities of the semiconductors were extracted. This verified that the C-V measurements were valid. Table 1 shows these extracted carrier densities and the reported carrier densities for each semiconductor. In addition, Table 1 shows the work function of the graphite point,  $\chi_{\text{graphite}}$ , extracted from the Schottky Mott relation ( $\phi_b = \phi_s - \chi_{\text{graphite}}$ ).

junction type	$\phi_{I-V}$ [eV]	$\phi_{C-V}$ [eV]	$N_D^{C-V}$ [ $\text{cm}^{-3}$ ]	$N_D^{Hall}$ [ $\text{cm}^{-3}$ ]	$\phi_{\text{graphite}}$ [eV]
HOPG/ <i>n</i> Si	0.40	0.70	$1.2 \times 10^{15}$	$1.0 \times 10^{15}$	4.40
HOPG/ <i>n</i> GaAs	0.60	0.76	$3.6 \times 10^{16}$	$3.0 \times 10^{16}$	4.60
HOPG/ <i>n</i> 4H-SiC	1.15	1.84	$1.2 \times 10^{16}$	$1.0 \times 10^{16}$	4.45

**Table 1** Extracted Schottky barrier heights from I-V and C-V measurements, extracted and reported doping densities, and corresponding work function of graphite

## Discussion

The linearity in the forward bias of the semi-logarithmic current versus voltage data implies that the junction follows the thermionic emission theory. The non-linearity at lower voltages can be attributed to a secondary transport process (i.e. space-charge limited emission) becoming more dominant. The non-linearity at higher voltages can be attributed to the series resistance of the semiconductor. Furthermore, the data exhibit a rectified current voltage relationship down to 20 K where the validity of the ohmic contacts became questionable.

The capacitance versus reverse bias plots consistently produced a Schottky barrier height greater than that of the current versus voltage plots. However, the doping densities strongly agree with the reported values for the semiconductors. This deviation may have been caused by a thin layer of oxide on the surface of the semiconductor prior to the application of the metals and graphite. The oxide layer would create a small additional capacitance, shifting the actual C-V relation slightly lower due to the series capacitance without changing the shape of the relation. This shift corresponds to a higher extracted Schottky barrier height and an accurate doping density based on the intercept and the slope of the linear fit respectively. Although the semiconductors were cleaned, without creating samples in a clean room which is evacuated of oxygen, samples without a small oxide layer would be impractical to make.

Using the Schottky barrier heights extracted from the I-V measurements, we calculated the work function of the graphite paint with the Schottky Mott relation and the known electron affinity of the three semiconductors. Not only did the work functions of the graphite paint match between all three semiconductors, but the calculated work function of the paint also matched the literature values for the work function of HOPG (4.4 – 4.8 eV) [8-10]. These values can be found in Table 1.

## Applications

Unlike most metals, graphite forms a Schottky barrier on a wide variety of semiconductors. This unique characteristic makes the graphite/semiconductor Schottky barrier extremely robust in the realm of electronics. Additionally, the three semiconductors we used have many applications in technology or are being extensively researched for application purposes.

Silicon is used almost exclusively in any commercially available electronic devices (personal computers, automobiles, PDAs, etc.). Gallium Arsenide is used by NASA in devices designed for space where the operating temperature range is much greater than Earth's operating temperature range. Silicon Carbide is being studied as a solution for high power and high frequency devices due to its extreme resistance to heat.

Graphite itself offers many advantages compared to traditional metals. Due to the extremely strong bonds between carbon atoms and the relatively small atomic size of carbon, graphite should not diffuse into the semiconductor at high temperatures and should therefore retain the rectification of the Schottky barrier. Also, graphite can be doped with holes to lower its Fermi energy, which will increase the Schottky barrier height. A metal's Fermi energy is fixed and cannot be raised or lowered by doping. This would allow a graphite/semiconductor Schottky barrier to act as though it were any variety of metal/semiconductor Schottky barriers based solely on the doping level of the graphite. Additionally, graphite is not a heavy metal and is non-toxic. Carbon itself is extremely abundant, although creating graphite is more intensive.

The research shown above is applicable to those interested in graphene. Since only one layer of graphene is in contact with the semiconductor and interactions between graphene sheets is relatively small especially at elevated temperatures, a graphene/semiconductor junction should act very similarly to a graphite/semiconductor junction. Graphene is undergoing research as a

“baseboard” upon which three dimensional devices can be built. Such devices would negate the two dimensional space restrictions in computer chips.

Graphite is extremely durable at high temperatures. When combined with the semiconductors gallium arsenide and silicon carbide, both of which are durable at high temperatures due to their low intrinsic carrier densities, devices will retain their functionality well beyond the limits of silicon. In the world of high power/high heat devices, a graphite/semiconductor Schottky junction which retains its rectification would be extremely useful.

The Schottky diode offers its own advantages in modern electronics where efficiency and speed are major concerns. The Schottky diode is based on the majority carrier whereas the PN diode, typically used in transistors, is based on minority carriers. Therefore, the Schottky diode has a much smaller forward bias voltage drop. The inevitable result is that PN diodes are less efficient than the Schottky diodes.

Similarly, since PN diodes use minority carriers, they require a definite time delay to “cool down” or relax. This delay limits a PN diode’s speed, especially at the speeds modern computers run. A Schottky diode, with its majority carrier transport process, does not require such a large time delay. Voltage can be switched and the current will change much faster as well. This contrast will make the Schottky diode much more applicable for high frequency devices and possibly even in personal computers if speeds reach the limits of the PN diode. High electron mobility transistors (HEMTs) are being researched for such purposes, but they are still limited by the capabilities of the PN junction, whereas the Schottky barrier can handle high frequencies much easier. Paired with a high resistance to heat, the graphite/semiconductor Schottky diode is suddenly becoming very applicable in modern electronics.



## Acknowledgments

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