

Recent developments in frequency domain multiplexing

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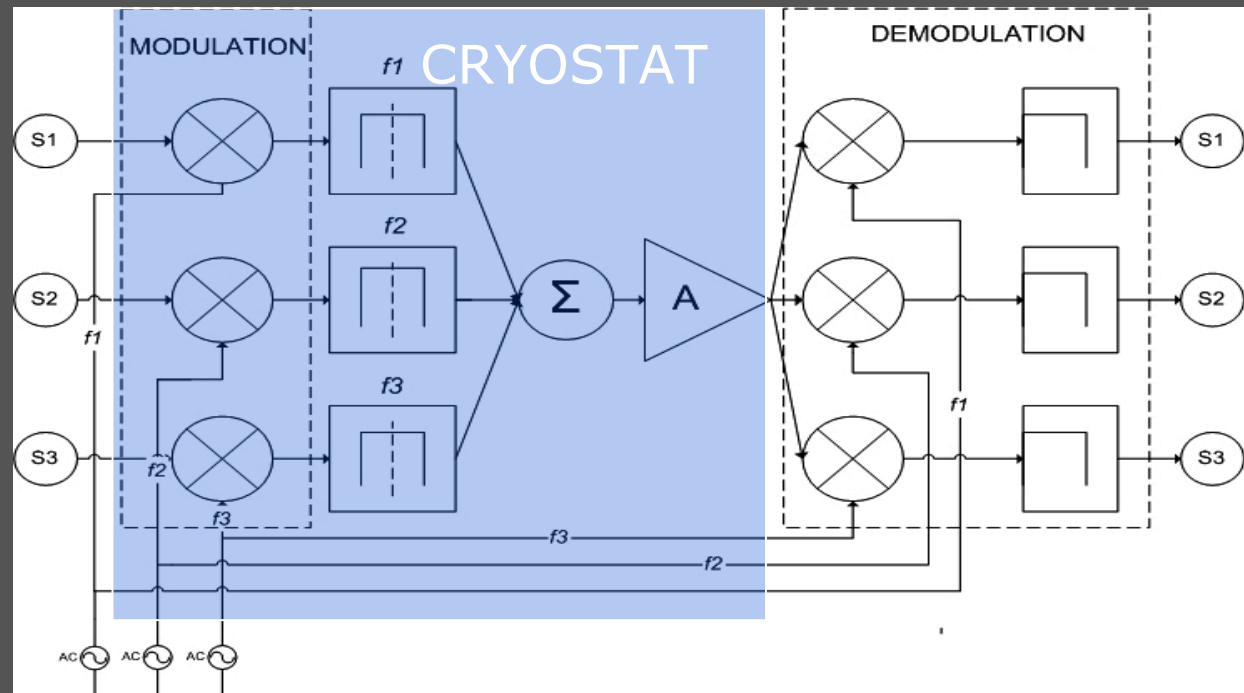
Outline

- Frequency domain multiplexed readout building blocks
- Building a prototype: European/Japanese EURECA collaboration
- Status building blocks
- Increasing the number of channels
- Summary

FREQUENCY-DOMAIN-MULTIPLEXING

Key characteristics:

- TESs act as AM-modulators of bias power
- Bias power sources separated in frequency space (i.e TESs AC-biased at frequencies f_1, f_2, f_3, \dots)
- LC band pass filter per pixel to prevent addition of wide-band noise
- Summed signal read-out by one SQUID-amplifier per column

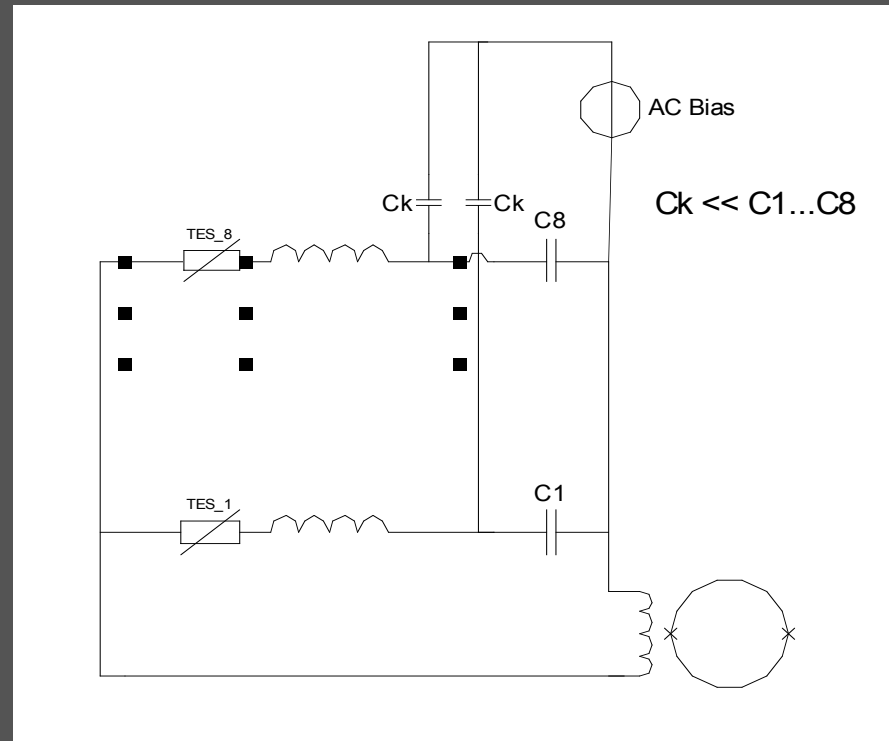


FDM compatible TES bias circuit

Dissipation-less voltage source

Capacitive voltage divider, instead of classical resistive voltage division

- Functional equivalent with resistive divider
- No extra dissipating element at base temperature
- Lower Q-requirements for capacitor



Building a prototype: the **EUROPEAN** Calorimeter **Array** (**EURECA**) Project

AIMS and Motivation:

- Design, build, and test of a prototype X-ray Imaging Spectrometer to demonstrate technical feasibility/readiness for a cryogenic space instrument by end 2007
- Use EURECA as a vehicle to breed a European/Japanese collaboration that is able and interested to deliver a cryogenic instrument for imaging X-ray spectroscopy
- Open up the potential to participate in future missions, like **ESA's XEUS (>2020)**, NASA's Con-X (>2020), future Japanese missions like NEXT (2015) and DIOS (2012), Italian's Estremo (2015), Dutch NEW (2015)
- Acquire development funding at (multi) national level

EURECA Project

ADR Cooler

- Commercial ADR (Janis)
- Flight type ADR

Detectors

- Si-micromaching
- Development + tests

- Mo-based bilayers

LC-filters

- Alternative routes

SQUIDS

- Three routes

Electronics

- LNA
- AC-BIAS + C&C
- Cold FLL
- Data Acquisition (BESSY)

Data analysis software

- System

- Algorithms

Contributions/Partners

PSI (Zürich)

MSSL (London)

→SRON

MESA (UTwente)

TMU (Japan), INFN(Genua), INAF(Rome),
KIP (Heidelberg)

IMM(Madrid), ICMA(Barcelona, Zaragossa)

→SRON

INA + ICMA (Zaragossa)

PTB (Berlin), VTT (Helsinki), SII (Tokyo)

→SRON

VTT (Helsinki)

PSI (Zürich)

Alcatel Alenia Space (Milano)

X-ray Astronomy (Leicester)

IFCA(Santander), MSSL(London),
Astr. Obs (Geneva)

X-ray Astronomy (Leicester)

Prototype development items

- EMI Shielding
- Microcalorimeters (tomorrow)
- LC bandpass filters
- SQUIDs
- Cryogenic detector unit
- SQUID front-end electronics
- AC bias source electronics
- Demultiplexing electronics
- Data analysis/processing

Approach:

- Conservative baseline system
- lumped elements, which can be exchanged once better parts are available

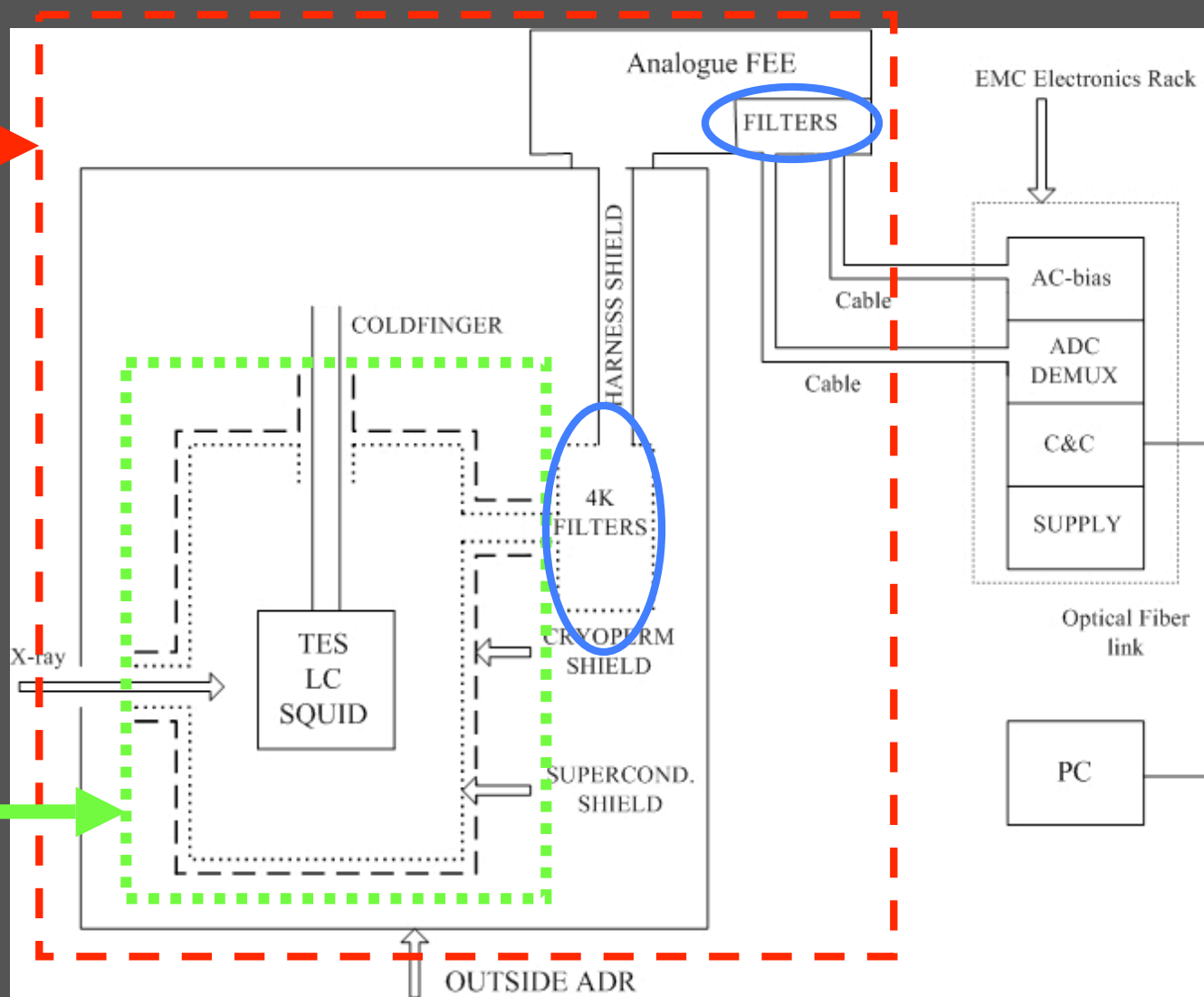
EMI prevention

- EMI origin and sensitivity:
 - pickup by wiring
 - 1 fW of power (broad band!) eq. ΔE of 1 eV
- Prevention approach:
 - Pickup attenuated by shielding and filtering in multiple stages
 - Minimize complexity within shielded environment
- Implementation:
 - Filters at entrance FEE-box and at 4 K interconnections
 - Differential electronics and twisted wire-pairs to reject common mode disturbances
 - Separation between SQUID FLL electronics and other parts
 - PC's + external equipment coupled by optical links

Prototype topological overview

Outer faraday cage

Inner faraday cage
+
Magnetic shield



Cross section cold head shielding

Radiation entrance window

Cryoperm outer shield 1 mm @ 4K

Superconducting inner shield
(Pb or SnPb plated OFHC copper) @ 500mK

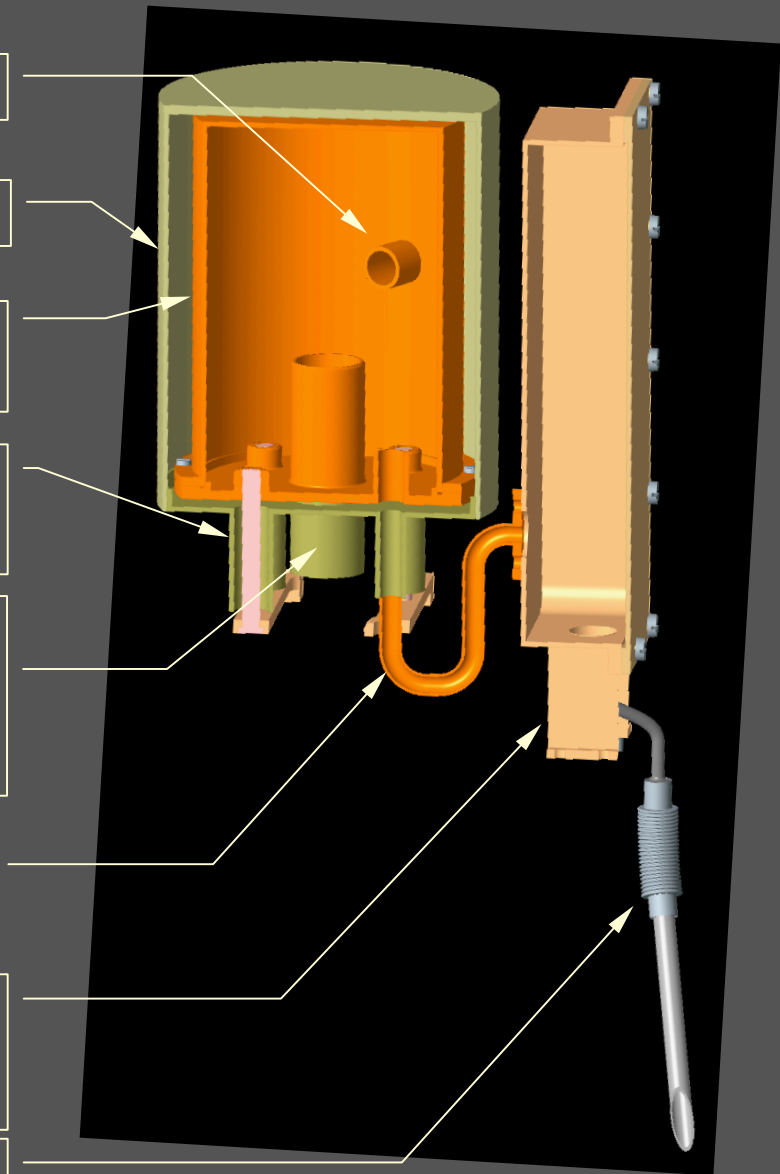
OFHC Copper support/thermal link
for inner shield @ 500mK

Cold finger entrance
Finger may be electrically coupled
with superconductor to inner shield
to reduce noise

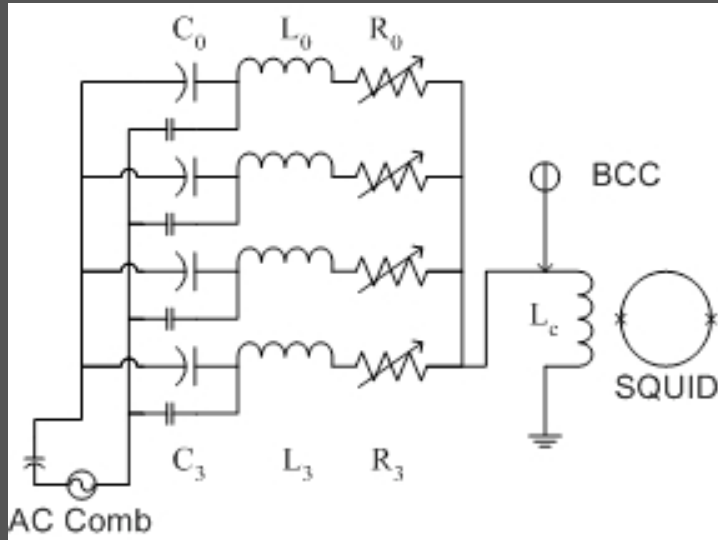
Superconducting harness shield
(Pb plated OFHC copper) @ 4K

Superconductor shielded loom
interconnection & filter box @ 4K
(Pb plated OFHC copper)

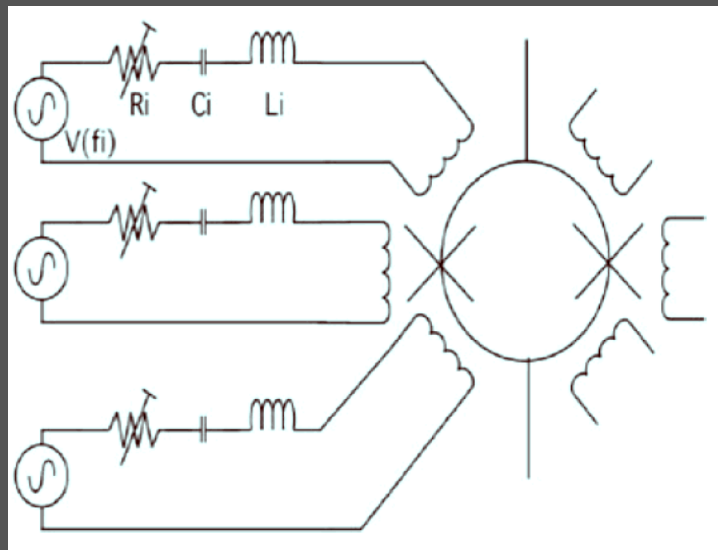
Harness shield, ss304



Summing Topology



Current Summing
BCC at input
8 channels/squid

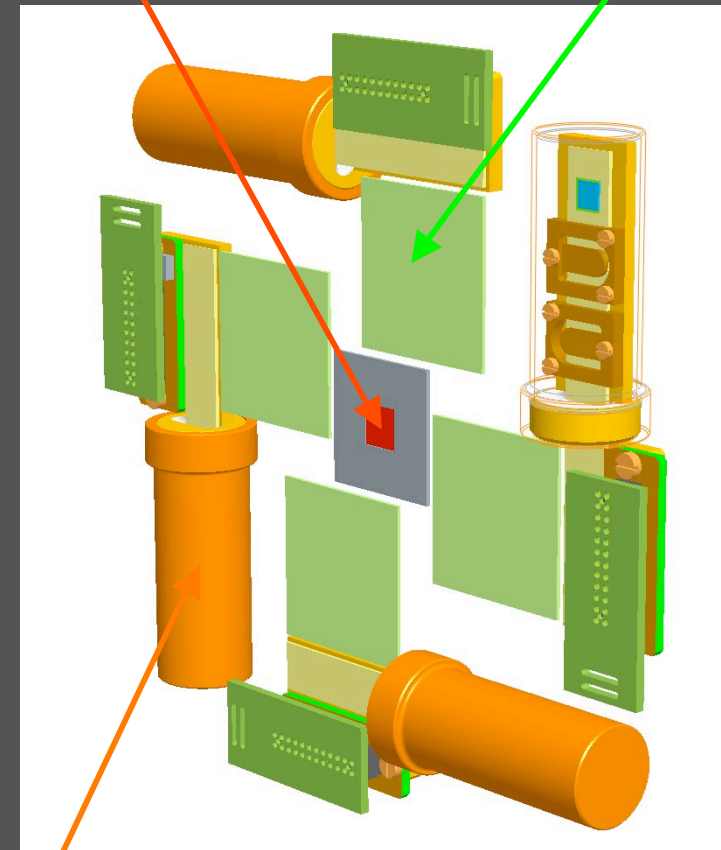


Japanese Ch.
Flux Summing
8-input SQUID
BCC via FB

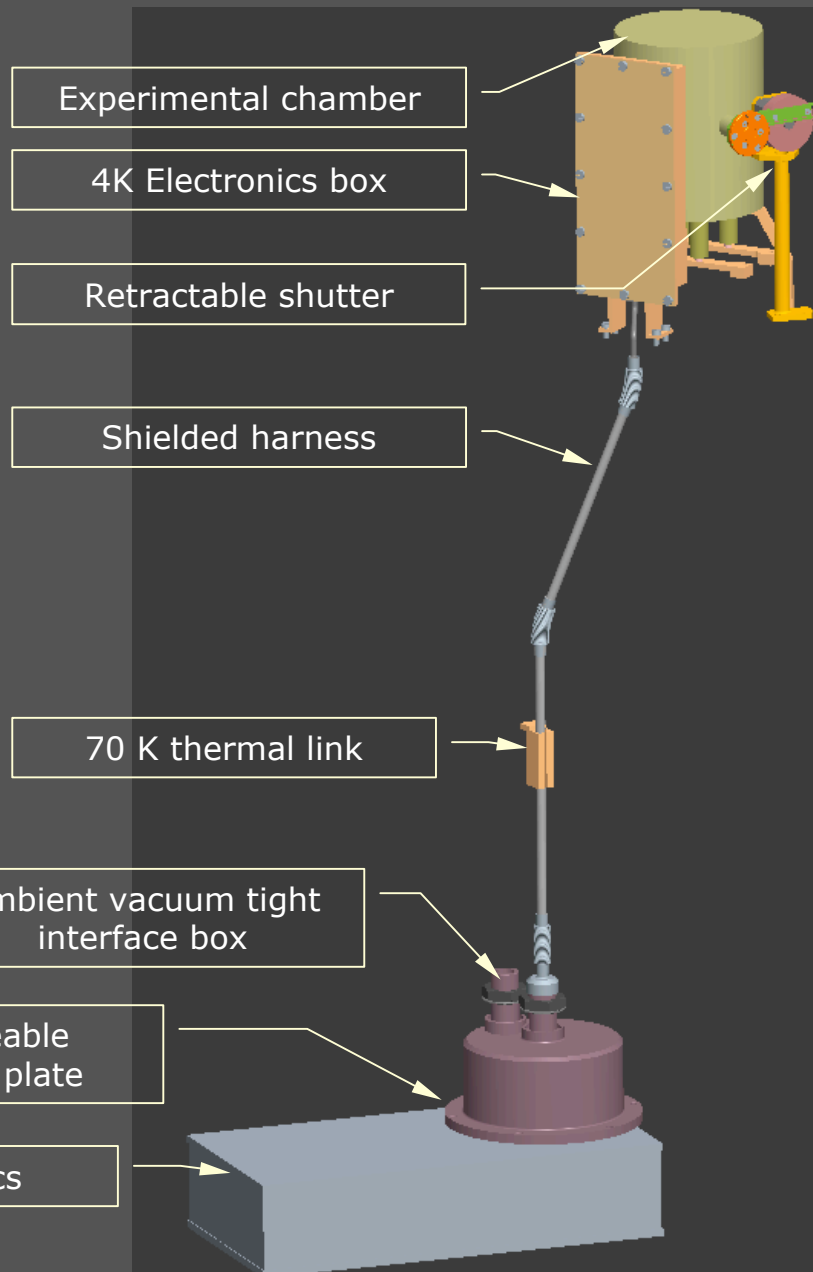
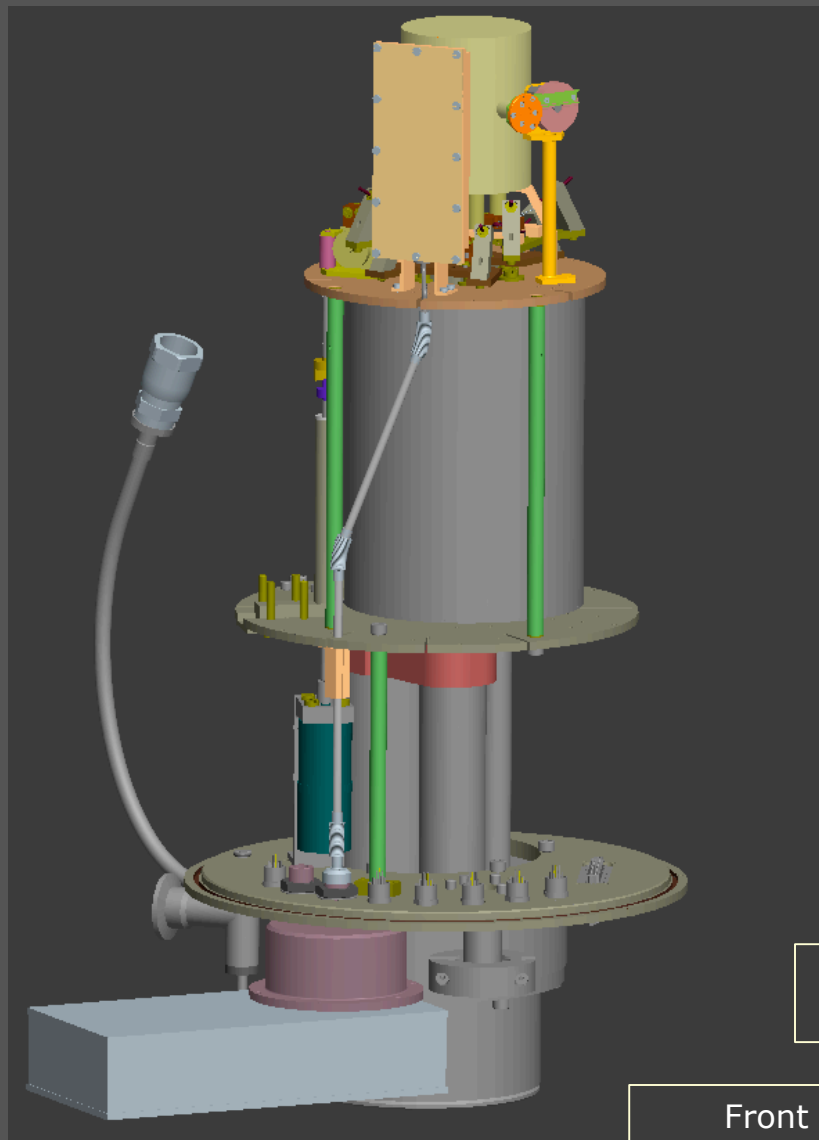
Cold Head Layout

TES-ARRAY

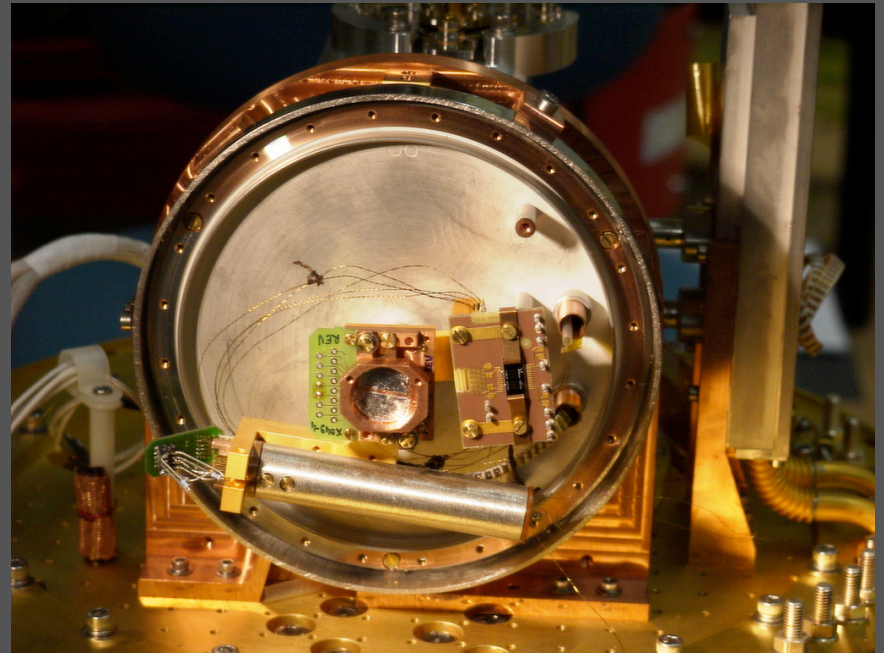
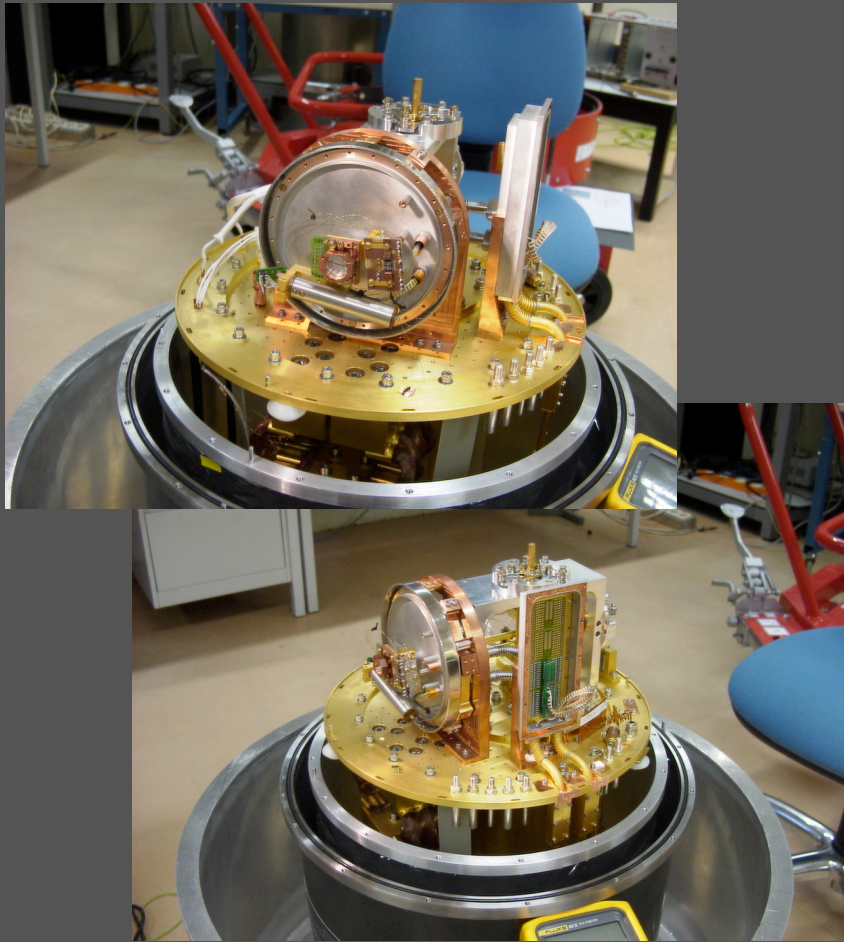
LC-filters



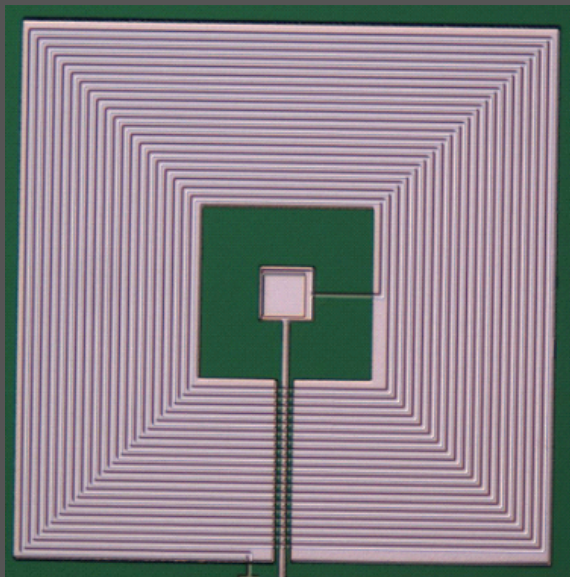
Cold head and COOLER



Cold head integration in progress



LC-filters



Filter Coil

$0.75 \times 0.75 \text{ mm}^2$

LC-wafer for EURECA:

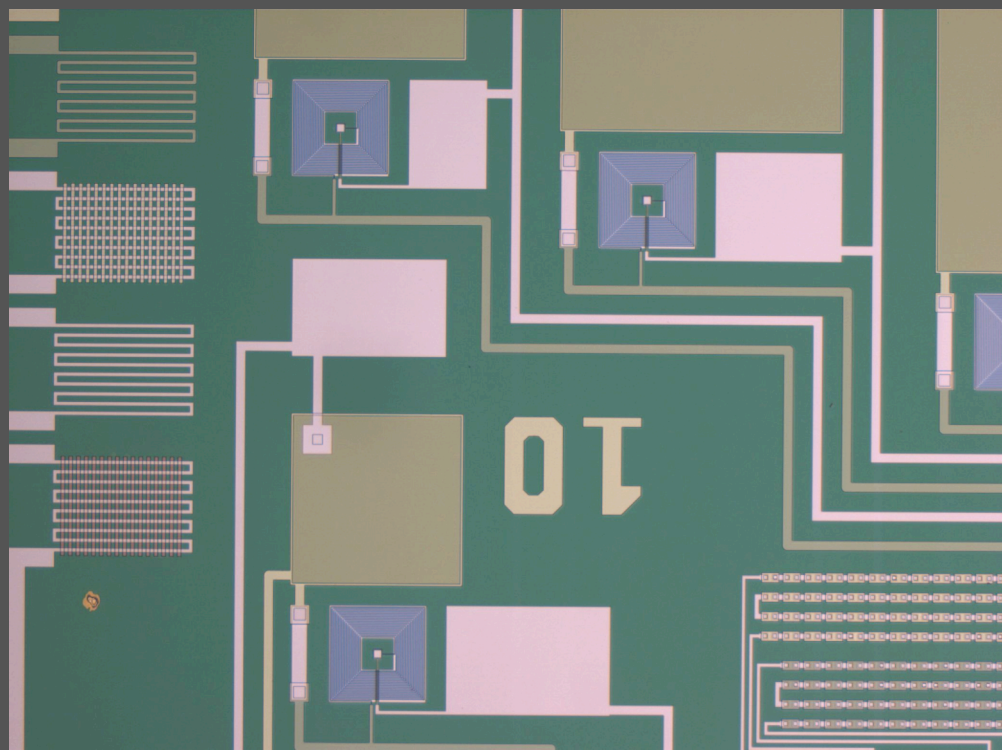
- $C = 4.3 \text{ nF/mm}^2$
- Q (expected) = 10.000

Eureca design values

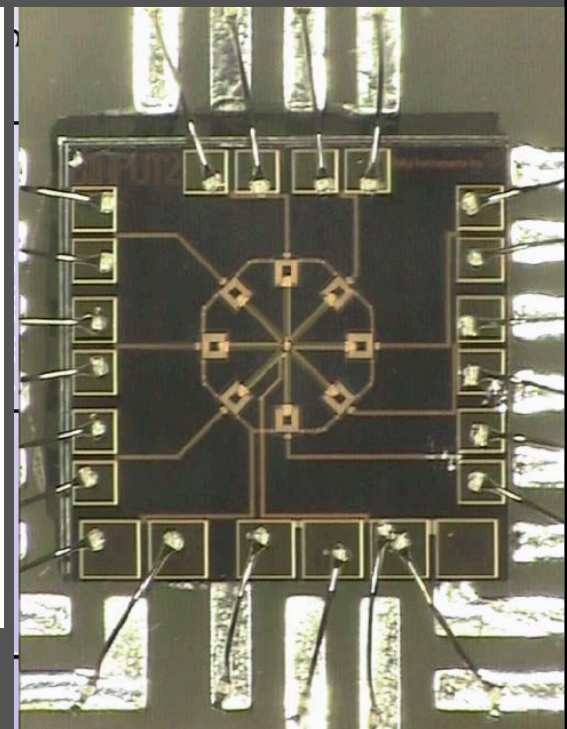
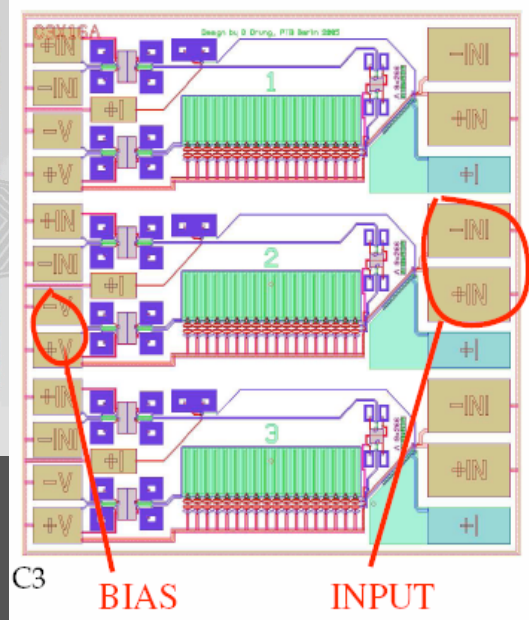
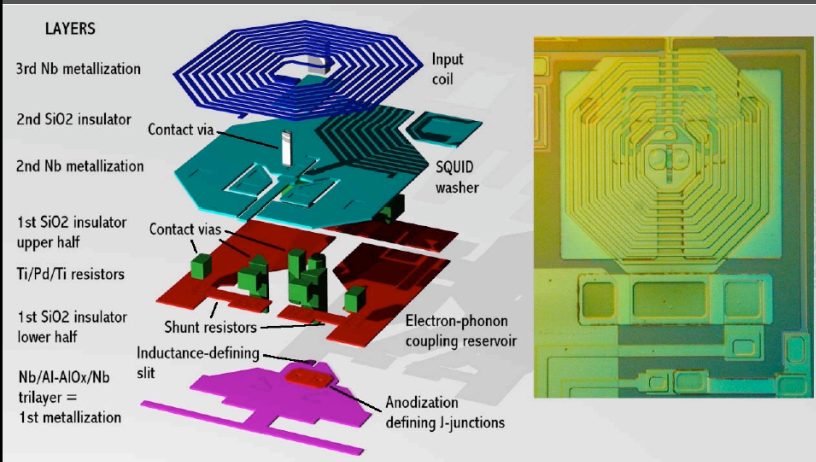
- $f = 0.8 - 2 \text{ MHz}$; $\Delta f = 100 - 200 \text{ kHz}$
- $L = 400 \text{ nH}$ for $R = 40 \text{ m}\Omega$
- So $C = 16 - 98 \text{ nF}$
- $Q > 800$ f (MHz) for $R_{\text{ESR}} < 3.5 \text{ m}\Omega$

Dielectric material

- Nb and Ta-oxides show too much absorption
- 25 nm Al_2O_3 with $\epsilon_R = 9.8$ has been chosen



SQUID current amplifiers



VTT input SQUID

$$\emptyset_N = 0.12 \mu\emptyset_0/\sqrt{\text{Hz}} @ 4\text{K}$$

$$L_{in} \approx 1\text{nH}$$

$$I_n = 3.5 \text{ pA}/\sqrt{\text{Hz}}$$

$T_N = 8 - 12 \text{ K}$ (2nd SQUID-array required)

PTB 16-SQUID array

$$\emptyset_N = 0.12 \mu\emptyset_0/\sqrt{\text{Hz}} @ 0.3\text{K}$$

$$L_{in} \approx 3 \text{ nH}$$

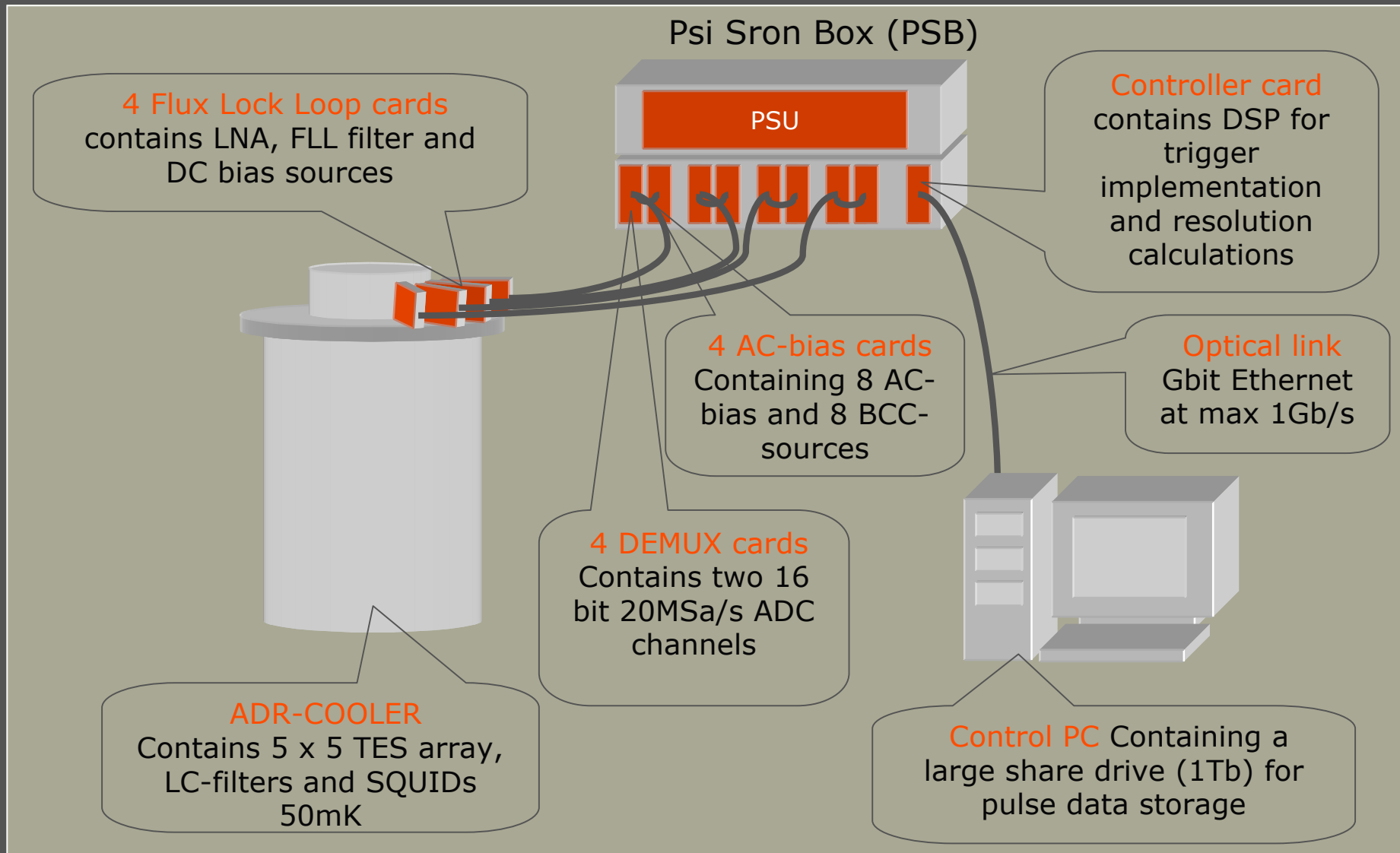
$$I_N = 2.8 \text{ pA}/\sqrt{\text{Hz}}$$

$T_N = 20 \text{ K}$ (direct coupling to LNA just possible)

$$\emptyset_N = 0.13 \mu\emptyset_0/\sqrt{\text{Hz}} @ 4.2\text{K}$$

(2nd SII SQUID-array planned)

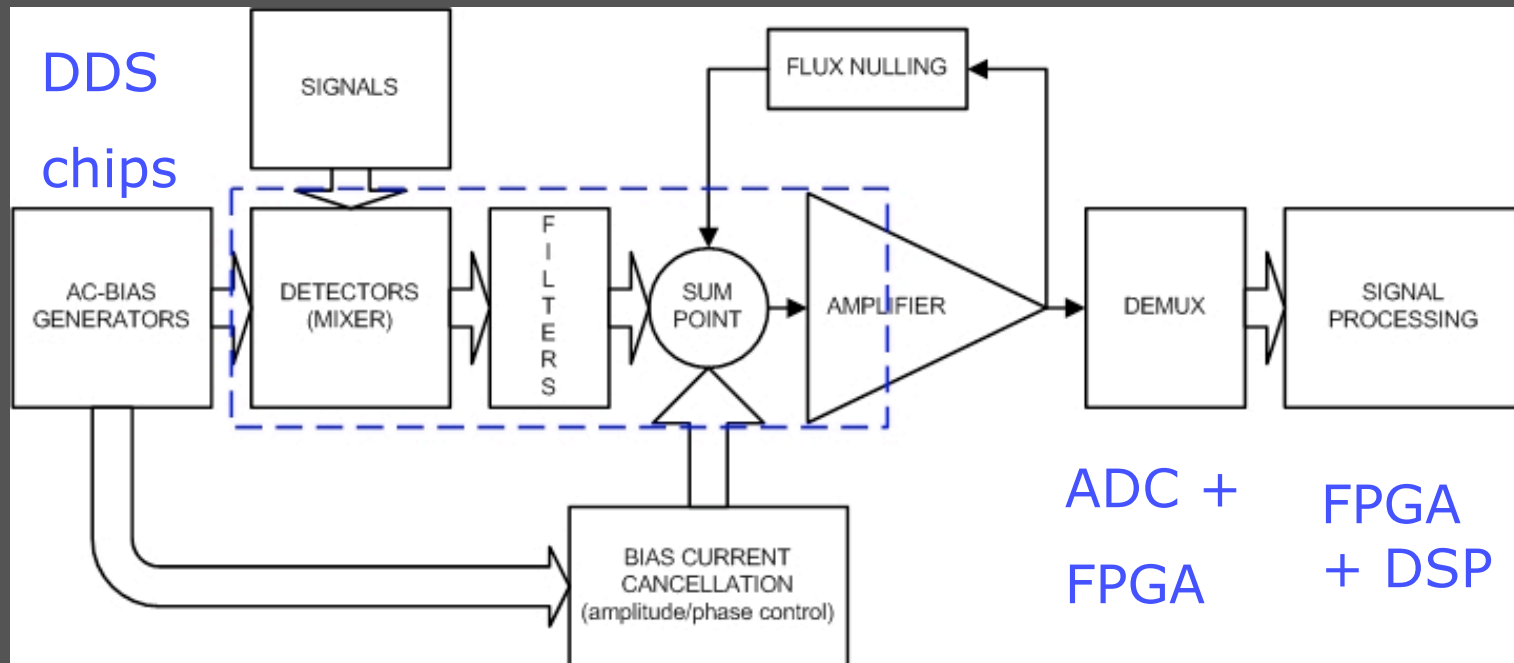
Artist impression of EURECA electronics



Functional diagram electronics

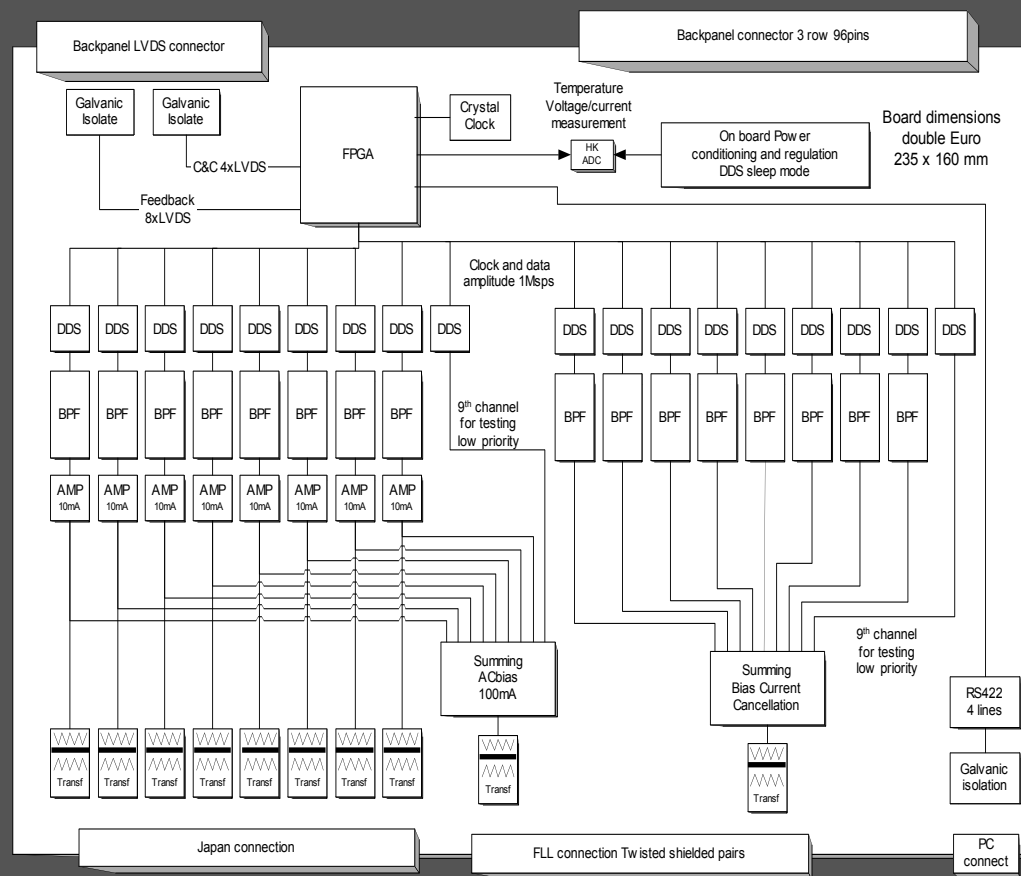
Applied technologies:

- AC-bias generation + Bias current cancellation (BCC): DDS chips
- DEMUX by ADC + digital processing: FPGA (later ASIC)
- Signal processing (photon energy extraction): FPGA + DSP

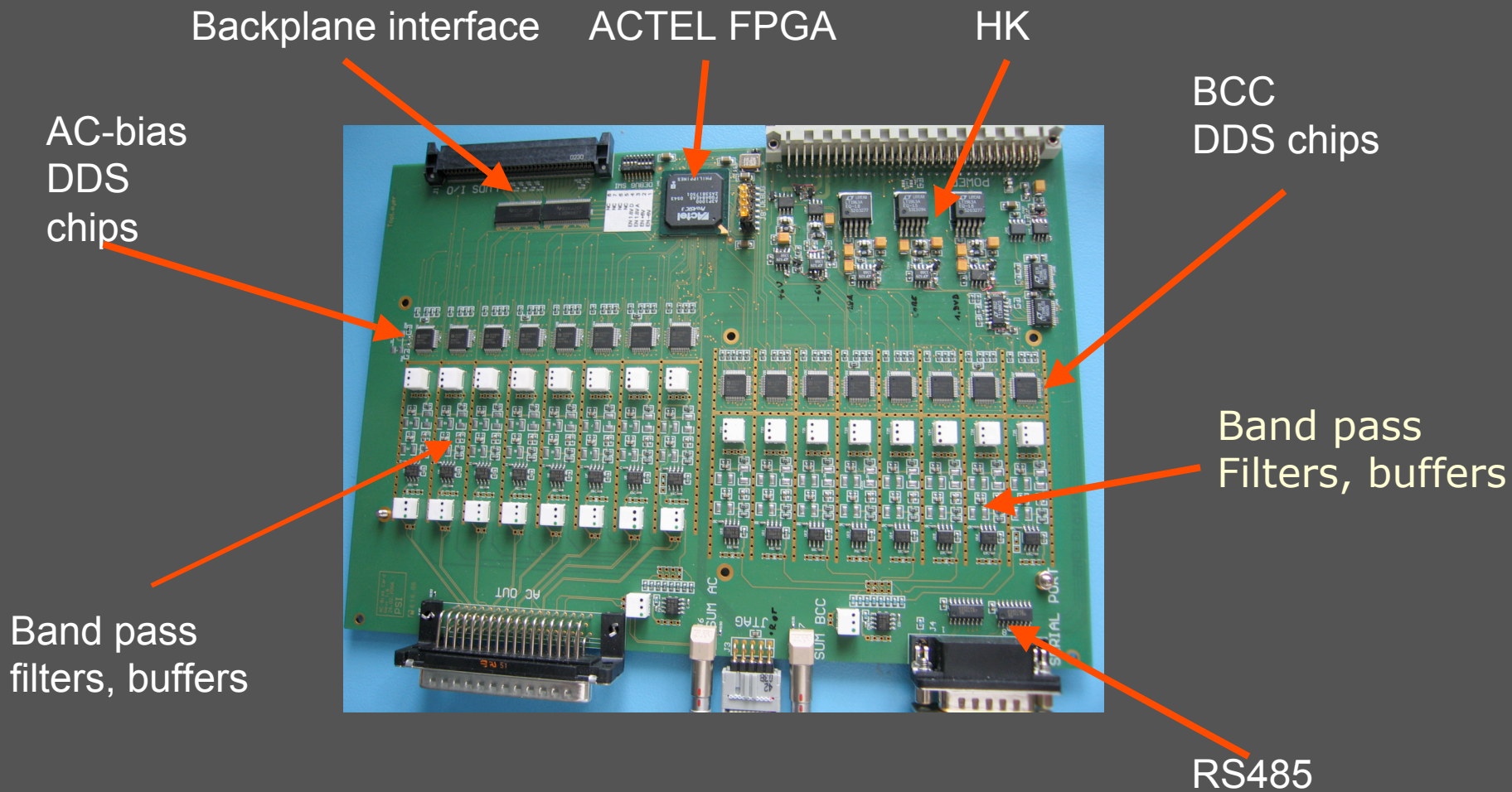


Functional diagram AC-bias sources

- 1 bias source/pixel (so f adjustable -relax of LC-filter f)
- $\pm 100 \text{ Hz} < f_c < \pm 2 \text{ kHz}$
- $< -120 \text{ dBc}$ amplitude noise
- $< -100 \text{ dBc}$ phase noise
- $< -80 \text{ dB}$ spurs
- Digital (DDS-chips) meet the specifications
- FPGA + DAC's could as well
- **ASICs under development for XEUS (power optimization)**

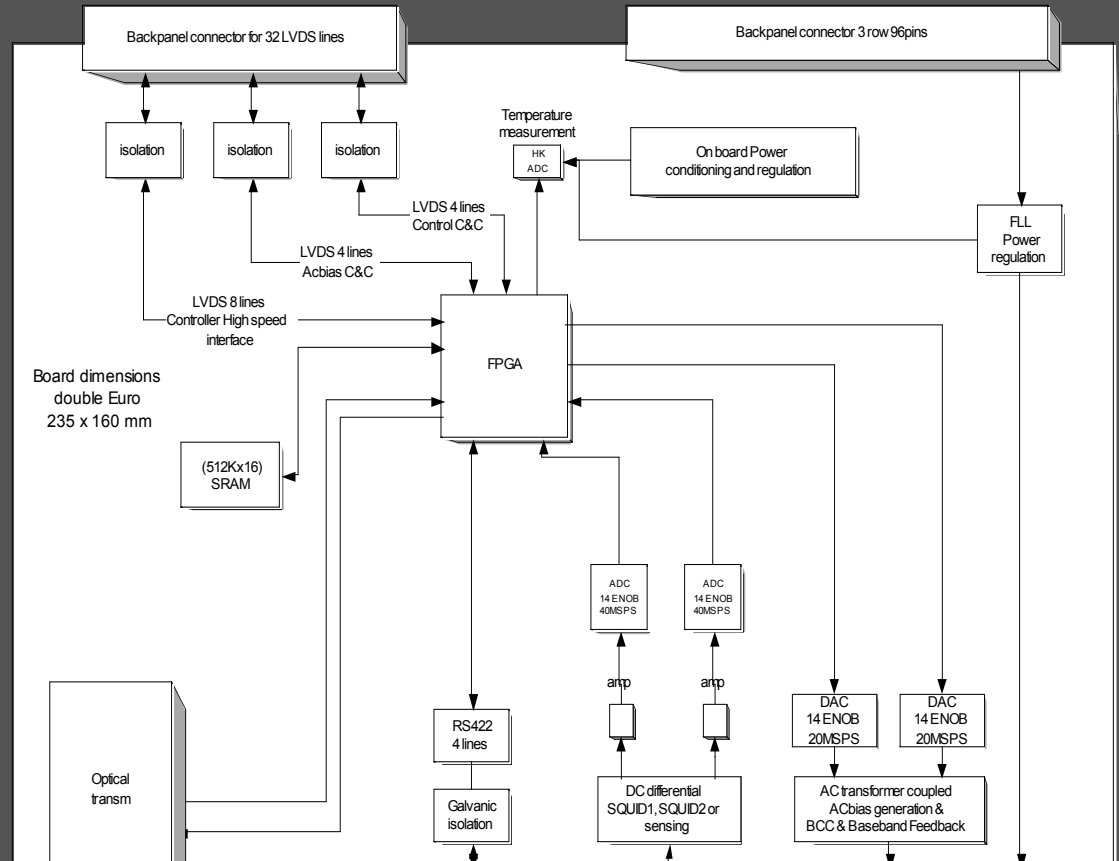


Functional 8-channel AC-bias card

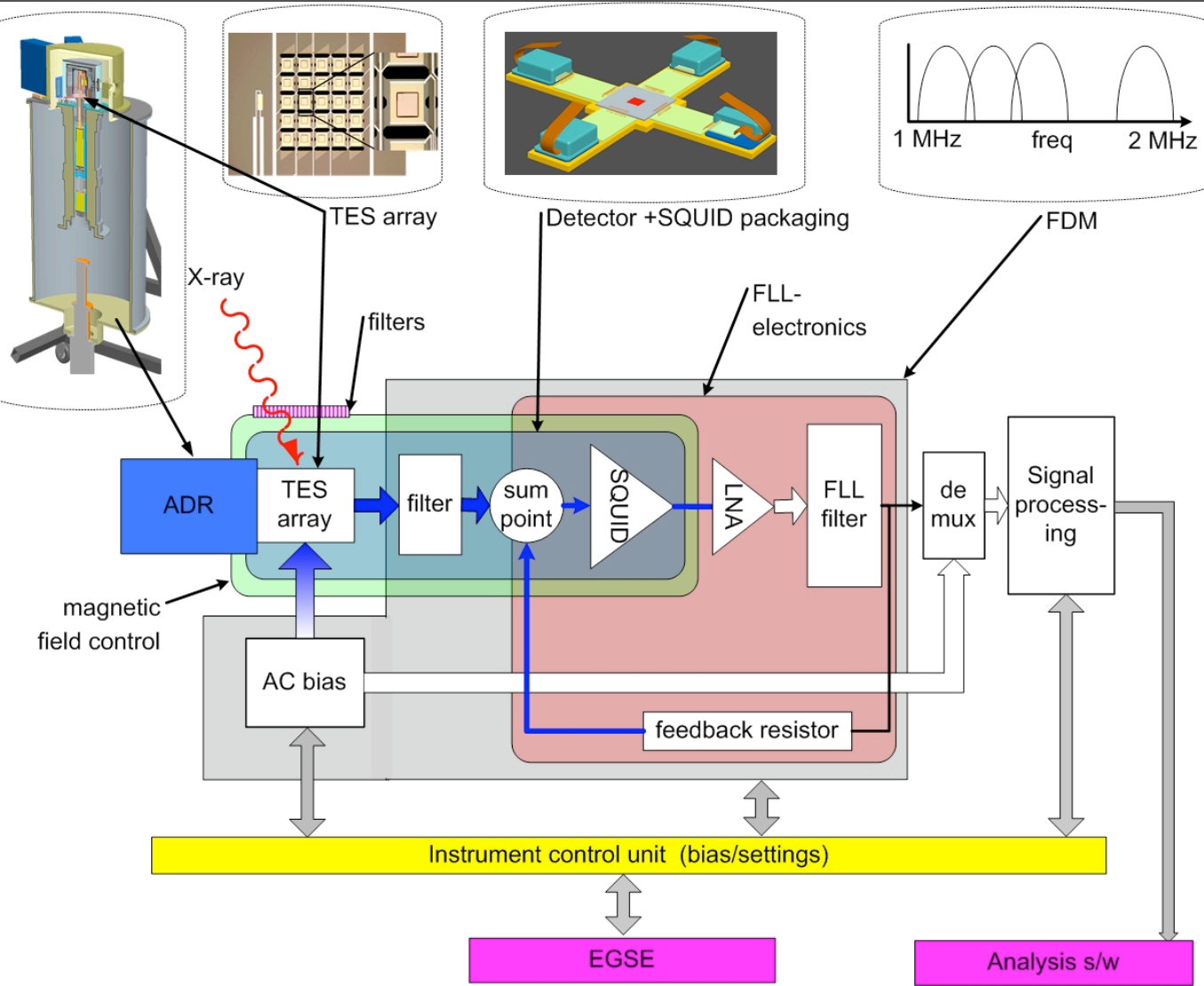


Functional diagram DEMUX-cards and C&C

- 2 16-bit ADC's
(25 MSA/s)
- Digital DEMUX in an FPGA
- Fast DAC's allow generation of signals for base-band feedback
- C&C card has large DSP to run energy extraction algorithm on data



EURECA Planning Overview



Qualification of a DC-biased pixel in dry ADR at BESSY
September 2006

Start Integration
 5 x 5 array + FDM-readout
Autumn 2006

Initial testing (one channel)
Begin 2007

Synchrotron testing (all channels)
End 2007

Increasing the number of channels

Channels per SQUID

- Number of channels limited by bandwidth
- Bandwidth limited by FLL system
- Two methods to increase bandwidth
 1. Baseband feedback
 2. Coarse/fine amplifier topology

Channels per cm^2 electronics

=> Electronics miniaturization by ASICs

Remember:

EURECA will have 8 channels/ SQUID, 24 channels in total

Dynamic range and Flux locked loop (FLL)

Requirements:

1. Signal dynamic range: $\pm 5 \cdot 10^6 \sqrt{\text{Hz}}$
2. Signal bandwidth: 150 - 200 kHz/pixel (crosstalk limited)

SQUID Dyn. Range:

- Typical SQUID: $\pm 0.25 \Phi_0 / \Phi_N = 2 \cdot 10^6 \sqrt{\text{Hz}}$
- SQUID in FLL:



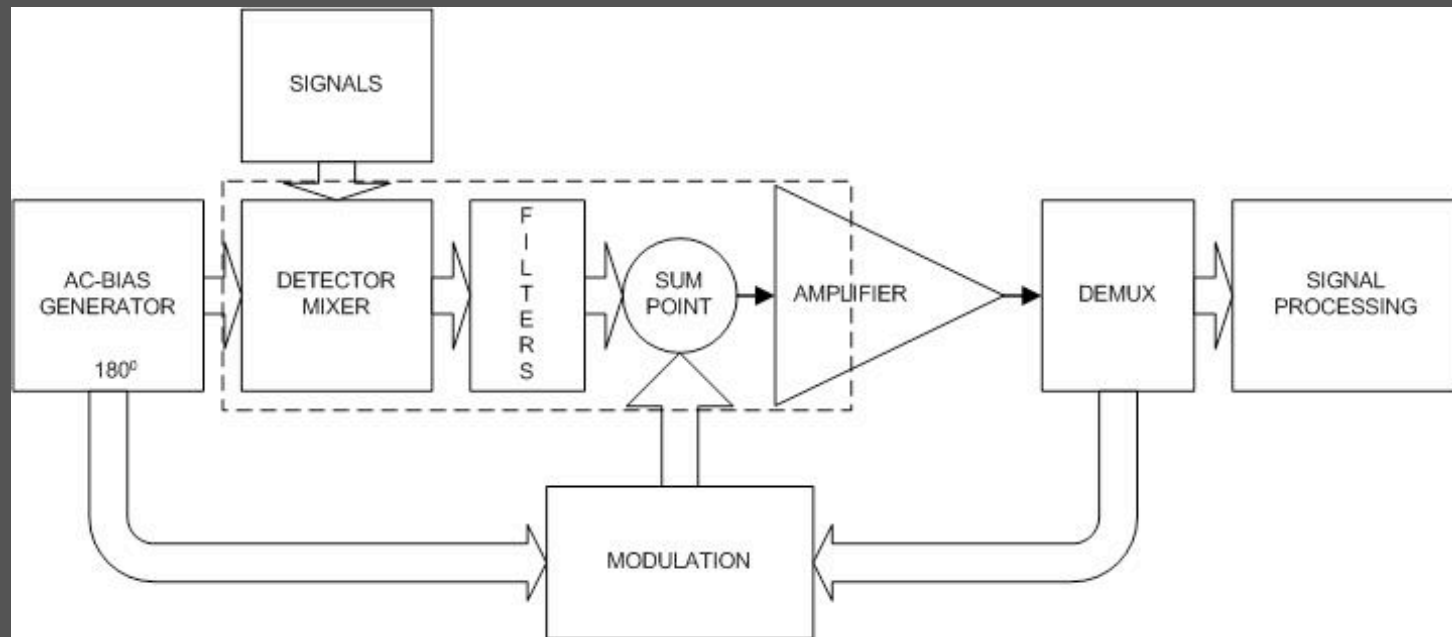
Assuming $G_{\text{FLL}} = 4$ (Unity-GBW, propagation delay limited ≈ 10 MHz)
 $\Rightarrow 2.5$ MHz available, I.e. 9 - 12 channels/SQUID.

This will be build for EURECA.

- So for larger arrays, other systems than standard FLL required.

Bandwidth improvement by BASEBAND FEEDBACK

- Carrier contains no information => feedback only on envelope
- A bandwidth up to about 10 MHz possible (SQUID back-action noise and LC-filter Q-factor limited)
- Stability issues limit packing density of channels
- FLL-gain of 5x with 32 pixels between 1 – 10 MHz appears feasible



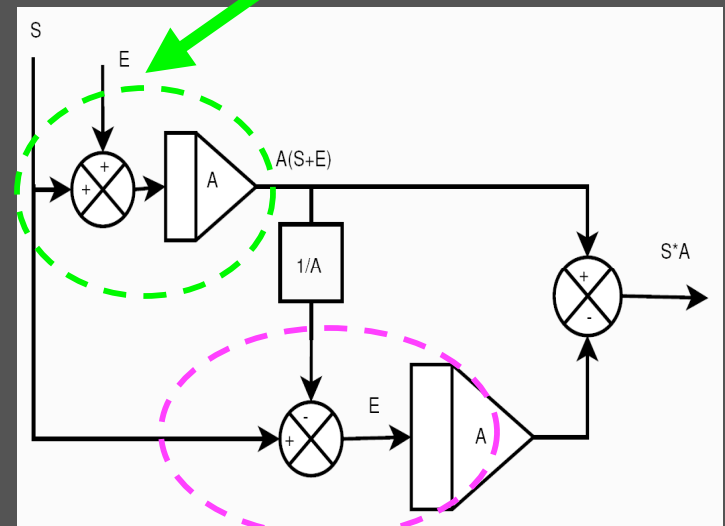
Bandwidth improvement by Coarse/Fine Amplifier Topology

Operating principle:

- 2 SQUIDs: **coarse** and **fine**
 - F-SQUID measures error made by coarse SQUID
 - Subtraction of coarse and fine signal yields original signal
- Coarse/fine topology enables 10 MHz bandwidth (backaction noise limited) => 40 – 80 channels/squid (100 μ s microcalorimeters)

Requirements:

- Coarse SQUID amplification sufficient to match RT-amplifier
- $A*S$ and $A*E >$ RT amplifier noise => 2 stage SQUID
- Largest signal $< 0.5 \phi_0$
- Flux noise F-SQUID negligible => minimum M-value



Coarse SQUID

Fine SQUID

Summary and Conclusions

- EURECA well under way with Preliminary Design Review in Jan. 2006. Start integration 1st channel in ADR by end-2006
- Integration of single TES-pixel with DC-electronics in dry ADR started with aim to perform BESSY-calibrations in 3rd week of September 2006
- FDM readout can be implemented without the bias resistors, and their dissipation
- FDM with standard FLL-electronics will only multiplex about 10 pixels per SQUID-channel with XEUS requirements ($E_{\max}=10$ keV, $\Delta E = 2$ eV, and $\tau = 100$ μ s)
- Coarse/Fine amplifier topology, Base-band feedback, or a combinations should offer appreciably better performance. It is planned to start working on this by 2007 in parallel to EURECA
- SQUIDs close to the requirements available. But further optimization still required
- ASIC developments for Space (power reduction) is starting

COLLABORATORS ON EURECA

SRON

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ISAS/JAXA + Metropolitan (SQUIDs + FLL for one read-out channel)

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Alcatel Alenia Spazio (Cold FLL)

Paolo Bastia

INA/ICMA (LC-filters)

Javier Sese

IMM (Mo-bilayers)

Jose Anquita

MSSL (ADR)

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