List of fixes applied to the assembled SP02:

   Problem: P1 has a circular shift of pin rows.
   How to fix: mount P1 on stand-offs, wire pcb A-pads to connector Z-pins, B-pads to A-pins, C-to-B, D-to-C and Z-to-D.

2. Where: Sheet 115 - CCB_BUFFERS
   Problem: U147 has wrong DIR set.
   How to fix: cut U147.24 from the GND net and reconnect it to the 3.3V net (wire jumper between U147.24 and U147.2).

3. Where: Sheet 12 - MS_BUFFERS
   Problem: unterminated MS_DAT0 backplane signal.
   How to fix: add 51 Ohm resistor between J3.A4 (MS_DAT0) and J9.B11 (VTT).  

4. Where: Sheet 12 - MS_BUFFERS
   Problem: unterminated MS_DAT1 backplane signal.

5. Where: Sheet 12 - MS_BUFFERS
   Problem: U132.35 connection to VREF is missing.
   How to fix: add a wire jumper between U132.35 and U146.31.

6. Where: Sheet 12 - MS_BUFFERS
   Problem: U133.35 connection to VREF is missing.
   How to fix: add a wire jumper between U133.35 and U145.31.

7. Where: Sheet 9 - JTAG_INTERFACE
   Problem: pullup resistor at /RDY output is missing.
   How to fix: add a 1 KOhm resistor between U137.20 and U137.28.

8. Where: Sheet 115 - CCB_BUFFERS, sheet 111 - CCB/VME_CONTROL, sheet 80 - ME_ALIGNMENT.
   Problem: 80.1574 MHz clock from the FPGA DCM has excessive phase jitter and can not be used as a reference clock for TLK2501 transceivers.
   How to fix: remove U107;  
   wire PATCH1 (QPLL patch to double the CCB clock);  
   remove R144, R145, R146, R147;  
   wire PATCH2 (LVDS_Repeater patch to deliver it to the TLK2501 transceivers);  
   mount a 51-Ohm 0603 chip resistor on R145.2 and R147.2 pads

9. Where: Sheet 117 - PWR_DISTRIB.
   Problem: Allegro cq3710.brd board file replaces J14, J15 and J16 SOCKET_4 parts with HD1, HD2 and HD3 HEADER4X1 packages/devices respectively.
Add a 1 kOhm resistor between U137.20 and U137.28 (5.0V).

CONNECTOR'S TDI PIN -- SCAN MASTER'S TDO PIN
AND VICE VERSA

UP - SELECT CHAIN 1  DOWN - PROGR CHAIN SELECTION

JTAG_CHAIN_0: MAIN FPGA
JTAG_CHAIN_1: VME->ME4->ME3->ME2->DDU->ME1DEF->ME1ABC
JTAG_CHAIN_2: SR LUTS
Add a 51 Ohm resistor between J3.A4 (MS_DAT0) and J9.B11 (VTT), and J3.B4 (MS_DAT1) and J9.B11 (VTT).

Add a wire jumper between U133.35 and U145.31 (VREF1)

Add a wire jumper between U132.35 and U146.31 (VREF2)
Mount a 51-Ohm 0603 chip resistor on R144,2 and R147.2 pads when applying QPLL patches to the board.

Remove R144, R145, R146, R147 when applying QPLL patches to the board.

Net AFIFO_RSV2 becomes CLK80P and net AFIFO_RE becomes CLK80N when applying QPLL patches to the board.
Remove U107, when applying QPLL Patches to the board
Lift U147.24 from the pad and reconnect it to the 3.3V2 net (wire jumper between U147.24 and U147.2).

Lift U148.5 when applying QPCL patches to the board.
P1 has a circular shift of pin rows. Mount P1 on stand-offs, wire pcb A-pads to connector B-pins, B-pads to A-pins, C-to-B, D-to-C and Z-to-D.
Allegro cq3710.brd board file replaces J14, J15 and J16 SOCKET_4 parts with HD1, HD2 and HD3 HEADER4X1 packages/devices respectively.