Status of CSC Trigger

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ALCT Boards (EMU subsystem)

Status:
- 284 boards produced
- 153 tested and passed
- 101 shipped out
TMB in Preproduction

Status:
- 18 built
- Firmware being updated

- Generates Cathode LCT trigger with input from CFEB (comparator)
- Matches ALCT and CLCT; sends trigger primitive info via MPC to Lev-1 muon trigger, sends anode and cathode hits to DMB.

Main FPGA (on back) XILINX XCV1000E
Mezzanine board
Input connectors From 5 CFEB's
Input connectors From ALCT

UCLA
MPC Design Status

- 3 boards have been fabricated and assembled in summer
- Have 6 UCLA mezzanine cards in hand
- Tested MPC standalone (sorter logic) and with one and two Trigger Motherboards and full-size custom backplane
  - various patterns sent from TMB to MPC at 80Mhz
  - feedback “winner” bits from MPC to TMB
  - periodic FPGA reconfiguration from EPROMs (both MPC and TMB) upon “hard reset”
  - measured the board latency

Waiting to test with Sector Receiver/Processor
CSC Track-Finder Crate Design

- Single Track-Finder Crate Design with 1.6 Gbit/s optical links
CSC Track-Finder GTLP Backplane

DDU (for DAQ)
MPCs (for test)
Endcap 1 (6 SPs)
CCB
Sorter
Endcap 2 (6 SPs)

Connections to DT Transition cards
CSC Sector Processor (2nd Prototype)

- Phi Global LUT
- Eta Global LUT
- Phi Local LUT
- DC-DC Converter
- EEPROM
- Fits all of previous SP board logic!
- VME/CCB FPGA
- From CCB
- To MS
- PT LUT
- MB1-to-SP
- ME1-to-DT
- Main FPGA Mezzanine Card
- SRAM
- Stiffener
- Indicators
- FM RJ45
- TLK2501 Transceiver
- Front FPGA
- DDU FPGA
- Optical Transceivers (16)
- Fits all of previous SP board logic!
Sector Processor Status

Schematics complete
Mezzanine card layout complete
Main board:

→ Problems encountered using OrCAD Layout
  □ Board is too complex, manual routing is labor intensive, and program pushed to its limits
  □ Suffered catastrophic failure
→ Sent routing to outside vendor for completion (they use Cadence Allegro for layout)
  □ Preliminary layout received
  □ Under review by design engineers
→ Fabrication and Assembly expected to take 3 weeks
  □ Prototype ready by January

Components ordered, most in hand
1. VME/CCB interface and Front FPGAs
   ➔ PNPI. Started. Necessary for optical link tests to MPCs

2. SP chip
   ➔ Trigger logic done, but supporting logic still to do

3. DDU (DAQ interface) firmware
   ➔ PNPI. Still to be done. Not critical for initial tests.

Hope to have first two items ready when board fabrication is complete
   ➔ Approximately Jan.15
**Track-Finder Test Plans**

**Approximate schedule**

- Jan.’03: SP prototype completed, initial tests begin
- Feb.’03: MPC→SP optical link tests
- Mar.’03: SP trigger logic tests
- Apr.’03: CSC system tests with cosmic rays
- May’03: beam tests with CSC chambers at CERN

**Time is very tight, and still have a lot of firmware and software to write**

- Software will be written using XDAQ, hopefully in a way that is relevant for future slice tests of muon system
Software and Test Plans

Getting started on implementing a XDAQ compliant set of software to run CSC trigger tests

VME (HAL):

- Classes exist for VME configuration of TMB, MPC, CCB, and TTC from Rice University.
- Developing similar SP class with additional capability to download LUTs and FPGAs from external files
  - Integrating previous code from prototype tests in 2000

Front-End Drivers (XDAQApp)

- Developing “Driver” classes that instantiate VME classes and execute XDAQWin configuration commands

![Diagram showing Bit3, Track-Finder Crate, Linux CPU, and XDAQApplications: SPDriver, CCBDriver (MPCDriver)]
CSC “TrigDAQ” Implementation

Track-Finder Crate

Peripheral Crate 1

Peripheral Crate n

Bit3

DB

Linux CPU

XDAQ Applications:
- SPDriver
- CCBDriver
- (MPCDriver)

“FEDs”

XDAQ Win

“Run Control”

Bit3

DB

Linux CPU

XDAQ Applications:
- MPCDriver
- TMBDriver
- CCBDriver

“FEDs”

XDAQ Applications:
- EventGenerator/Builder
- “Event Builder”