Plans for VME Backplane and Status of the Track-Finder

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Channel Link Backplane Tests

Prototype VME backplane tested with Channel Link

- Longest traces extend 4 VME slots
- Line pitch is 6 mils, impedance measured to be 130 Ω
- Transmitter and Receiver boards have input/output FIFOs implemented in FPGA

No Errors found operating Channel Link at 40 MHz

- Fixed and random patterns tested
- FIFOs send/receive data at full speed
- Maximum clock achieved is 58 MHz without errors (400 MHz backplane frequency)
- Stated maximum should be 66 MHz

TriDAS Backplane

The Track-Finder crate in the TriDAS project has a similar backplane to the EMU peripheral crate

Crate contains:

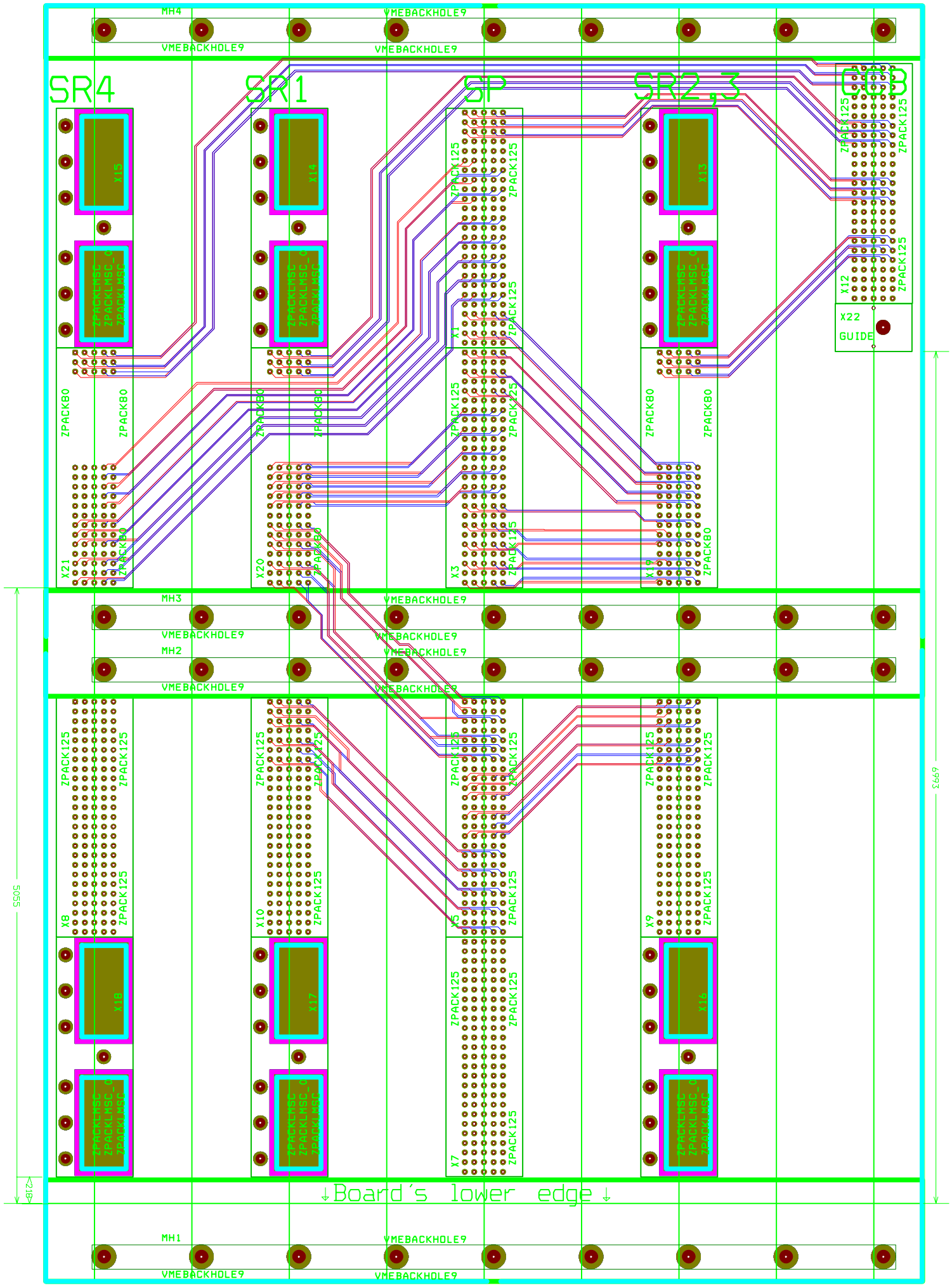
- **2 Sector Processors**
- **6 Sector Receivers**
- **1 Clock and Control Board**

} **double width modules**

Each Sector Processor receives ~600 signals via Channel Link

Back of crate also has 8 transition boards to DT Trigger system

- **Requires male connectors to punch through to back of crate**


SR4
SR1
SP
SR2,3
SB
MH4
MH3
MH2
MH1
VMEBACKHOLE9
X15
X14
X13
X12
X22
GUIDE
X21
X20
X1
X3
X18
X8
X10
X5
X9
X18
X17
X16
X7
ZPACK125
ZPACK80
ZPACKLMSC
5055
6993
218
↓Board´s lower edge↓

Status of Prototype TriDAS Backplane

Prototype backplane designed for one sector (half of crate)

Standard 3U VME64x upper connector

- **A24/D16 VME control and 3.3 V**

Custom 6U Channel Link backplane

Routing basically complete

Production to begin in a month or two

- **When SR and SP are ready to go to production**

Crate tests to begin June 1

Plans for EMU backplane

Begin design after results of Track-Finder crate tests

- **Fall 2000**

Need about 2 months for routing, once signals and connectors are specified

- **It will be more complicated than the Track-Finder backplane because the VME modules are single width and there are more signals**

Propose 10/1/2000 as target date to define signals and connectors

- **CLCT/TMB, DAQ-MB, MPC, CCB**

But, backplane routing will define pinout and connector locations

Prototype backplane must be produced by 3/1/2001

Status of Prototype Track-Finder

Sector Processor / Sector Receiver interface defined

- Includes extra bits to handle ghost-busting
- Backplane routing nearly complete

DT Trigger interface still to be fully defined

- Freeze design for prototype, though

FPGA schematics nearly finished for trigger logic

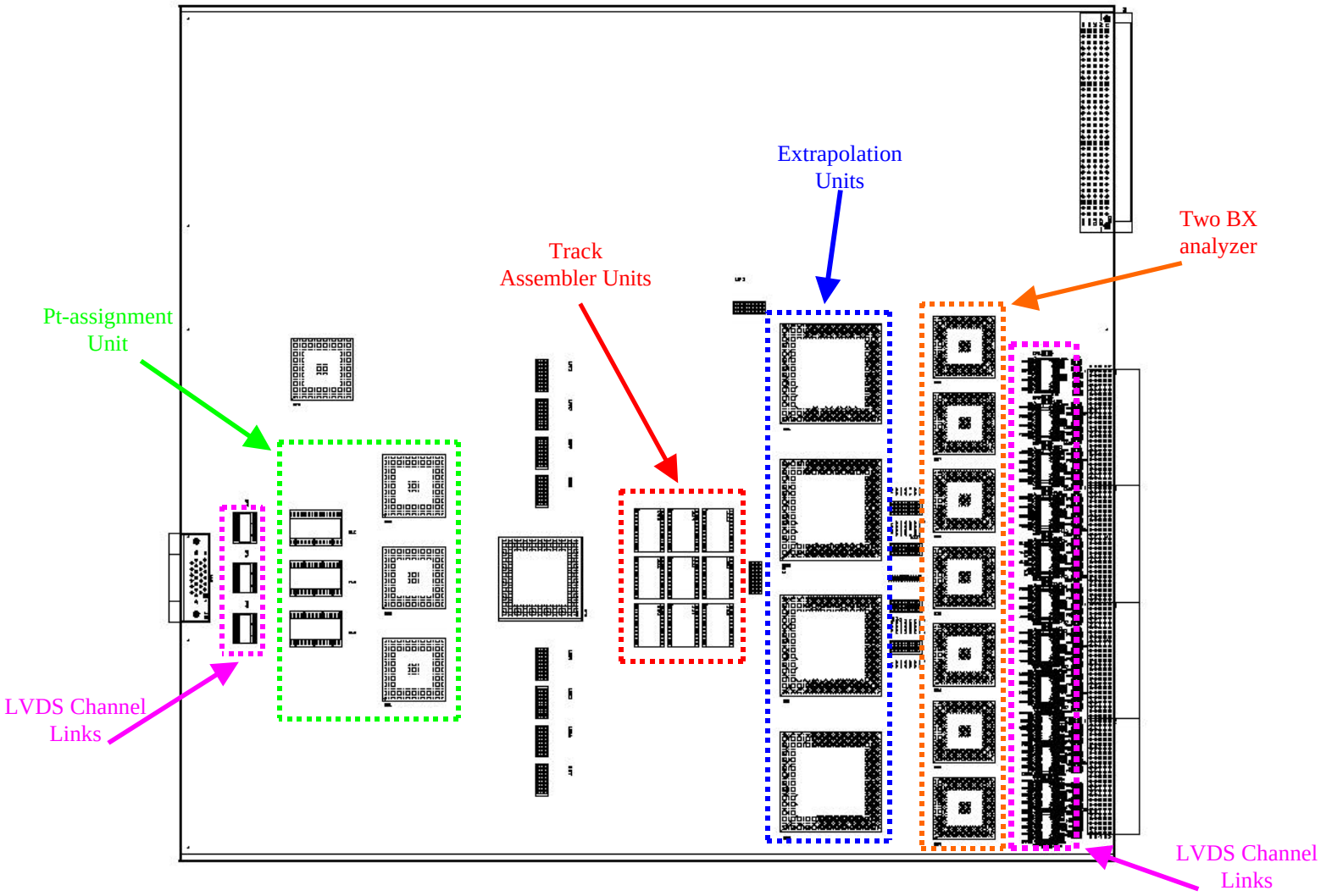
Board routing underway

- 11 layers, including 3 power planes

VME/JTAG interface underway

- Xilinx Spartan VME Interface
- National SCANPSC100F Parallel to Serial interface for JTAG

UCLA meeting (current version)



Board Layout of the Sector Processor.

Sector Processor FPGA type	Design status		
	Started	*Underway*	*Finished*
1. *Two* Bunch Crossing Analyzer (endcap)			√
2. *Two* Bunch Crossing Analyzer + FIFO as delay (barrel)		√	
3. Extrapolation Unit + Global FIFO (MB1 – ME2, MB2 – ME2)		√	
4. Extrapolation Unit + Global FIFO (ME1 – ME2) or (ME1 – ME3)		√	
5. Extrapolation Unit + Global FIFO (ME2 – ME3, ME2 – ME4, ME3 – ME4)		√	
6. Final Selection Unit	√		
7. Pt – assignment 1			√
8. Pt – assignment 2			√
9. Pt – assignment 1 (lowest priority)		√	
10. Pt – assignment 2 (medium priority)		√	
11. Pt – assignment 3 (highest priority)		√	
12. Output data storage			√
13. VME Interface		√	
14. Clock Distribution and control signals			√

Removed from design

FPGA design current status

Sector Processor FPGAs

Design incorporates Xilinx Virtex FPGAs

Bunch Crossing Analyzer:

XCV50-6BG256C (speed grade = 6)

Number of slices: 432 out of 768 (56%)

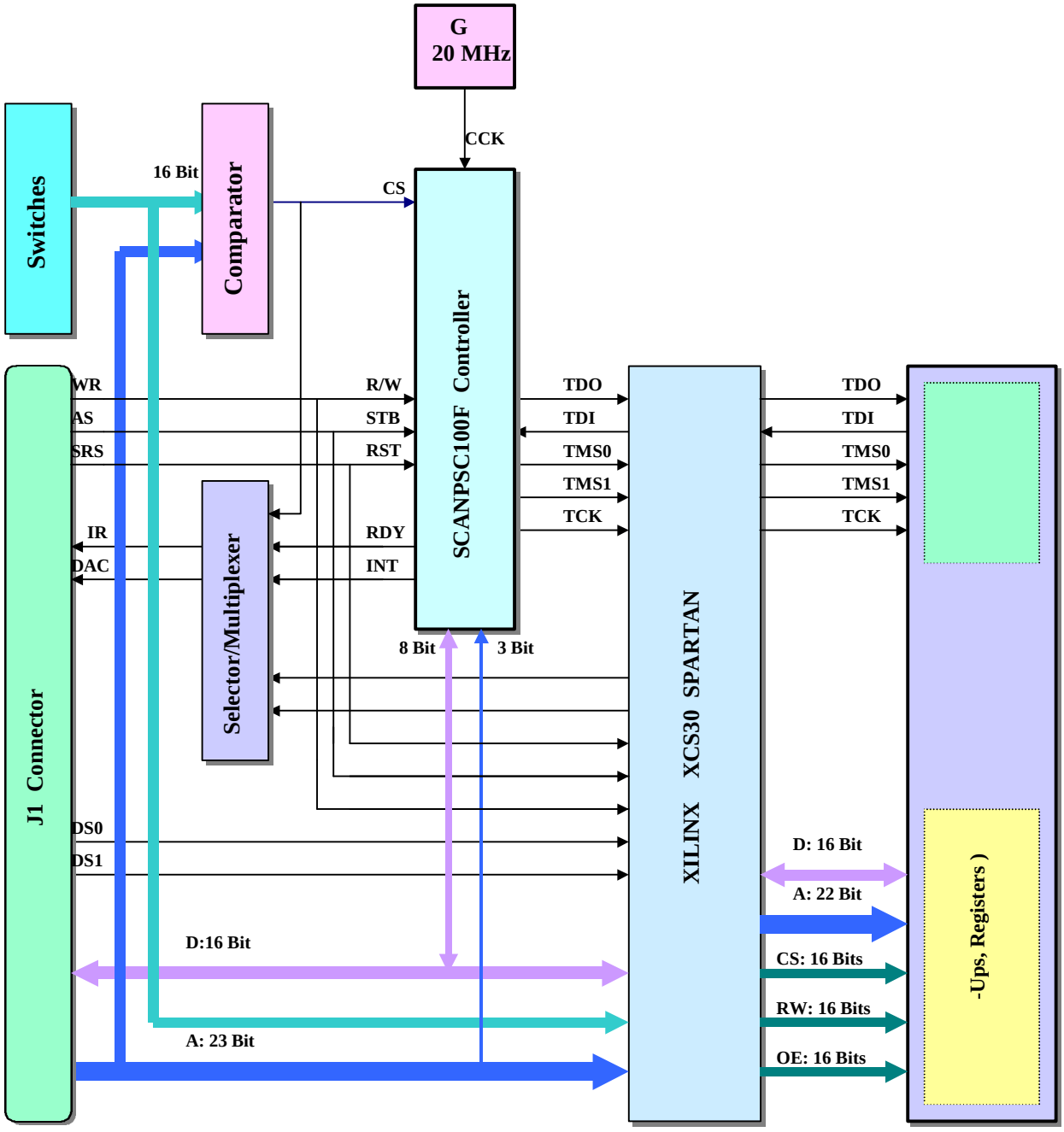
- Number of IOB: 168 out of 180 (93%)
- Maximum frequency: 56.883MHz
- Cost: $93.05

Extrapolation Unit / Global FIFO:

XCV400-6BG560C (speed grade = 6)

Number of slices: 2,006 out of 3,072 (65%)

- Number of IOB: 302 out of 316 (95.56%)
- Maximum frequency: 46.48MHz
- Cost: $665.00



VME and VME/JTAG Interface

Ghost-Busting in the TF

Algorithm developed to handle ghosts in the TF

- ME1 chambers only
- All possible η, φ combinations tried

Requires:

- 2 extra bits per 3 muons from SR
- Additional logic and interconnections in SP

Looks quite feasible

Method works only when both LCTs survive Port Card

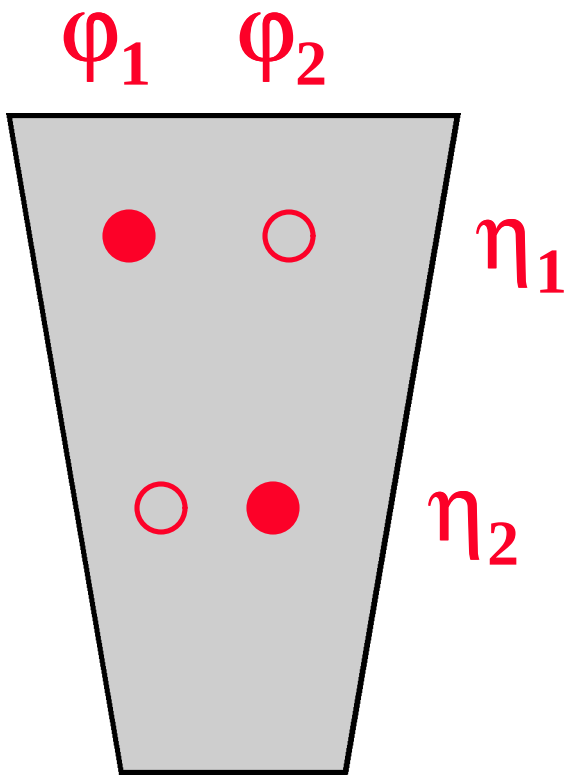
- $\leq$ 3 stubs / sector / station

Simulation shows that it works

- See Ming's talk

Ghost Hits

Try all combinations in Track-Finder by swapping η values



Plan for Sector Processor

Crate tests with SR, SR, CCB (and TMB, MPC) scheduled for June 1, 2000

SP design is proceeding well, should be able to make date

Still a lot of work to do, and software to write…