Track-Finder Test Results and VME Backplane R&D

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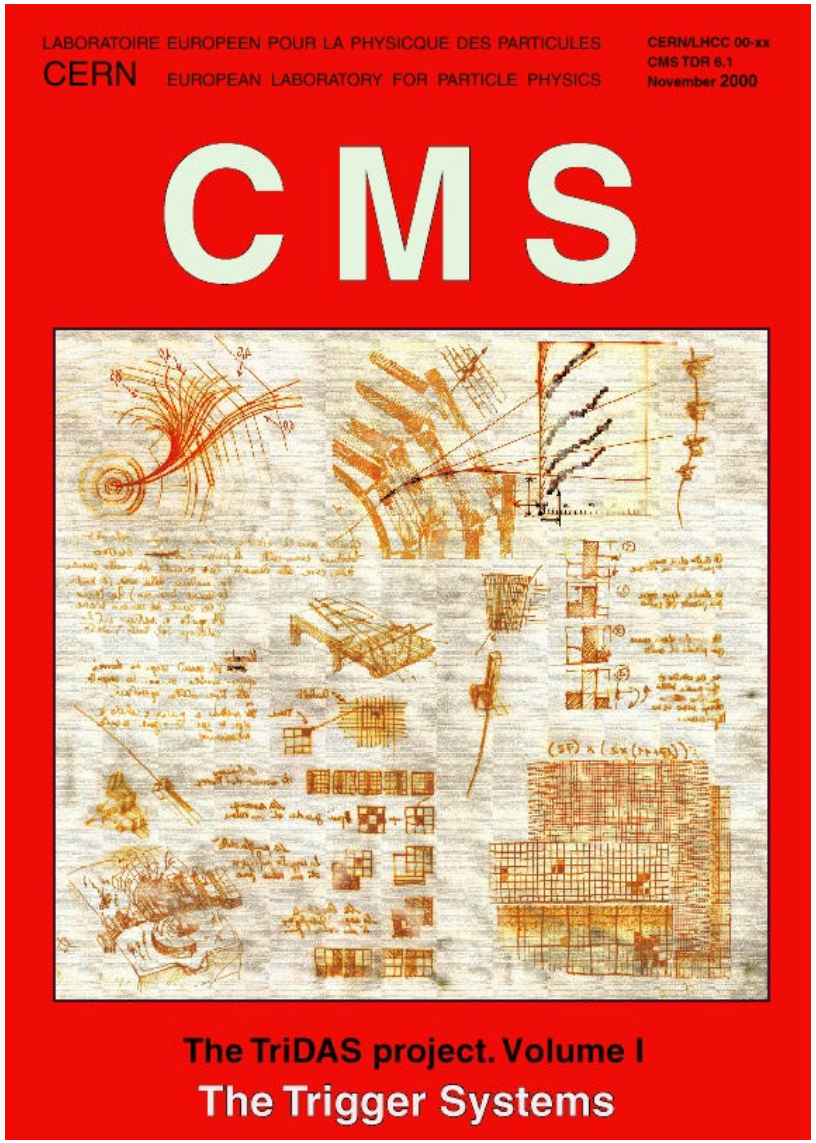
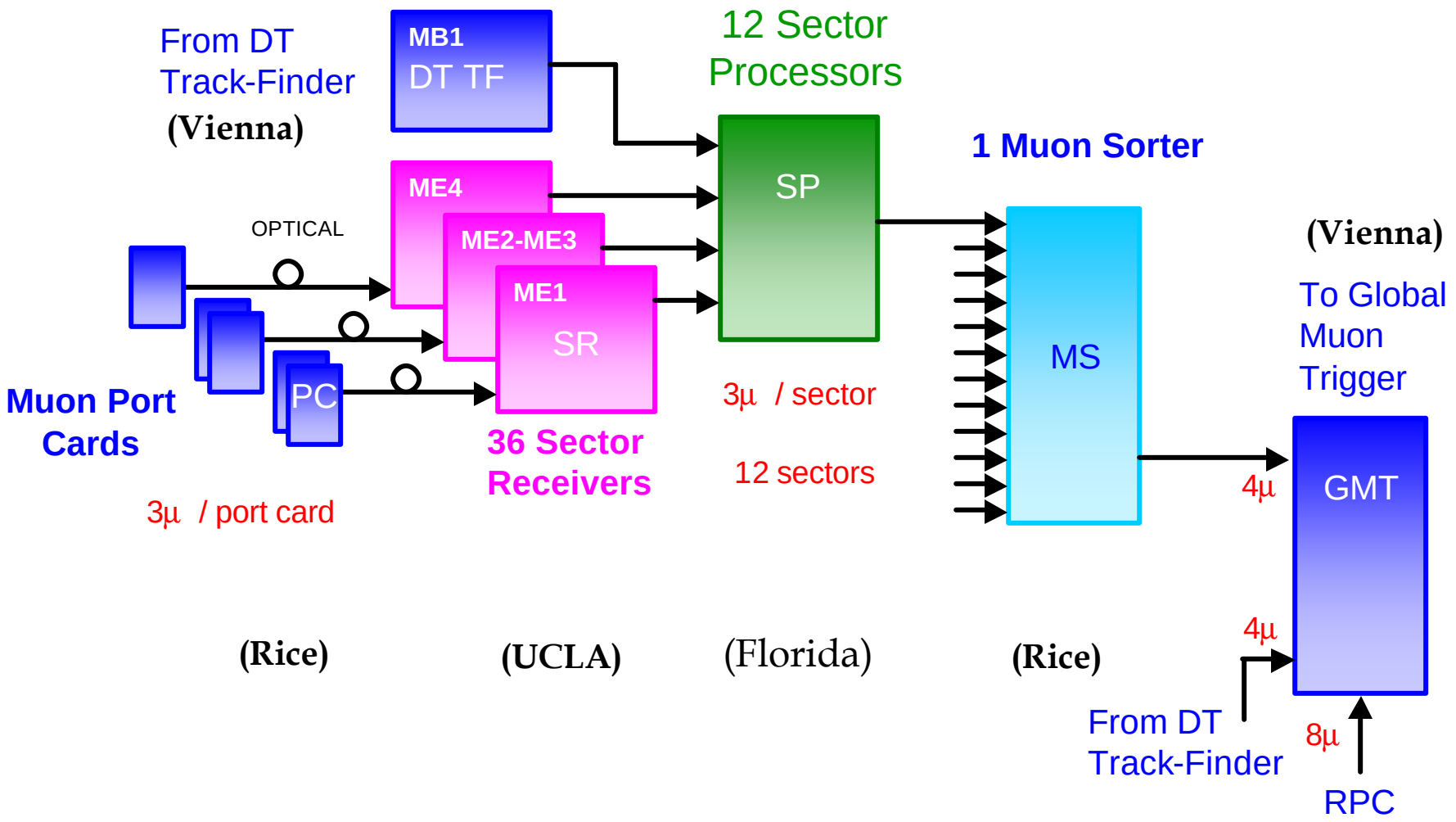
Technical Design Report



- Trigger TDR is completed!
- A large amount effort went not only into the 630 pages, but into CSC Track-Finder prototypes, tests, and simulations
- Latest test results and R&D reported in this talk
- Simulation results reported in software session

Level-1 Trigger Architecture



Tests of Current Prototypes

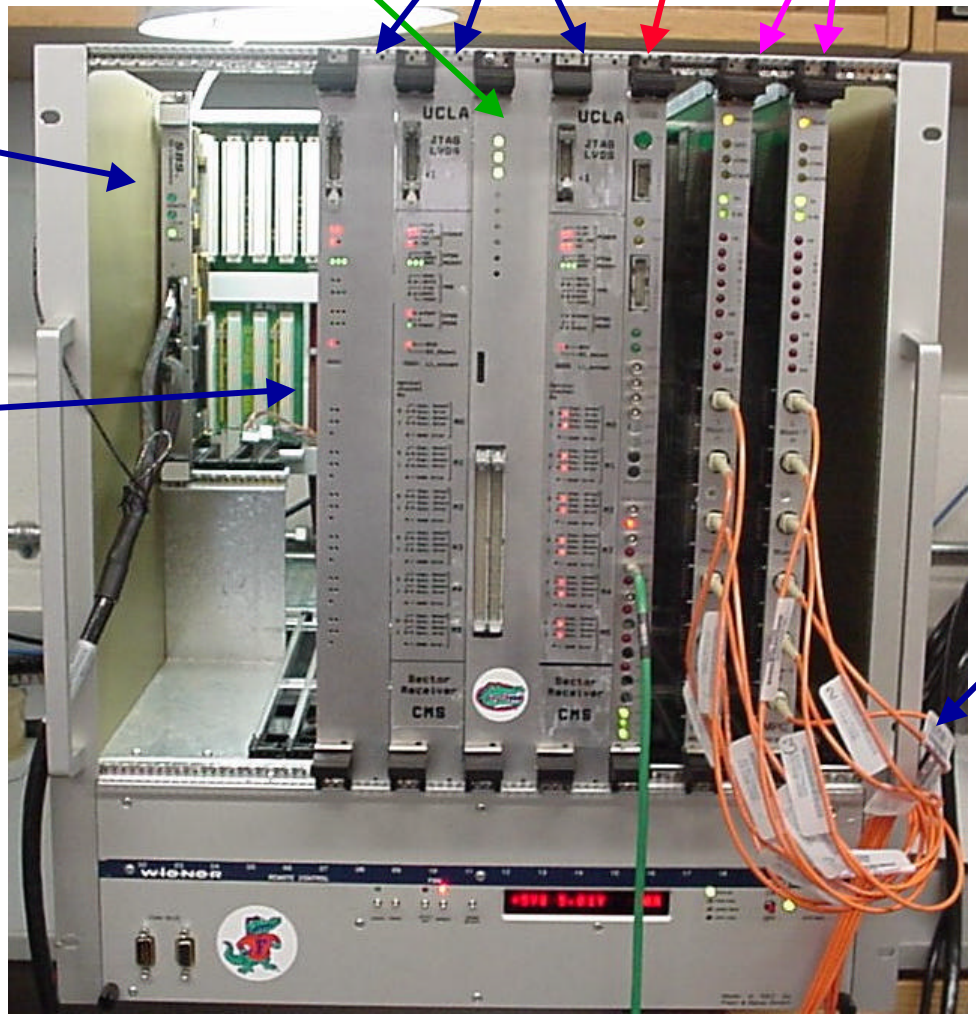
Prototypes of all Track-Finder components (except the CSC Muon Sorter) have been constructed:

- Sector Processor: UFlorida
- Sector Receiver: UCLA
- Muon Port Card: Rice
- Clock and Control Board: Rice
- Channel-Link backplane: UFlorida

All boards were completed in July

Since the last CMS week and EMU meeting, we have focused on completing integration tests of the complete system

Track-Finder Crate Tests



Test Results: Sector Processor

VME Interface

- All LUTs and FPGA programs downloaded in less than 30s through SBS Bit3 PCI to VME interface
- JTAG serialized on board @ 25 MHz

Functionality

- Internal dynamic test @ 40 MHz works with 100% agreement with ORCA simulation
  - 180K single muons (and 60K triple muons)
  - Internal FIFOs are 256 b.x. deep
- Latency is 15 b.x. (not including Channel-Link input)
- Firmware updated to latest algorithms for Trigger TDR
  - Some subtle logic errors discovered and fixed in HW
- Plan to test even larger data samples (and random data) to look for any rare errors

Test Results: Sector Receiver

Functionality

- Three boards built and tested
- Internal dynamic test @ 40 MHz works with ORCA data and pseudo-random data
  - Tested 30K cycles of 256 random events
- Some rare (10^{-6}) errors encountered and under study
- One board with slower SRAM (10ns vs. 8ns) works fine even with 2 memories cascaded with 25 ns clock
- Emulation software is similar to ORCA, but not same code
  - Although LUT contents were generated from ORCA

System Tests Done in Last Month

Port Card ® Sector Receiver

- ➔ MPC and SR communicate via HP GLinks and optical fiber
- ➔ Data successfully sent from input of one MPC, through 100m of optical cables, to output of SR
- ➔ 1.6M random events processed with no errors

Sector Receiver ® Sector Processor

- ➔ SR and SP communicate via Channel-Link backplane
- ➔ Data successfully sent from input of one SR, through custom backplane, into the SP
  - Some errors encountered from unmasked inputs, but tracks were reconstructed correctly from the SR input
- ➔ Successfully sent data from three SRs connected to the SP to emulate an entire trigger sector

System Tests (Continued)

Port Card ® Sector Receiver ® Sector Processor

- ➔ Successfully sent data from the input of two MPCs (representing ME2 and ME3), through one SR, and reconstructed tracks correctly in the SP
- ➔ Complete chain test

The Clock and Control Board prototype coordinated these tests:

- ➔ Distributed clock and control signals with programmable delays
- ➔ Sent BC0 to initiate tests

Lots of software had to be developed (and coordinated between institutes) for these tests to happen

Future Plans: Backplane

We plan to replace Channel-Link transmission as much as possible from the CSC trigger path because of its long latency (~3.5 b.x.)

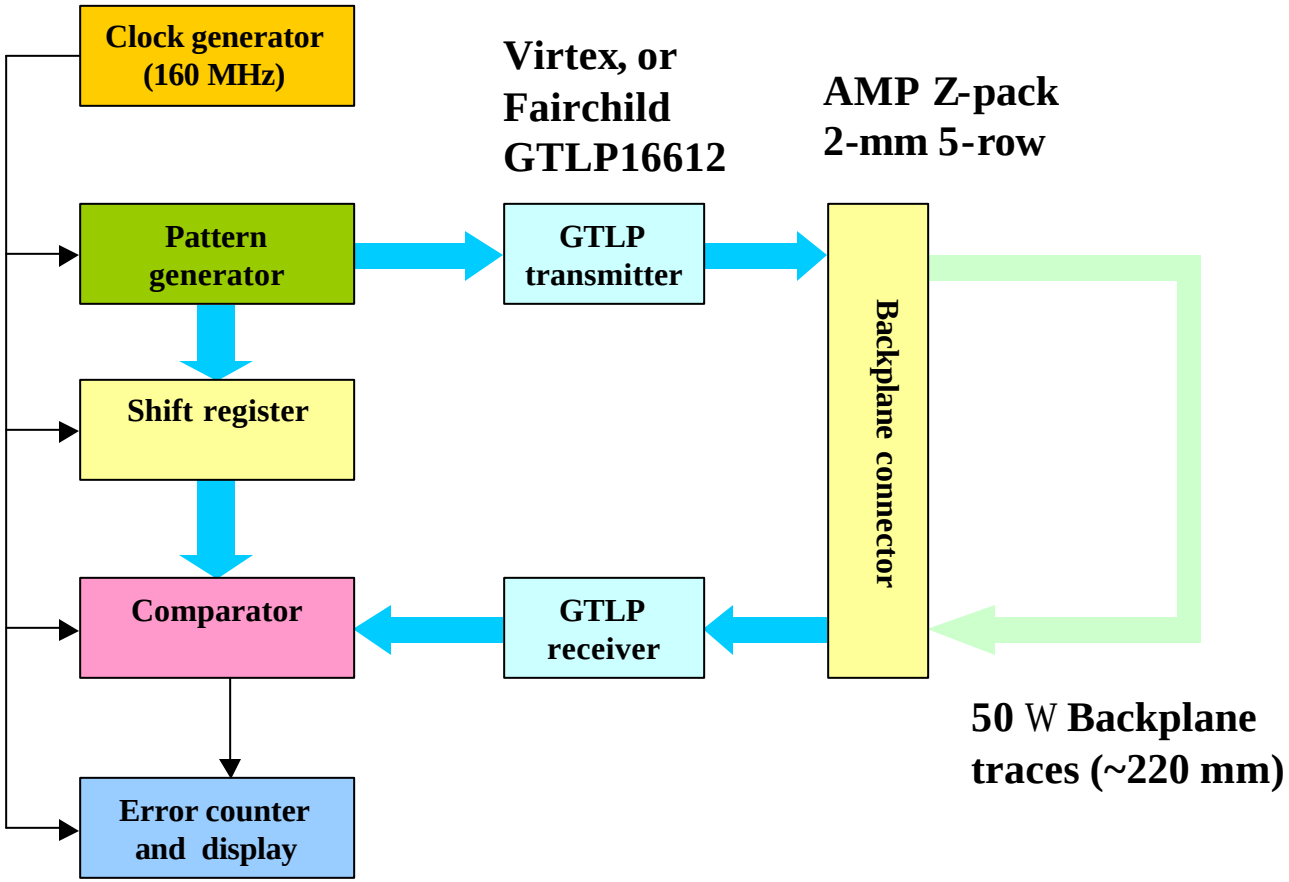
- In particular, for the custom point-to-point backplane in the Track-Finder crate and the front-end peripheral crates

Florida proposal is to use GTLP at 80 MHz

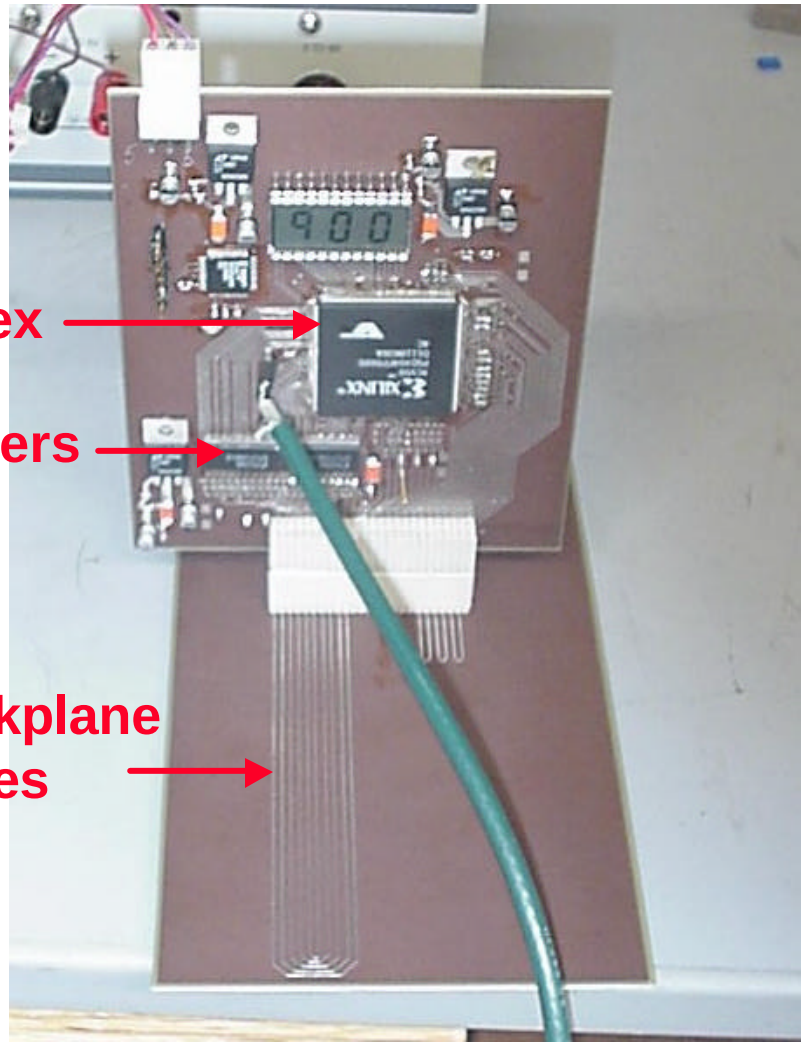
- Doubled frequency achieves 2´ signal reduction (vs. 3´ from Channel-Link)
- Can be bussed (although we plan point-to-point)
- No differential signals (fewer traces)
- Can be driven by Xilinx Virtex I/O directly, or from driver chips by Fairchild and TI

Prototype backplane successfully tested in Florida

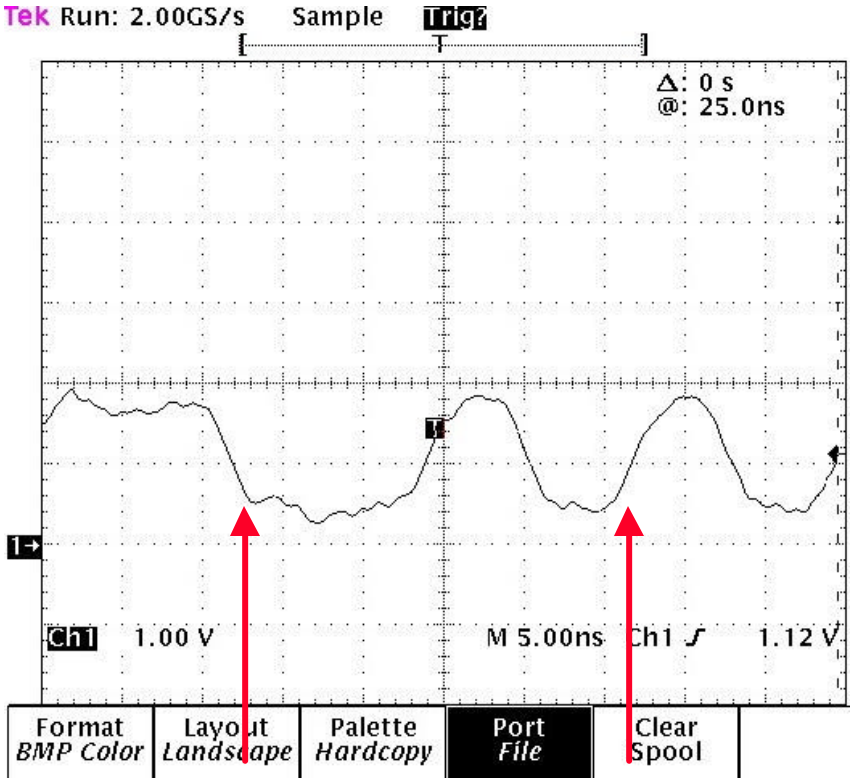
GTLP Test Fixture



GTLP Backplane Tests



Alternating and random patterns driven up to 160 MHz with no errors



80 MHz signal

160 MHz signal

Conclusions

GTLP backplane technology works well, ready for peripheral crate design

Prototype tests were a success (but a lot of work)

It was a useful exercise to commission a crate of trigger electronics

- ➔ Validates the trigger architecture
- ➔ Gives us some idea of what to expect when we commission the real system
- ➔ Learned of some (solvable) incompatibilities
  - Different VME addressing conventions
  - Different patterns and sorting logic than expected
- ➔ Provides guidance on how to improve future boards
  - Additional VME registers to set board functions or to spy on intermediate data
  - A real DAQ readout path for continuous running (i.e. circular buffer with DDU connection)
    - In particular, can the TF trigger data "piggy-back" on EMU data?