Status of the Track-Finder

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HW Tests
Future Plans
Tests of Current Prototypes

In preparation of the Level-1 TDR, all trigger prototypes must be tested by end of September

- **Sector Processor:** UFlorida
- **Sector Receiver:** UCLA
- **Muon Port Card:** Rice
- **Clock and Control Board:** Rice
- **ChannelLink backplane:** UFlorida

All boards were completed in July

Crate tests of the boards (the TriDAS “testbeam”) followed and are still on-going

- Have shifted from single board tests to integration tests
Level-1 Trigger Architecture

From DT Track-Finder (Vienna)

Muon Port Cards
3μ / port card

ME1
SR
36 Sector Receivers

ME2-ME3
ME4
MB1
DT TF

12 Sector Processors
3μ / sector
12 sectors

1 Muon Sorter

To Global Muon Trigger

GMT
4μ

RPC

4μ
From DT Track-Finder

8μ

(UCLA)

(Rice)

(Florida)

From DT Track-Finder

(Rice)

EMU Meeting, September 2000
Darin Acosta
Muon Track-Finding

- CSC system divided into 12 sectors (6 per endcap)
- Link trigger primitives into 3D tracks
- Select best 3 tracks per sector
- Assign $p_T$, $\phi$, and $\eta$ using data from up to 3 stations
- Send 4 highest quality candidates to Global L1
Track-Finding Logic in Sector Processor

From Backplane

Bunch Crossing Analyzer

Extrapolation Units

EU1-2
EU1-3
EU2-3
EU2-4
EU3-4
EU MB1-2

EU1 – E2
EU2 – E4

Track Assembler Units

TAU1
TAU2
TAU3

Final Sorter

FSU

Assignment Unit

AU

FIFO
MUX

To Front panel

EMU Meeting, September 2000
Sector Processor Prototype

Final Selection Unit
XCV150BG352

Extrapolation Units
XCV400BG560

Assignment Units
XCV50BG256 &
2M x 8 SRAM

Track Assemblers
256k x 16 SRAM

Bunch Crossing
Analyzer
XCV50BG256

12 layers
10K vias
Sector Receiver Prototype

Optical Receivers and HP Glinks

SRAM LUTs

Front FPGAs

Back FPGAs
Track-Finder Crate Test

Bit3
VME Interface
Custom backplane

SP  SR  CCB
UF Test Software on Win95

JAVA GUI to call command line programs

programs to load FPGAs and LUTs through Bit3 VME interface (JTAG runs at 25 MHz on board)

Test software and subset of ORCA simulation to compare hardware and simulation results

Should be portable to UNIX
Test Results: Sector Processor

Front half of logic (Extrapolation, Track Assembly) works flawlessly with 100% agreement with ORCA simulation

- 180K single muon events, 60K triple muon events, generated from CMSIM
- Usual bug fixes to software and firmware took place

Dynamic tests of front logic determined that maximum clock frequency is 63 MHz

- FIFOs on input and output hold 256 events

Back half of logic is currently under test

- Sorter logic and $P_T$ assignment seem to be working correctly - a few discrepancies under investigation

Overall latency is 15 b.x. (w/o ChannelLink)

- Already can reduce to 14 b.x.
Test Results: MPC & Sector Receiver

Muon Port Card:
- Plug-in mezzanine card (with low profile connectors) for sorter FPGA works
- Basic sorter logic verified
- Optical communication to Sector Receiver verified

Sector Receiver:
- Static tests of FPGA and LUTs verified
- Dynamic test from Back FPGAs of one SR (through ChannelLink backplane) to SP verified with UF software
- Dynamic test of SR logic still on-going using UCLA software

Dynamic test of complete system planned

Merge of UF and UCLA software required
Lessons from Construction & Tests

It is possible to work with ball-grid arrays (BGAs) on large 9U VME boards.

It is possible to remove and replace BGAs
  ➔ SR and SP each had one chip replaced.

Not all board assembly companies are equal!
  ➔ Conquest in Orlando is out.
  ➔ Bat PC in San Jose is in.

Channel Link chips fail when connected to Xilinx Virtex I/O pins
  ➔ Sector Receiver had many chips die.
  ➔ Probably related to over/undershoot.
  ➔ Slow risetime configuration of Virtex I/O pin is okay.
  ➔ Connection to buffer chips is okay.

And... opinions on software outweighed all opinions on hardware!
Future Plans: SR/SP

Current technology will allow us to merge all 17 FPGAs of prototype Sector Processor into just one:

- Xilinx Virtex XCV2000E (~2.5M gates) available now
- or Virtex 2, available soon

This opens the possibility of merging the Sector Processor and Sector Receivers onto a single board:

- Would allow for a single crate Track-Finder (currently 6)
- Reduces latency
- No Channel Link connection between SR and SP
- No cable to Muon Sorter

Depends on new optical link technology to reduce connections from peripheral crate:

- 2.5 Gbit links or parallel optical cables
Optical Solution 1

- 1 Optical Connection per each track segment
- Completely tested by Texas Instruments (optical modules + ser/des chips only)
- 15 connections per SR/SP module (3 connections x 5 MPC)
- Low power consumption:
  - 2.2W MPC (3 links)
  - 11W SR/SP (15 links)
- Latency ~ 0.5Bx for Tx and 1.5Bx for Rx
• 1 Optical Connection per each MPC
• 5 connections per SR/SP module (1 connection x 5 MPC)
• Low power consumption:
  2W MPC (1 link) and  9W SR/SP (5 links)
• Latency ~ 1Bx for Tx and 2Bx for Rx
• LVDS to PECL conversion must be tested
Possible Board Layout

Preliminary layout of SR/SP module (2.5Gb/s link option)

- Low power consumption: ~ 38.5W per 9U VME card
- Latency: ~ 15Bx
- SP structure is fully programmable
- Cost reduction: 1 SR/SP module instead of 3 SR and 1 SP
- 1 SR/SP module per 60° sector
Possible Crate Layout

Track-Finder crate (2.5Gbits/s optical links)

- Total latency: ~ 20Bx (from input of SR/SP card to output of CCB/MS card)
- Power consumption: ~ 500W per crate
- 17 optical connections per SR/SP card (15 - from endcap, 2 – from/to barrel)
- Custom backplane for SR/SPs < > CCB/MS connection
### Possible Latency Savings

<table>
<thead>
<tr>
<th>Description</th>
<th>Bx</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR optical receiving and synchronization</td>
<td>2</td>
</tr>
<tr>
<td>SR Front FPGAs and Lookups</td>
<td>2</td>
</tr>
<tr>
<td>SR to SP Channel Link transmission over short backplane</td>
<td>4</td>
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<tr>
<td>SP processing</td>
<td>15</td>
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<tr>
<td>SP to Muon Sorter transmission over 5m cable</td>
<td>2.5</td>
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<tr>
<td>Muon Sorter processing</td>
<td>5</td>
</tr>
<tr>
<td>Muon Sorter to GMT transmission over 11m cable</td>
<td>3.5</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>34</strong></td>
</tr>
</tbody>
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Prototype 1 (current)

<table>
<thead>
<tr>
<th>Description</th>
<th>Bx</th>
</tr>
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<tbody>
<tr>
<td>SR/SP optical receiving and synchronization</td>
<td>2</td>
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<tr>
<td>SR/SP Front FPGAs and Lookups</td>
<td>3</td>
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<tr>
<td>-</td>
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<tr>
<td>SP processing</td>
<td>10</td>
</tr>
<tr>
<td>SP to Muon Sorter transmission over short backplane</td>
<td>2</td>
</tr>
<tr>
<td>Muon Sorter processing</td>
<td>3</td>
</tr>
<tr>
<td>Muon Sorter to GMT transmission over 11m cable</td>
<td>3.5</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>23.5</strong></td>
</tr>
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</table>

Prototype 2 (merged)
Recently discovered that Channel Link chips have unacceptably long latency (~3.5 clocks)

- Rice, UCLA, UF have verified this
- e.g. SR → SP test had 4 clock delay

Need a replacement technology ASAP for peripheral crate and Track-Finder crate backplanes

- Or run Channel Link at 80 MHz as Bristol group?

UF proposal (Madorsky) is to use GTLP at 80 MHz

- Doubled frequency achieves 2× signal reduction (vs. 3× from ChannelLink)
- Can be bussed.
- No differential signals (fewer traces)

Prototype backplane will be tested in the next 3 months