CSC and Overlap Track Finder

TriDAS Progress Report
April 28, 1998

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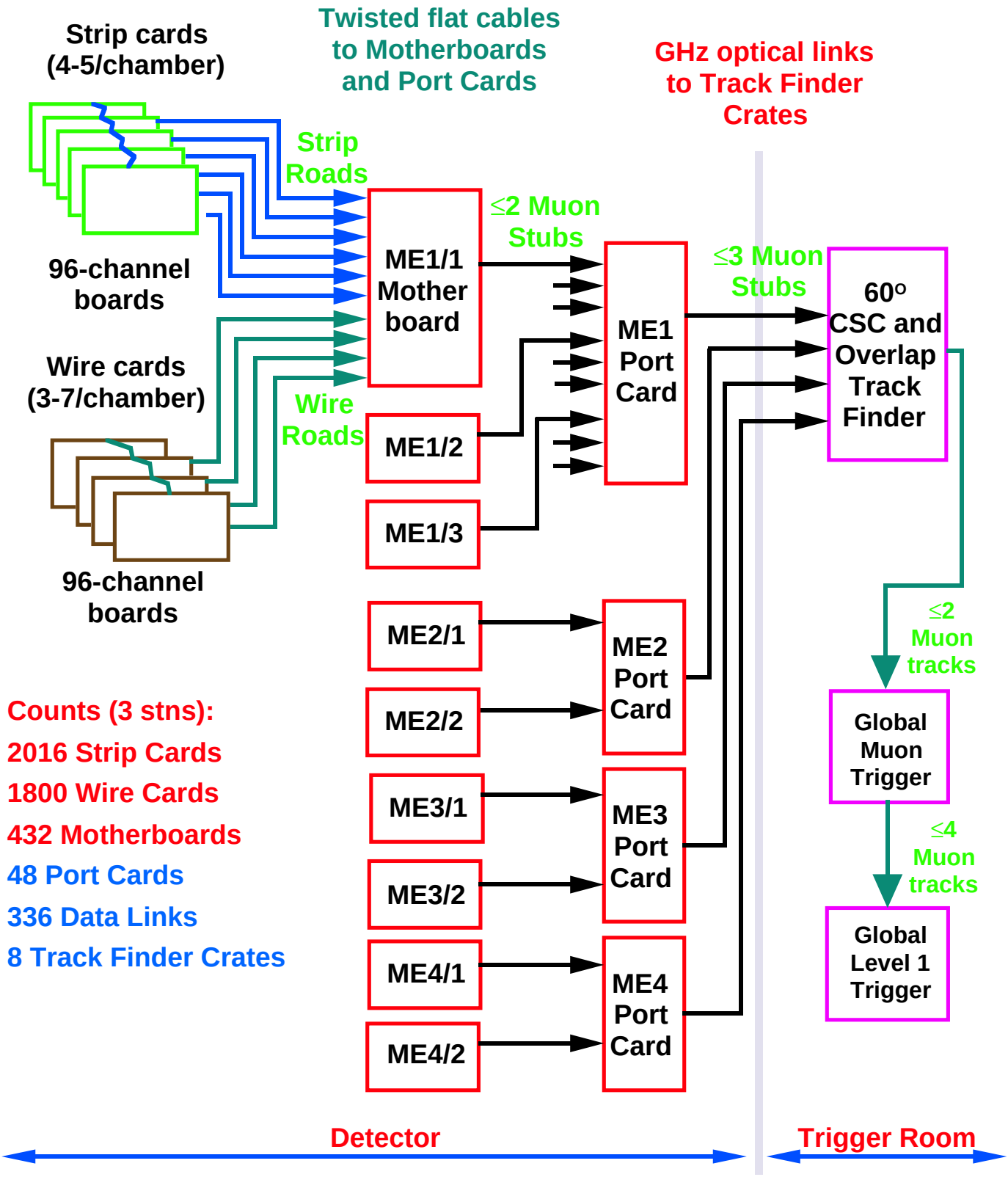
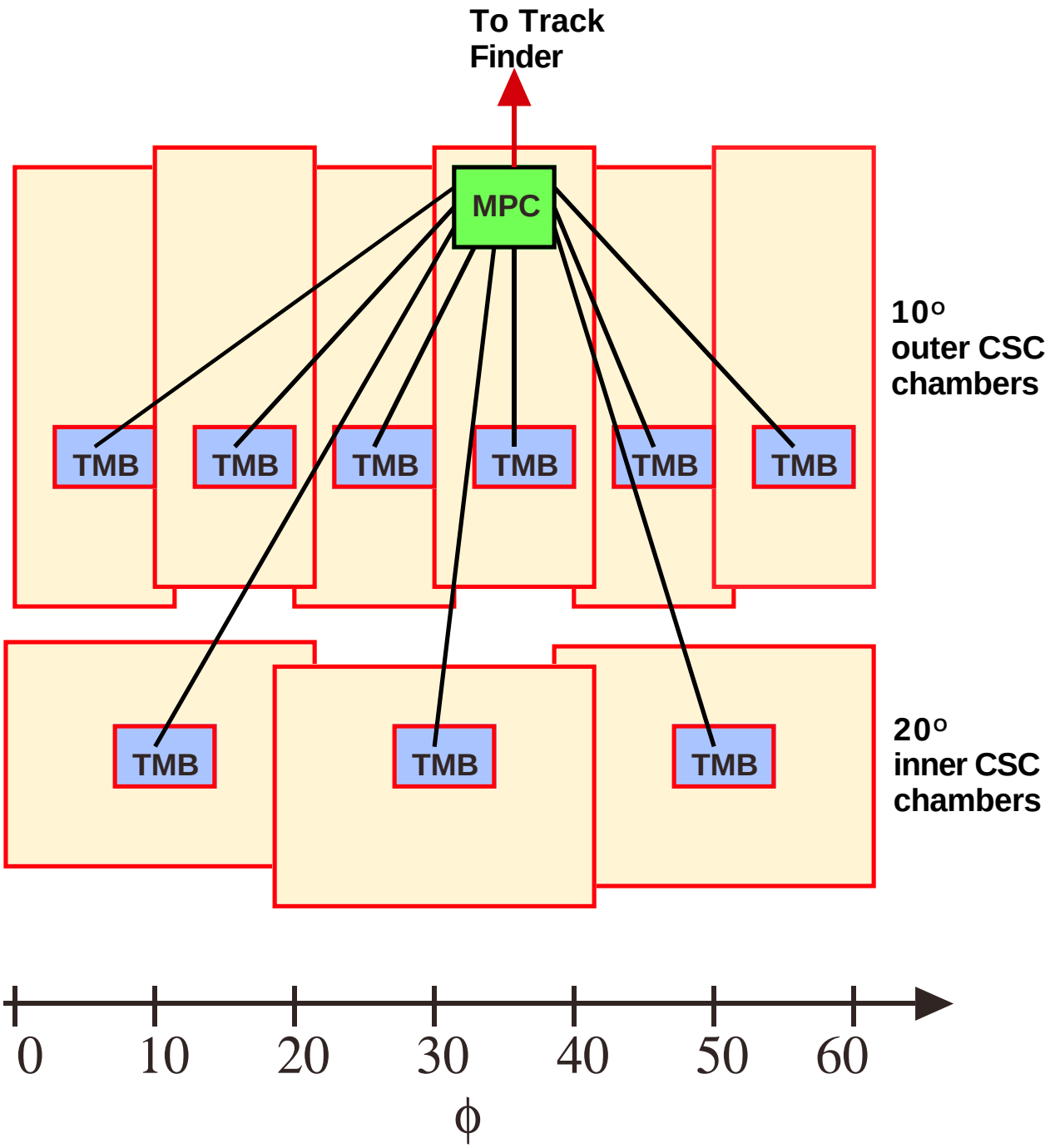
- System Re-Design
  - Rescoped to 3 stations
  - 60 degree CSC sectors
  - Data flow
  - Crate Arrangement
- Cost and Schedule

CSC Trigger Block Diagram

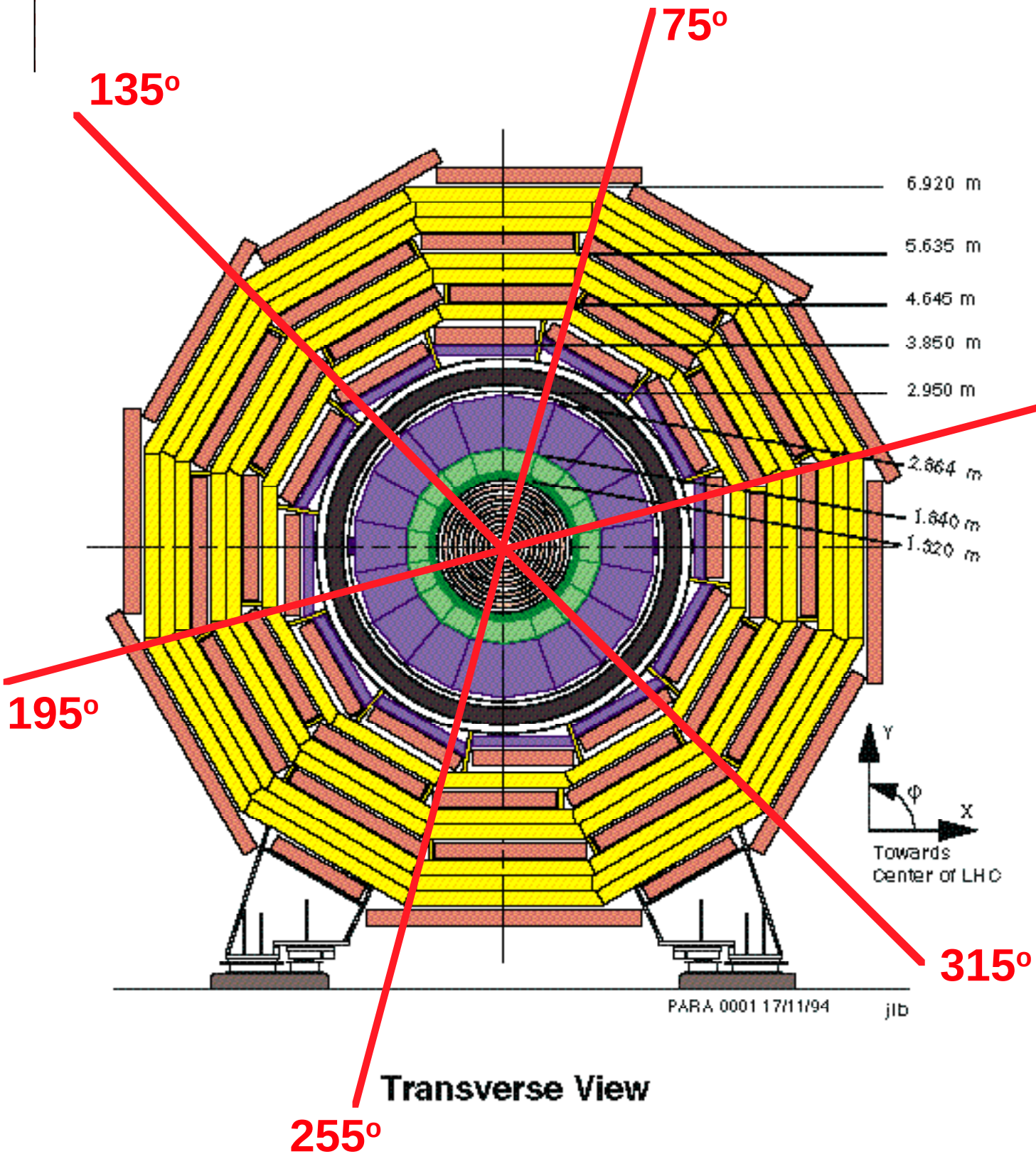


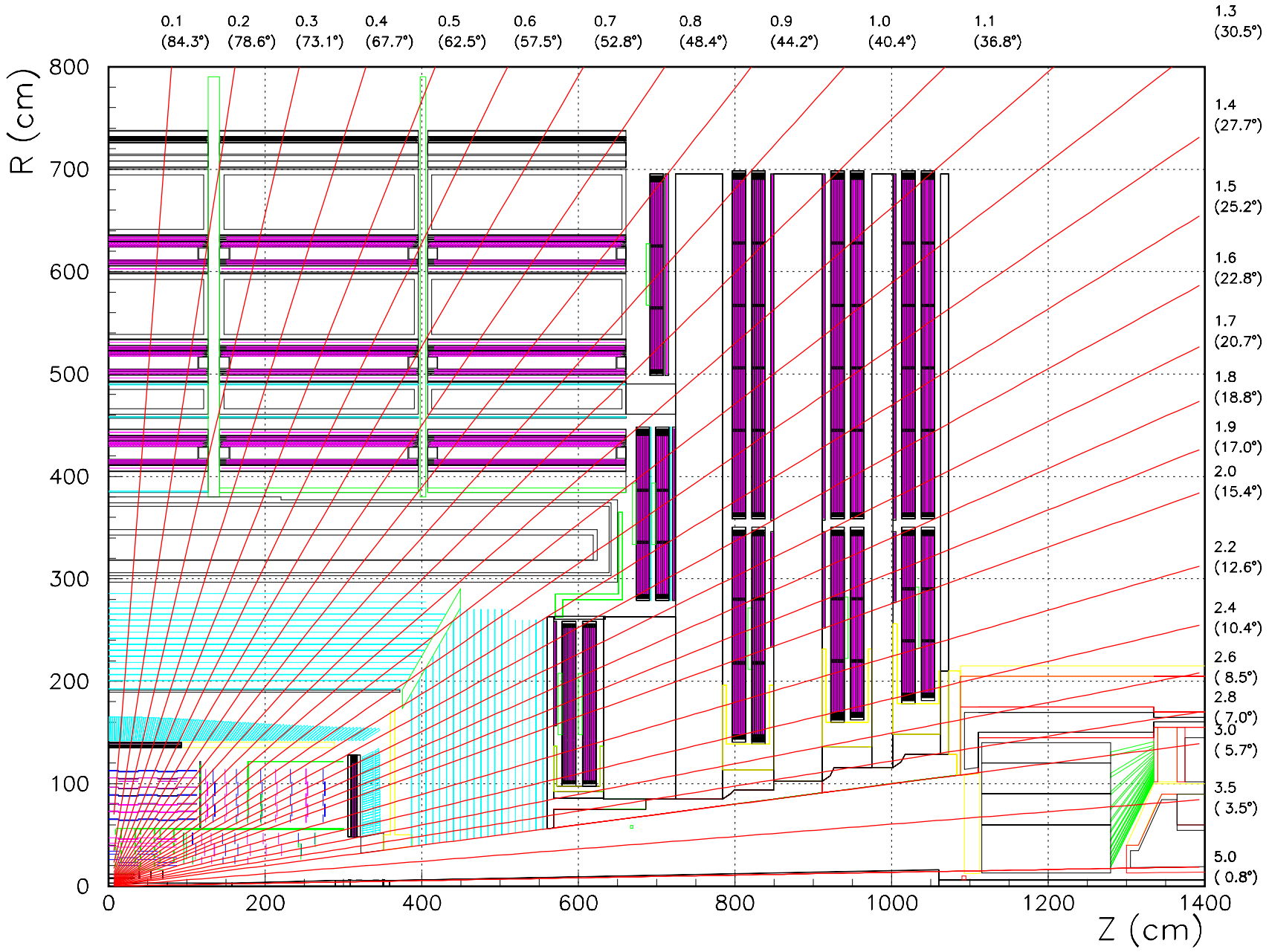
CSC Trigger Port Cards

TMB = Trigger MotherBoard
MPC = Port Card

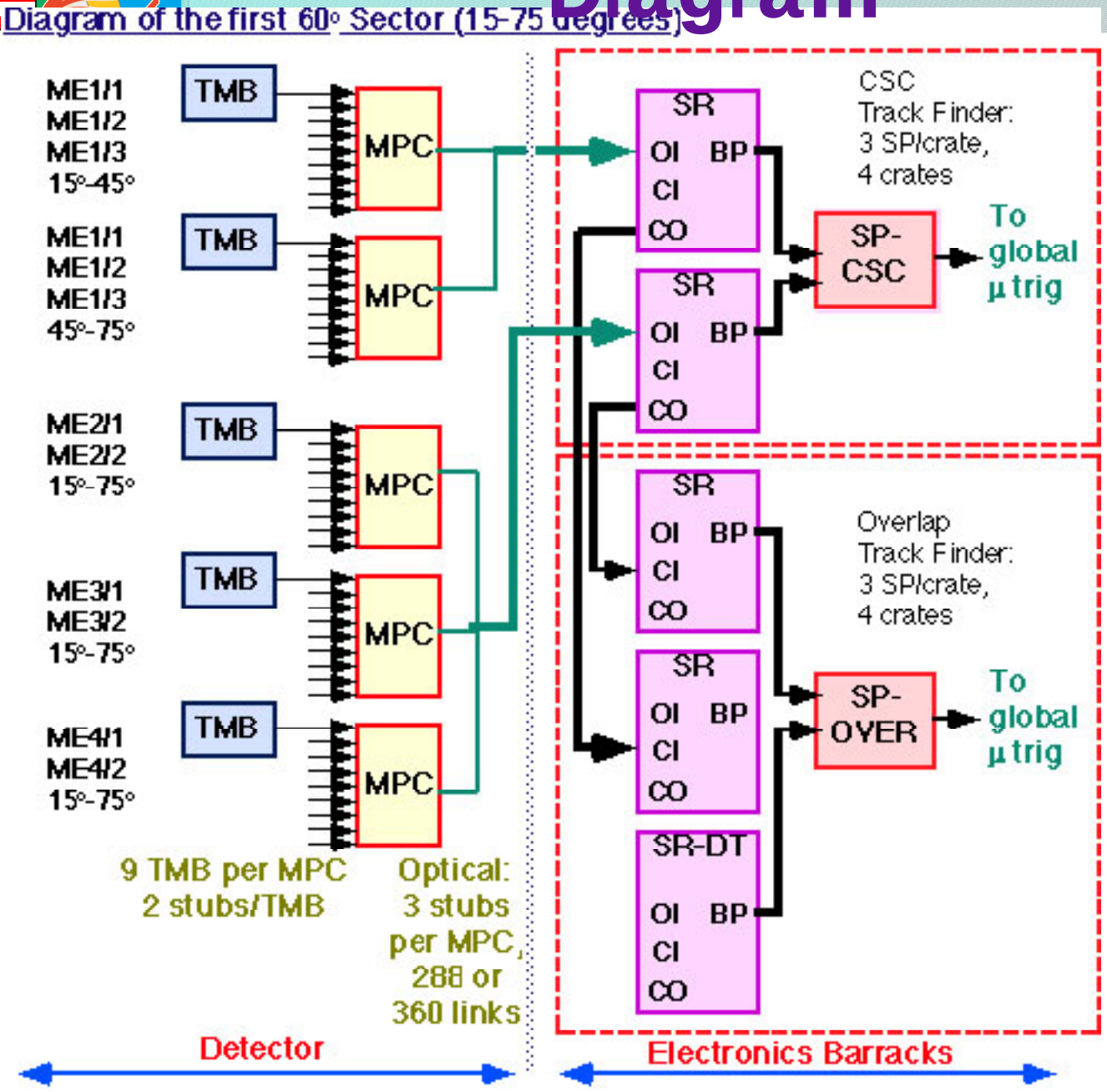


CMS Transverse View




0.1 (84.3°)
0.2 (78.6°)
0.3 (73.1°)
0.4 (67.7°)
0.5 (62.5°)
0.6 (57.5°)
0.7 (52.8°)
0.8 (48.4°)
0.9 (44.2°)
1.0 (40.4°)
1.1 (36.8°)
1.3 (30.5°)
1.4 (27.7°)
1.5 (25.2°)
1.6 (22.8°)
1.7 (20.7°)
1.8 (18.8°)
1.9 (17.0°)
2.0 (15.4°)
2.2 (12.6°)
2.4 (10.4°)
2.6 (8.5°)
2.8 (7.0°)
3.0 (5.7°)
3.5 (3.5°)
5.0 (0.8°)
R (cm)
0
100
200
300
400
500
600
700
800
Z (cm)
0
200
400
600
800
1000
1200
1400

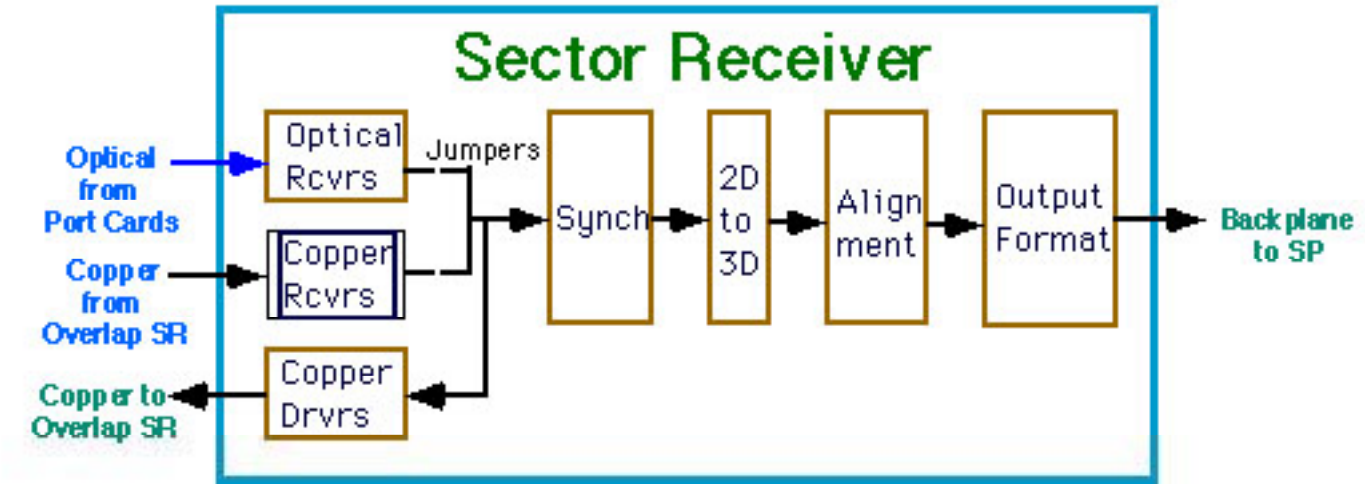
CSC & Overlap TF Block Diagram



Glossary and Part Count

TMB: Trigger Motherboards (432 or 540)
MPC: Muon Port Cards (48 or 60)
SR: Sector Receivers for CSC (24)
SR-DT: Sector Receivers for DT (12 or 24)
SP-CSC: Sector Processors for CSC region (12)
SP-Over: Sector Processors for Overlap region (12)
OI, CI, CO, BP: Optical in, copper in, copper out, backplane

Specific Functions of Sector Receiver



Block diagram

LCT content (from each MPC to SRC)

Signal	Bits
Half-Strip ID	5
Strip Left/Right Bend Angle	1
Strip Hi/Lo Pt Flag	1
Strip Pattern ID	8
Strip FEB Number	3
Strip Status	1
Wire Gang ID	4
Wire Pattern ID	7
Wire Status	1
Wire FEB Number	3
Wire BXN	8
Chamber ID	4
Total	46

Table 6

Data to be send from each SRC to SP

Data	Bits
Phi position	12
Rapidity	11
Local bend angle	6
Quality	3
Total	32

Sector Receiver Layout

Inputs/Outputs:

Transceivers and Glinks - 216 bits/xing requires 14 links

Copper: CSC to Overlap crate cables require 8 x 60-pin

Backplane: 3 192-pin Z-pack connectors

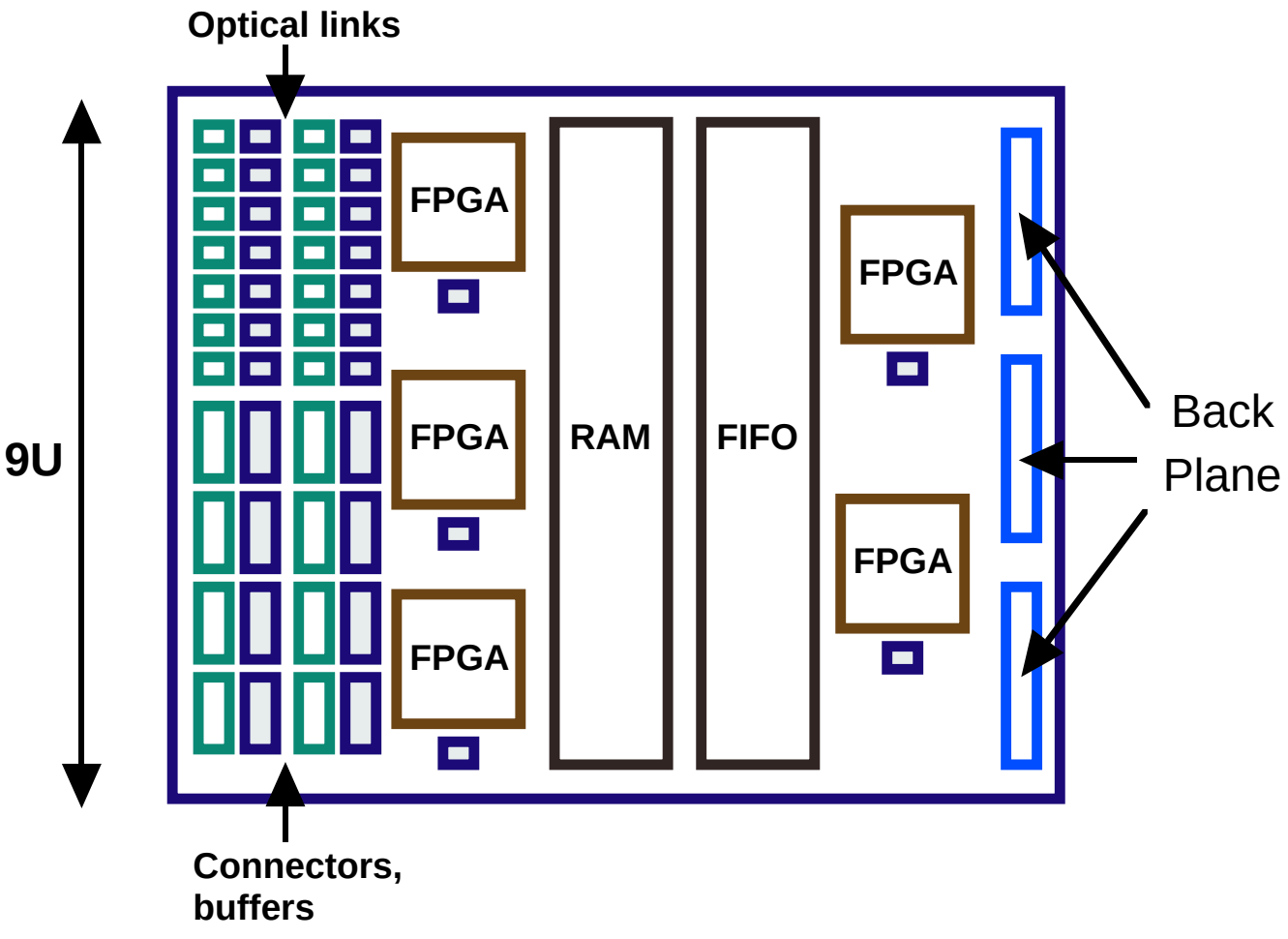
Processing:

Buffers for copper signals

FPGAs and Memory look-ups for main functionality:

- space and time alignment
- 2D to 3D stub conversion
- output formatting

plus configuration EPROMs and FIFOs for data storage



Preliminary Estimate of SR Latency

Input serial to parallel conversion and synchronization: 3

LUT conversion and alignment: 3 - 4

Output reformatting and buffering: 2 - 3

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8 - 10 b.x.

Sector Processor Layout

Inputs/Outputs:

Backplane inputs: 3 192-pin Z-pack connectors

Front panel outputs to Global mu: three 60-pin cables

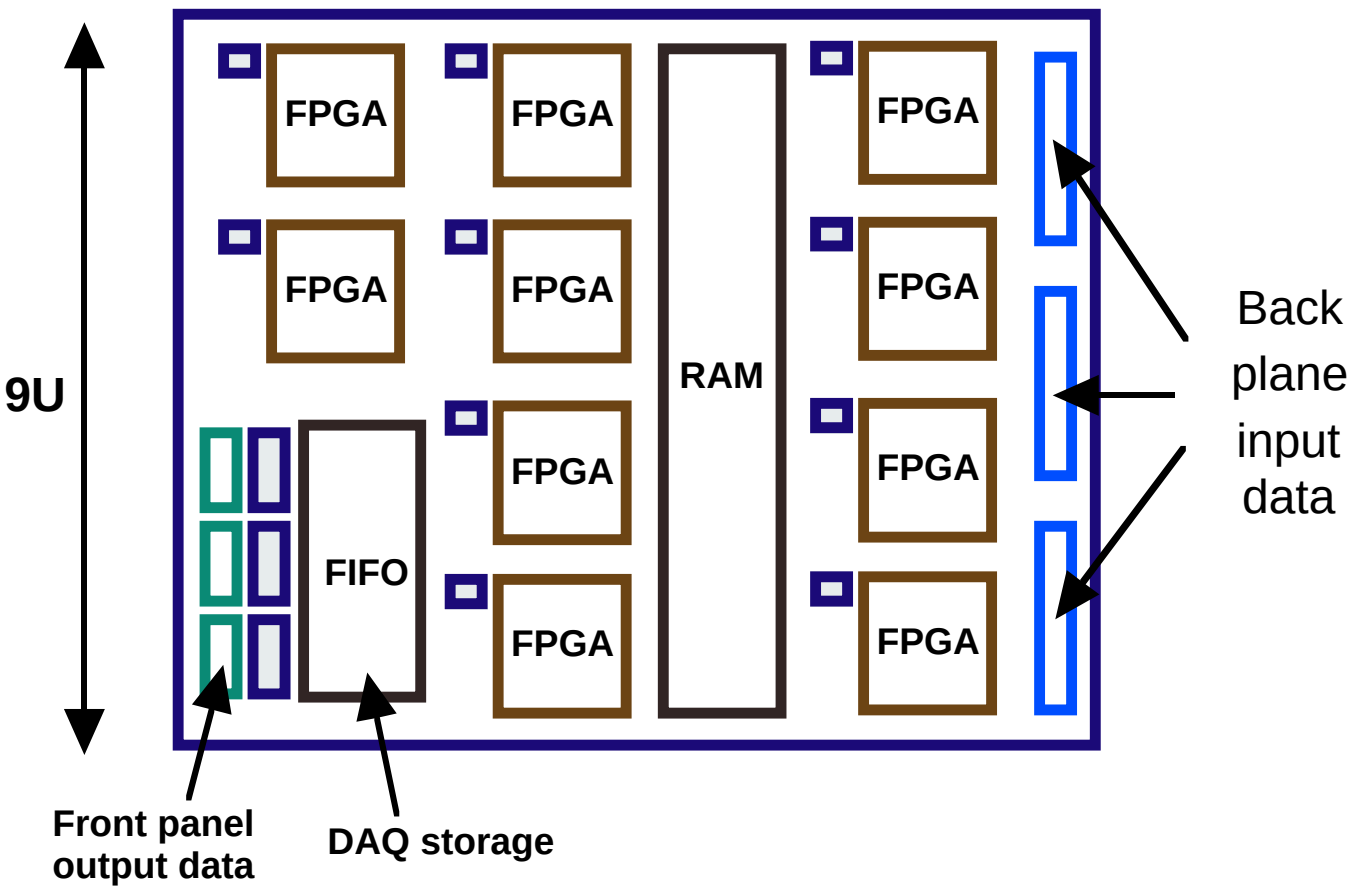
Processing:

FPGAs and Memory look-ups for main functionality:

- muon stub coincidence
- p_T lookup
- output formatting

Configuration EPROMs and FIFOs for data storage

Buffers for data to global muon trigger



Muon Track Finder Crates and Data Flow

180 degrees in ϕ per crate

Drift Tubes organized by wheel

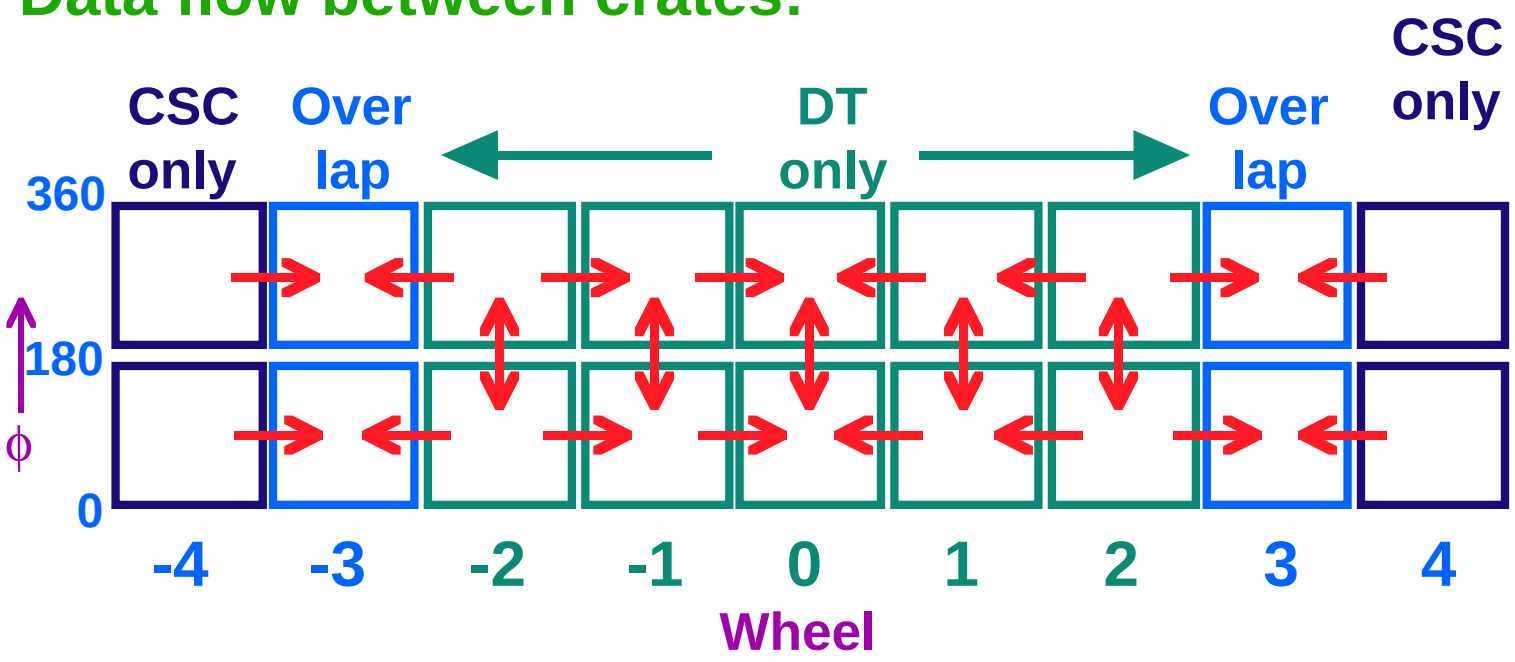
CSC and Overlap regions are extra "wheels"

CSC signals received in CSC-only racks

CSC and DT signals fanned out to Overlap racks

- **Endcap crates do not share data at ϕ boundaries**
  - bending is smaller in endcap region
  - chamber coverage is "seamless"
- **CSC-only racks send ME1,2,3 info. to overlap racks**

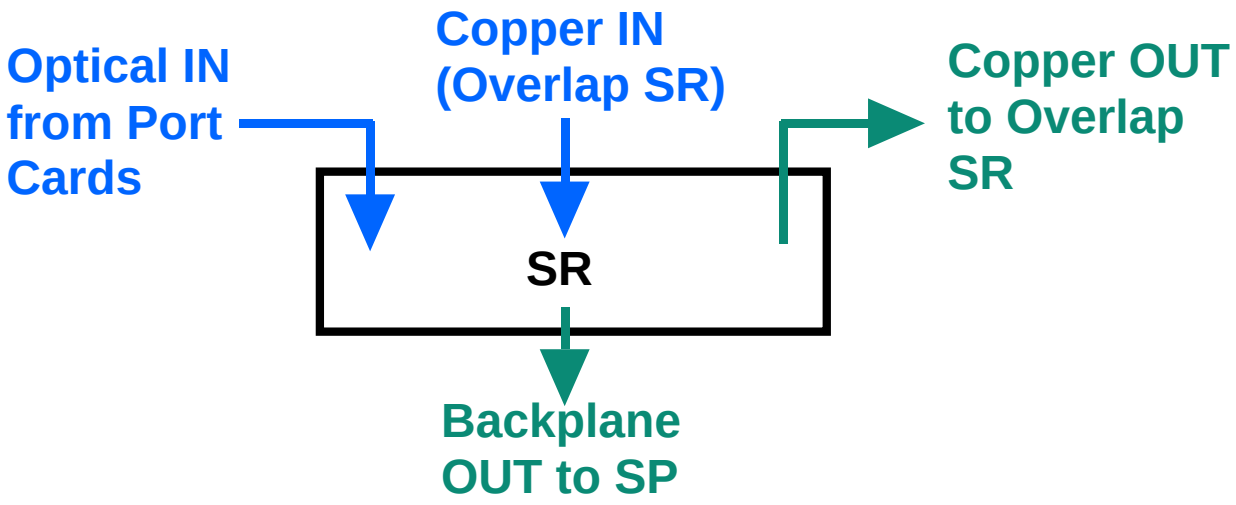
Data flow between crates:



CSC-only Track Finder Crate

Sector Receiver data flow:

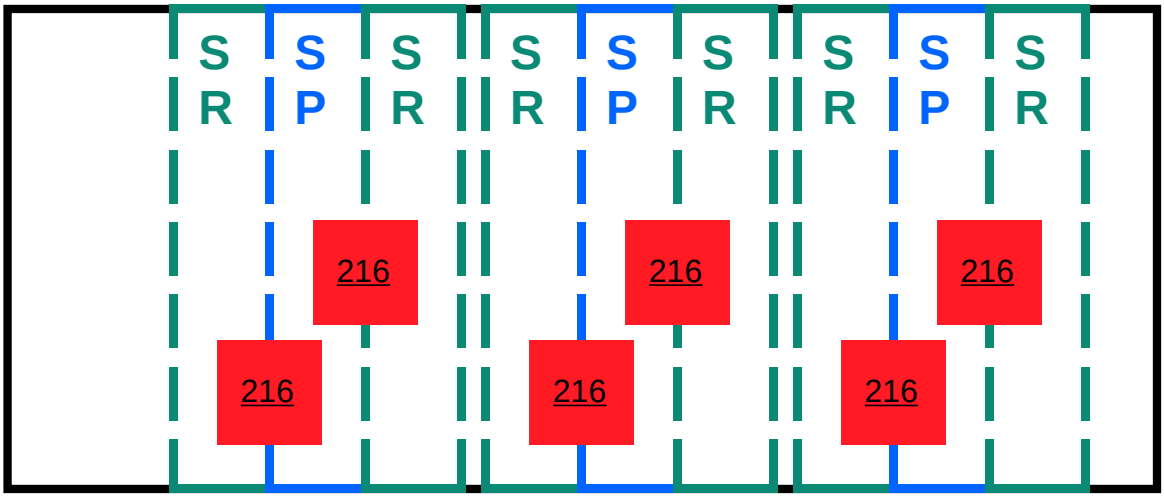
Each SR receives 2 ME stations, 12 optical links
3 stubs per Port Card
37 bits per muon stub in, 32 bits out
ME1,2,3 data repeated on copper to overlap crate



CSC crate backplane data flow:

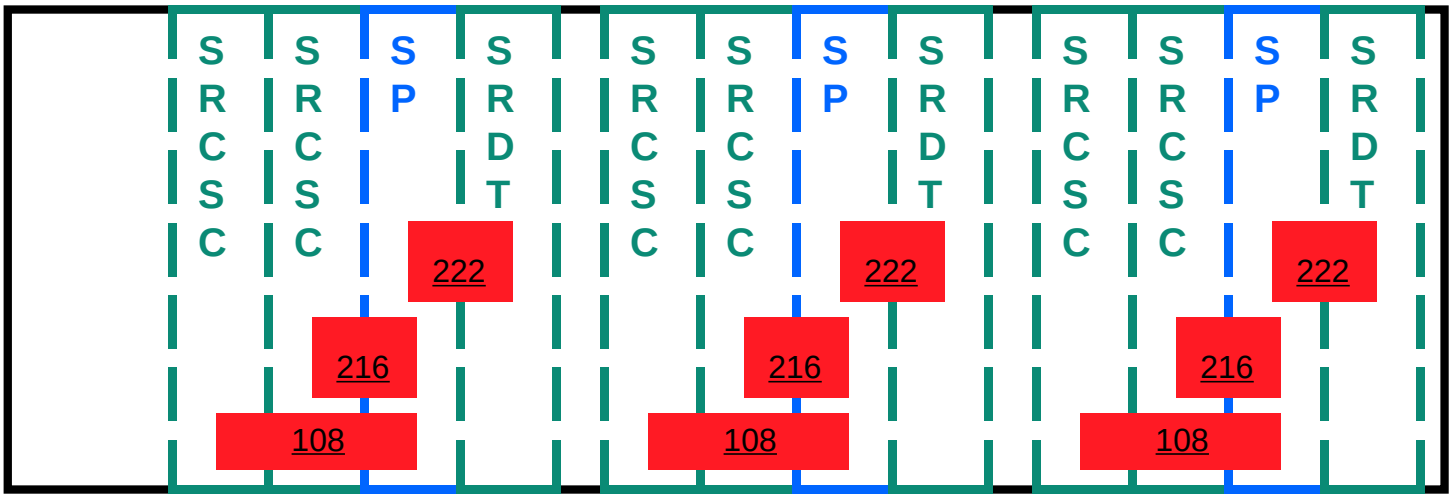
High-density Z-pack connectors: 192 pins per 96mm
Two connectors for 3-station operation, or three for 4 stations

Pin count, 4 stations, including 12% grounds:



Overlap Track Finder Crate

- **Two CSC and one DT Sector Receivers per SP-OVER**
  - **DT signals repeated on copper from Wheel +-2?**
- **32 bits/stub for CSC, 22 bits/stub for DT**
- **Assume 3 stubs/sector/station for CSC and DT**
- **CSC crate backplane data flow:**
  - High-density Z-pack connectors: 192 pins per 96mm
  - Three connectors required
  - **Small** amount of backplane space left for readout bus
  - Consider using front panel connections



Track Finder Data I/O Counts

CSC/Overlap Sector Receivers: 636

- 222 optical inputs,
- 222 copper in/out,
- 192 backplane output

CSC Sector Processors: 422

- 384 backplane inputs,
- 38 front-panel outputs

Overlap Sector Processors: 524

- 486 backplane inputs,
- 38 front-panel outputs

Barrel Sector Processors: 1670/2474

- (6/9-neighbor versions)

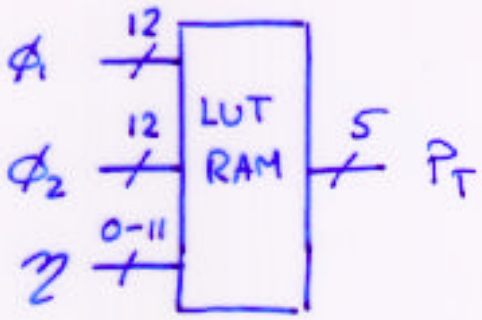
Main savings: ignore ϕ overlaps

Design Considerations

- Tracks crossing sector boundaries are not linked by sector processors
  - reduces data flow on VME backplane
  - P_T>10 $\Rightarrow$ $\Delta\phi_{12} < 2°$
- Magnetic field is non-uniform in endcap
  - Extrapolation in ϕ is more complicated
  - P_T assignment depends on η $\Rightarrow$ LUT complication
- 2D or 3D track finding?
  - Track finding in η-r to reduce combinatorics?
- Ghost suppression
  - Try all η, ϕ possibilities from chamber, or take best matches from MPC?
- Overlap region
  - Problem with ambiguity in η
- What is sector occupancy from background?

Endcap P_T Assignment

Consider single LUT approach using $\Delta\phi_{12}$



Number of η bits required needs to be studied

Size of LUT may be prohibitive:

$$2^{12+12+n} = 17\times10^6 \cdot 2^n \cdot 5 \text{ bits}$$

(P_T resolution dictates 12 bit ϕ precision)

⇒ Arithmetic (ϕ_1-ϕ_2) or cascaded LUT approach

⇒ extra latency

CMS Note 1997/096
G. Wrochna
Warsaw calculations

after calorimeter

Rate

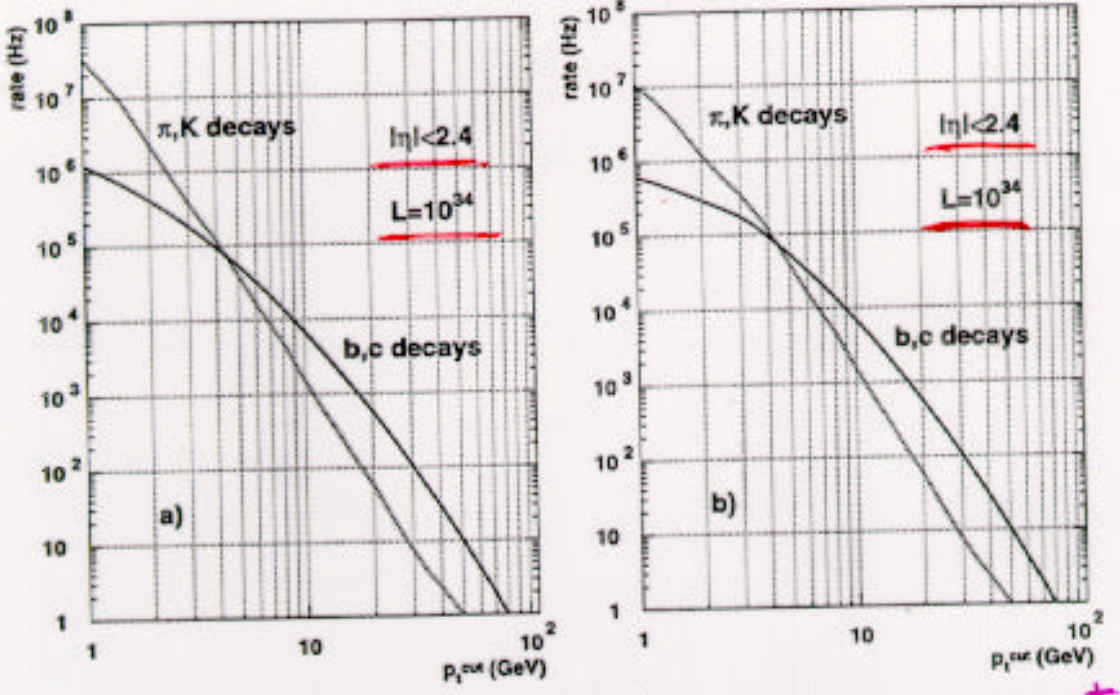


Figure 5.4: Integrated muon rates: a) before and b) after calorimeters.

p_T^{cut}

PROMPT μ's : $\frac{d^3N_\mu}{d\eta\, dP_T\, dt} = a \cdot \exp\left[-\frac{(x-\mu)^2}{2\sigma^2}\right]$

$x = \log_{10} P_T \quad \mu = -0.725 \quad a = 1.308 \cdot 10^6 \quad \sigma = 0.433$

DECAY μ's : $\frac{d^3N_\mu}{d\eta\, dP_T\, dt} = A \cdot P_T^{-b}$

$A = 5.723 \cdot 10^7 \quad b = 5.578$

Real Muon Flux

- Prompt Muons + π/K decay Muons @ $10^{34}cm^{-2}s^{-1}$

P_T Cut	Total Rate	Sector Rate	Sector Occupancy	
1.0 GeV	1.0E7 Hz	170 kHz	0.43%	30° Sector $1.4<\eta<2.4$
2.5 GeV	1.2E6 Hz	56 kHz	0.14%	
5.0 GeV	8.7E4 Hz	4.2 kHz	0.01%	60° Sectors $1.0<\eta<2.4$
10.0 GeV	8.0E3 Hz	0.4 kHz	0.001%	

$|\eta|<2.4$

- Punch-through may approximately double rates
- Occupancy is fairly low
- Is rate of fake stubs from neutrons negligible?
- Assumes 20 min. bias events per xing, no pile up

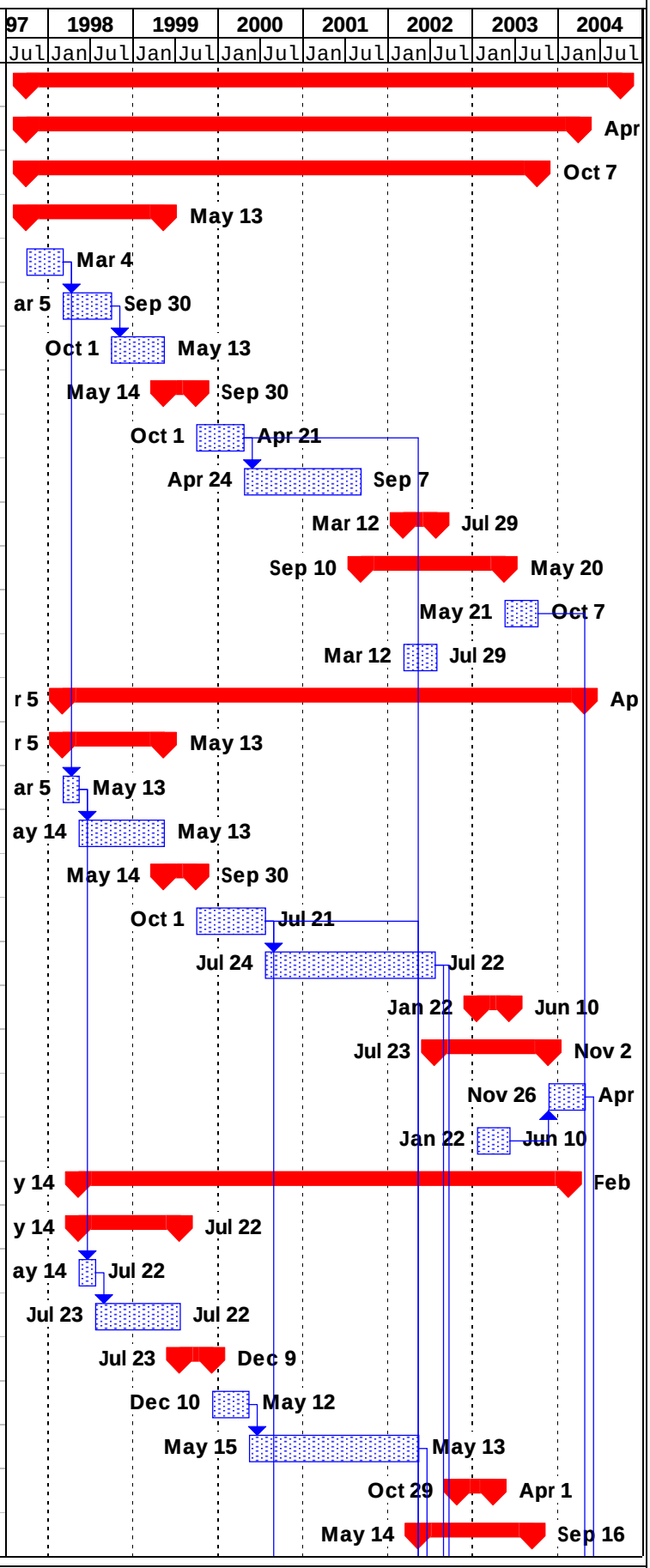
Design Possibilities

- Low occupancy $\Rightarrow$ Track finder is just a coincidence unit between all 3 stations
  - But, still must calculate P_T accurately
    - Total μ rate is of order 100 kHz
    - Single μ trigger rate < 6 kHz

- High occupancy $\Rightarrow$ Track Finder must employ 2D and maybe 3D track finding, resolve ghosts, and prioritize tracks

- Track Finder should be flexible enough to handle everything in between

WBS	Task Name
3.1.1	CSC Muon Trigger
3.1.1.1	Muon Port Cards (MPC)
3.1.1.2	Sector Receivers (SR)
3.1.1.2.1	SR Design
3.1.1.2.1.1	SR Initial System Design
3.1.1.2.1.2	SR Initial Proto. Design
3.1.1.2.1.3	SR Proto. Design
3.1.1.2.2	SR Proto. Construction
3.1.1.2.3	SR Proto. Test
3.1.1.2.4	SR ASIC and Board Design
3.1.1.2.5	SR Active Components
3.1.1.2.6	SR Boards
3.1.1.2.7	SR Installation
3.1.1.2.8	SR Spares
3.1.1.3	CSC Sector Processors (SP-CSC)
3.1.1.3.1	SP-CSC Design
3.1.1.3.1.1	SP-CSC Initial System Des
3.1.1.3.1.2	SP-CSC Proto. Design
3.1.1.3.2	SP-CSC Proto. Construction
3.1.1.3.3	SP-CSC Proto. Test
3.1.1.3.4	SP-CSC ASIC and Board Design
3.1.1.3.5	SP-CSC Active Components
3.1.1.3.6	SP-CSC Boards
3.1.1.3.7	SP-CSC Installation
3.1.1.3.8	SP-CSC Spares
3.1.1.4	Overlap Sector Processors (SP-OVR)
3.1.1.4.1	SP-OVR Design
3.1.1.4.1.1	SP-OVR Initial System Des
3.1.1.4.1.2	SP-OVR Proto. Design
3.1.1.4.2	SP-OVR Proto. Construction
3.1.1.4.3	SP-OVR Proto. Test
3.1.1.4.4	SP-OVR ASIC and Board Design
3.1.1.4.5	SP-OVR Active Components
3.1.1.4.6	SP-OVR Boards



WBS	Item	Unit Cost	Uts	Prj M&S
3.1.1	CSC Muon Trigger	812,038	1	812,038
3.1.1.1	Muon Port Cards (MPC)	5,311	55	292,079
3.1.1.1.1	MPC Design	-	1	-
3.1.1.1.2	MPC Proto. Construction	20,998	2	41,996
3.1.1.1.3	MPC Proto. Test	-	1	-
3.1.1.1.4	MPC ASIC and Board Design	-	1	-
3.1.1.1.5	MPC Active Components	2,975	48	142,800
3.1.1.1.6	MPC Boards	728	48	34,947
3.1.1.1.8	MPC Installation	-	1	-
3.1.1.1.9	MPC Spares	3,703	7	25,921
3.1.1.2	Sector Receivers (SR)	3,714	56	207,994
3.1.1.2.1	SR Design	-	1	-
3.1.1.2.2	SR Proto. Construction	10,000	2	20,000
3.1.1.2.3	SR Proto. Test	-	1	-
3.1.1.2.4	SR ASIC and Board Design	-	1	-
3.1.1.2.5	SR Active Components	2,585	48	124,102
3.1.1.2.6	SR Boards	772	48	37,036
3.1.1.2.7	SR Installation	-	1	-
3.1.1.2.8	SR Spares	3,357	8	26,856
3.1.1.3	CSC Sector Processors (SP-CSC)	5,065	15	75,973
3.1.1.3.1	SP-CSC Design	-	1	-
3.1.1.3.2	SP-CSC Proto. Construction	20,000	1	20,000
3.1.1.3.3	SP-CSC Proto. Test	-	1	-
3.1.1.3.4	SP-CSC ASIC and Board Design	-	1	-
3.1.1.3.5	SP-CSC Active Components	2,815	12	33,778
3.1.1.3.6	SP-CSC Boards	917	12	11,000
3.1.1.3.7	SP-CSC Installation	-	1	-
3.1.1.3.8	SP-CSC Spares	3,732	3	11,195
3.1.1.4	Overlap Processors (SP-OVER)	5,065	15	75,973
3.1.1.4.1	SP-OVER Design	-	1	-
3.1.1.4.2	SP-OVER Proto. Construction	20,000	1	20,000
3.1.1.4.3	SP-OVER Proto. Test	-	1	-
3.1.1.4.4	SP-OVER ASIC and Board Design	-	1	-
3.1.1.4.5	SP-OVER Active Components	2,815	12	33,778
3.1.1.4.6	SP-OVER Boards	917	12	11,000
3.1.1.4.7	SP-OVER Installation	-	1	-
3.1.1.4.8	SP-OVER Spares	3,732	3	11,195
3.1.1.5	Clock&Control Cards (CCC)	3,580	10	35,800
3.1.1.5.1	CCC Board Design	-	1	-
3.1.1.5.2	CCC Active Components	2,600	8	20,800
3.1.1.5.3	CCC Boards	980	8	7,840
3.1.1.5.5	CCC Installation	-	1	-
3.1.1.5.6	CCC Spares	3,580	2	7,160
3.1.1.6	Crate Monitor Cards	1,000	10	10,000
3.1.1.7	Muon Backplanes	2,000	10	20,000
3.1.1.9	Muon Crates	600	10	6,000
3.1.1.10	Muon Power Supplies	2,300	10	23,000
3.1.1.11	Additional Cables	-	1	29,770
3.1.1.12	Trigger System Tests	-	1	-
3.1.1.13	Trigger Project Management	-	1	-

Conclusions

- Major Changes:
  - Arrangement of data into 60° sectors with boundaries at 15°, 75°, 135°, …
  - Ignore ϕ boundaries
    - Negligible P_T - dependent loss
    - Potential 10°/60° = 17% loss in overlap region
- Cost savings (~20%) from reduced number of crates and boards
- Initial system design phase
- Details can be found here:

  http://www-collider.physics.ucla.edu/cms/trigger/

  http://bonner-ntserver.rice.edu/motherboard/Archive/src.htm