
# *Towards A Unified Track-Finder Processor*

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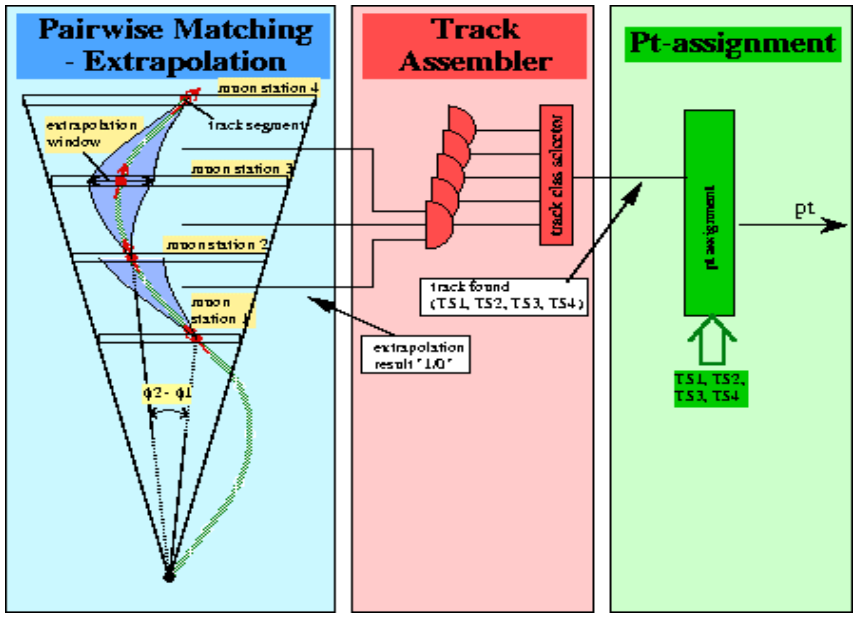
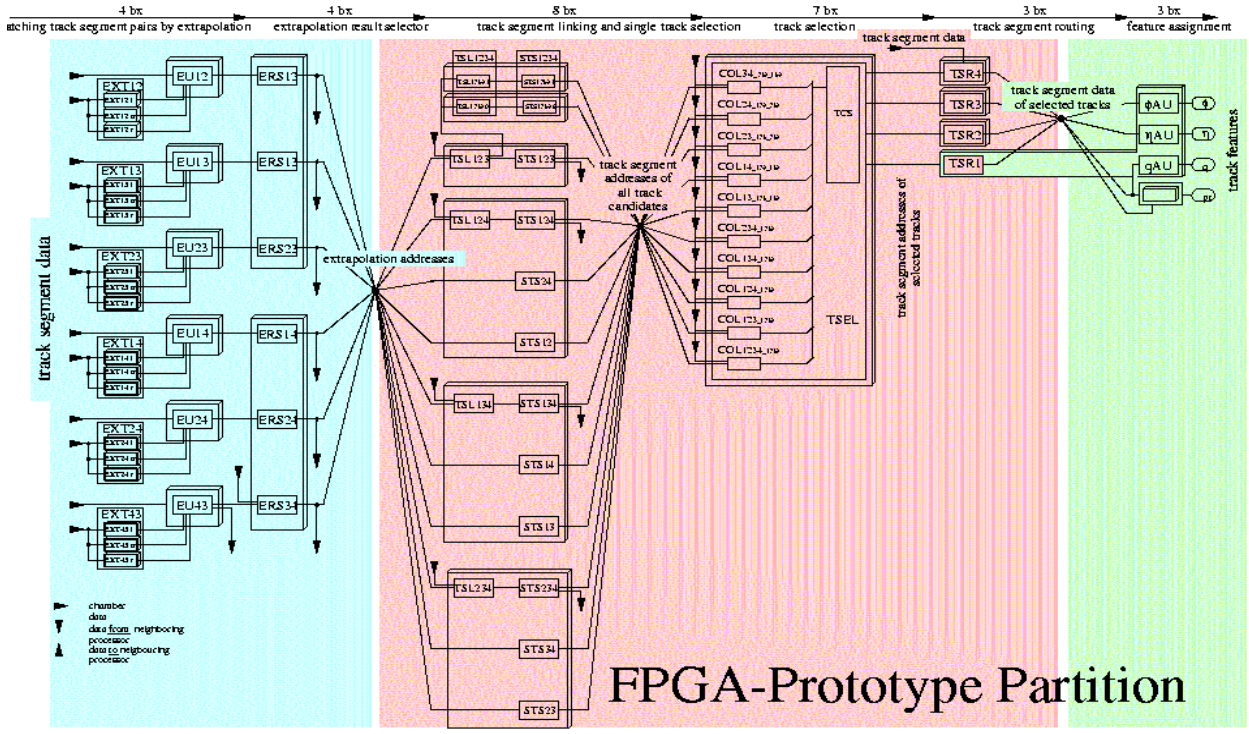
# Vienna Approach to Track Finding




Generalize scheme to include η dependence in endcap and overlap regions for matching and Pt-assignment

# *Number of Extrapolation Units Per Sector Processor*

| | DT | CSC | Overlap |
|---|---|---|---|
| **Sector size** | **30°** | **60°** | **60°(30°)** |
| **Number of stations** | **4** | **3 (4)** | **3 / 4** |
| **Number of extrapolation pairs (1↔2, 1↔3, 2↔3, …)** | **6** | **3 (6)** | **3 / 6** |
| **Source track segments / station** | **2** | **3** | **2 / 3** |
| **Target track segments / station** | **12 (18)** | **3** | **3 ?** |

**Number of extrapolation units:**

**DT: 6 (or 9) neighbors in φ and η** — **144 (216)**

**No φ sharing** — **48 (72)**

**CSC: 3 (4) stations, no φ sharing** — **27(54)**

**Overlap: no φ sharing** — **18-54+**

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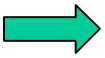
# *Inputs to a Single Pairwise Extrapolation Unit*

| | DT | CSC |
|---|---|---|
| **φ :** | **11 bits / 30°** | **12 bits / 60°** |
| **dφ :** | **8 bits** | **6 bits** |
| **η :** | **2 bits** | **11 bits** |
| **Quality :** | **2 bits** | **3 bits** |



*n.b.* No η information from DT in overlap region

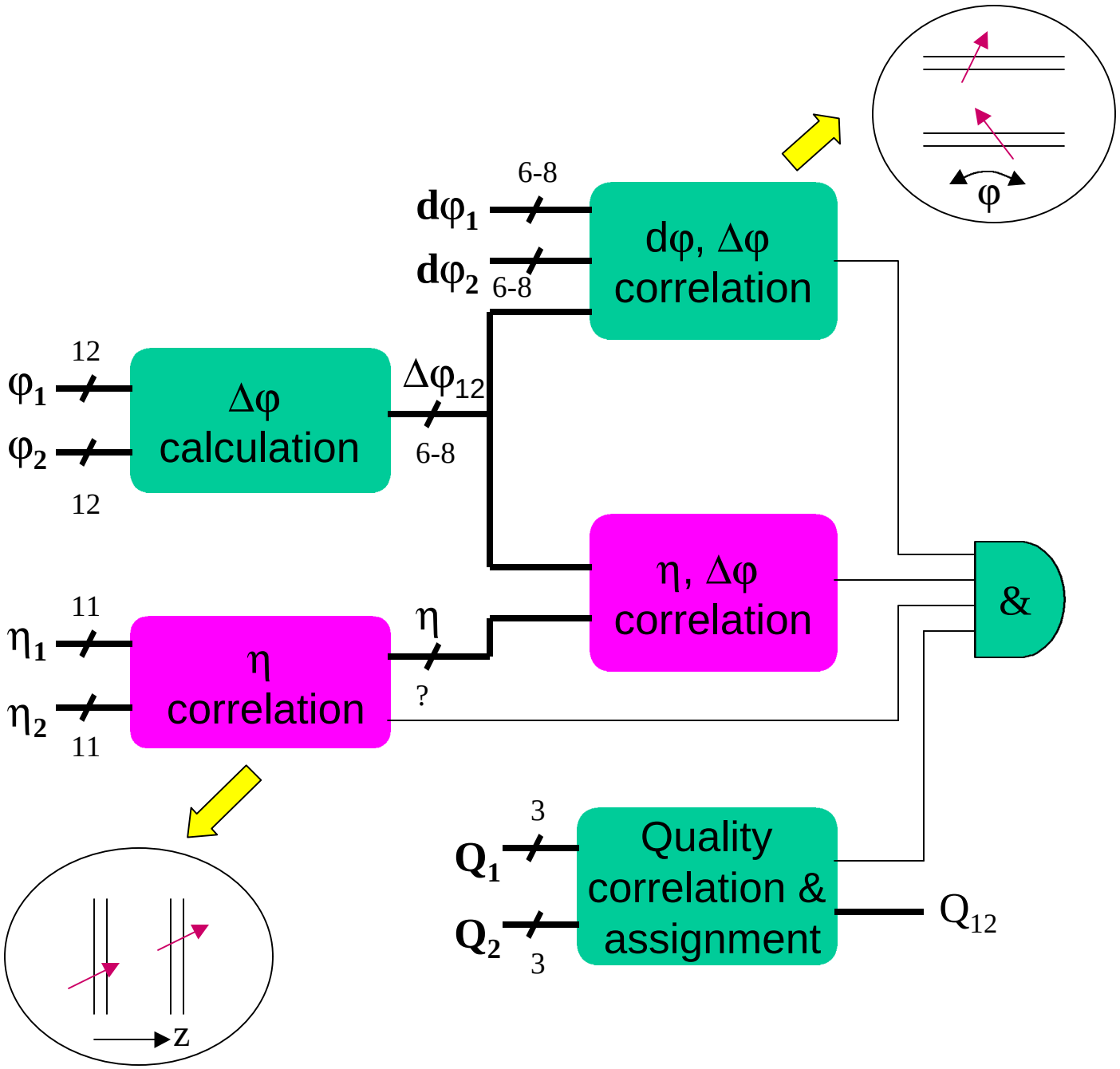

# *Effect of 12-bit φ Resolution in Endcap*

| | ME 1 / 1 | ME 2,3,4 / 2 | ME 2,3,4 / 1 |
|---|---|---|---|
| Strip Count | 59 / 10° | 75 / 10° | 75 / 20° |
| 12-bits / 60° segmentation | 0.09 strip | 0.11 strip | 0.06 strip |
| Resolution Contribution | 0.03 strip | 0.03 strip | 0.02 strip |

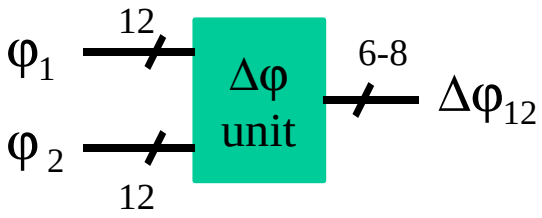
⇒ LCT φ resolution expected to be ~0.1 strip

⇒ 12-bit precision contributes < 5% to overall resolution

# Block Diagram of Extrapolation Unit



# $\Delta\varphi$ *Calculation Unit*



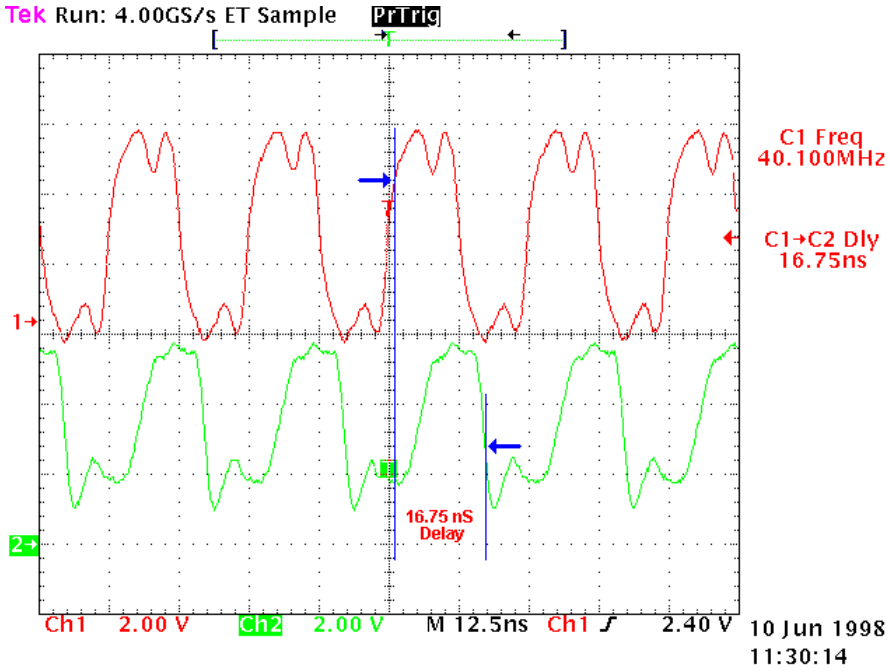

$\Rightarrow \Delta\varphi$ result used in further correlations

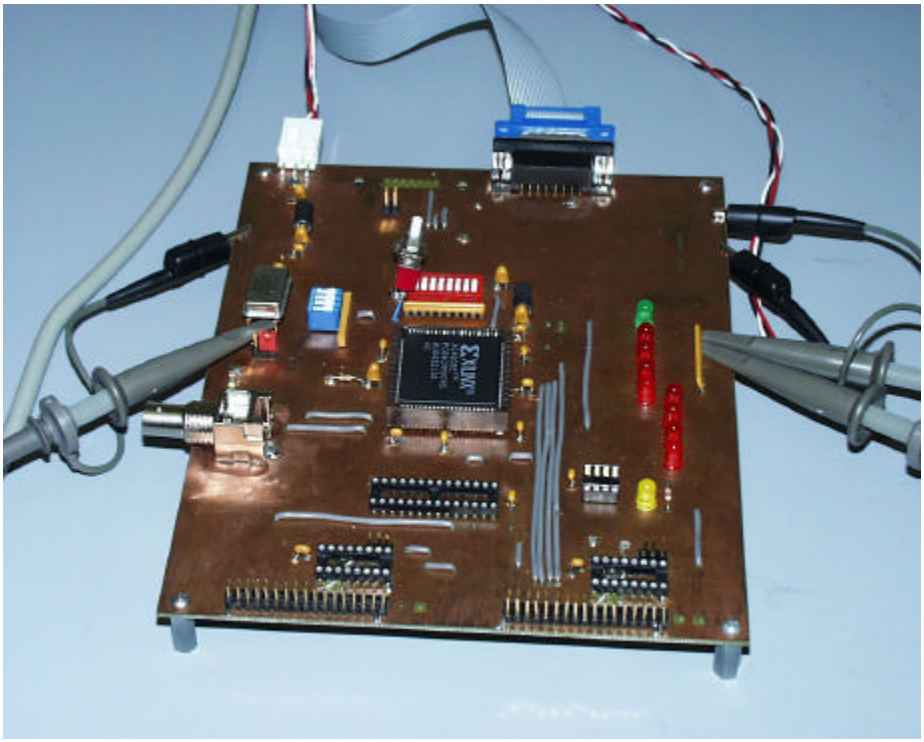
$\Rightarrow$ Compresses $\varphi_1$ and $\varphi_2$ information into physically meaningful quantity

$\Rightarrow$ Only need 6 - 8 bits for $\varphi$ extrapolation

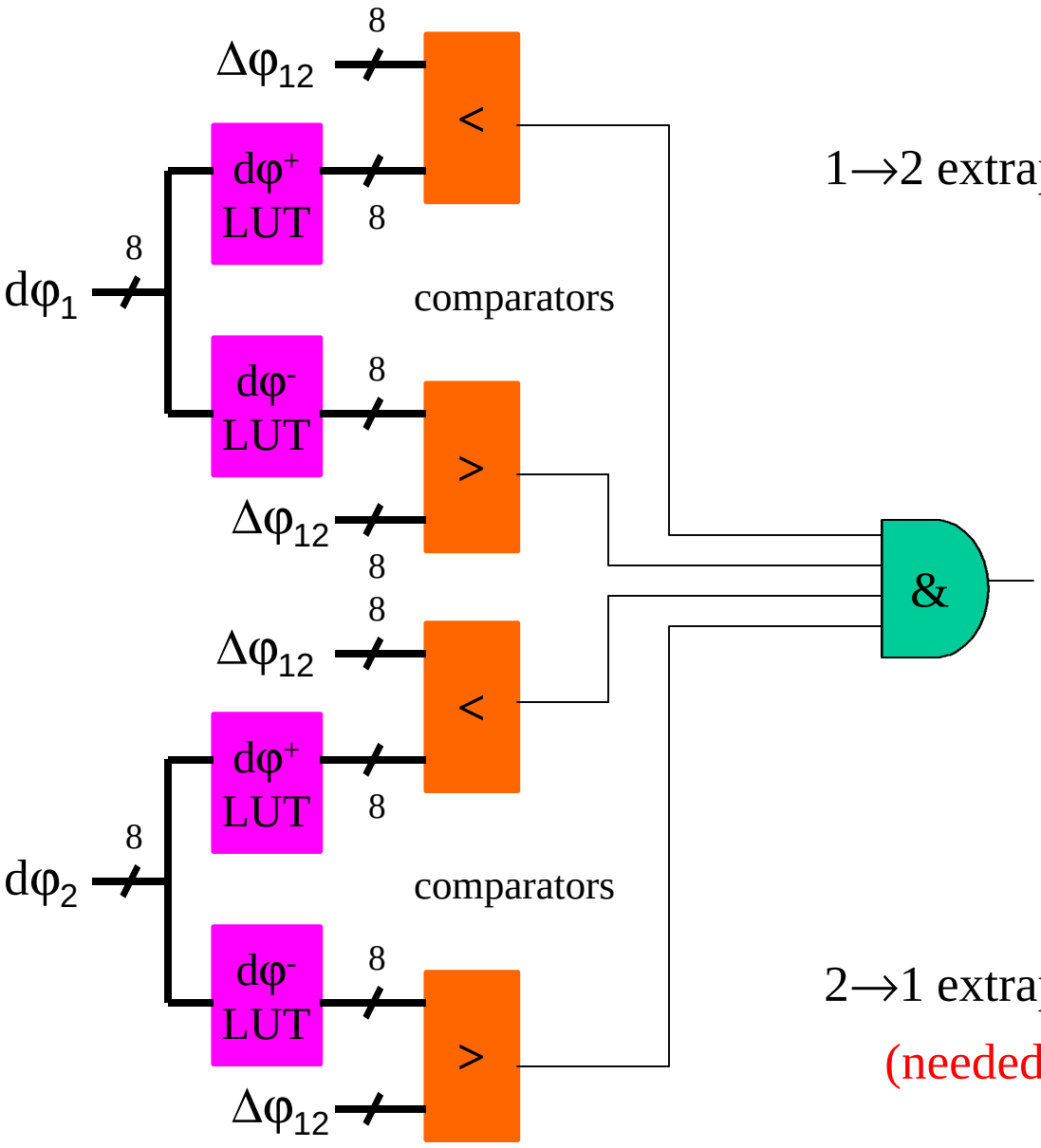
$\Rightarrow$ Subtraction can be implemented in FPGA in 1 b.x.

# *12-bit Adder Ripple Delay* (FFF+1) *in Xilinx XC4000 testboard*



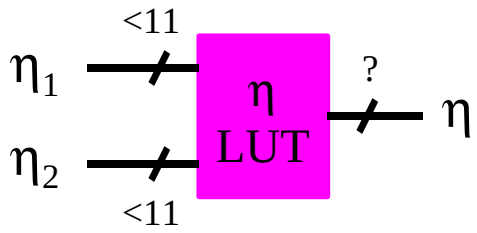



# Φ Extrapolation (dφ, Δφ Correlation)




⇒ Checks consistency between Δφ and dφ


# η *Extrapolation*



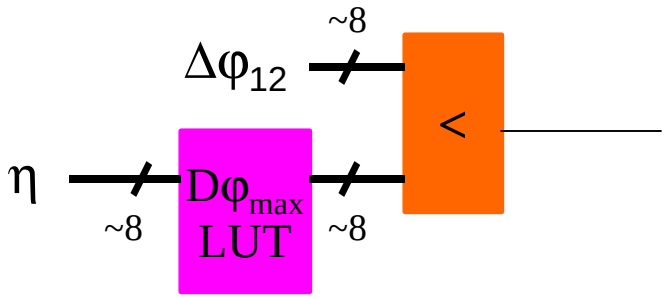

⇒ η correlation unit sends $\eta_1$ for further correlations if $\eta_1$ and $\eta_2$ are in agreement

⇒ Necessary precision still to be determined

⇒ LUT implementation in FPGA if the bit count is low

⇒ $\Delta\eta$ calculation followed by LUT if bit count is larger, or external LUTs

# η, Δφ *Correlation Unit*

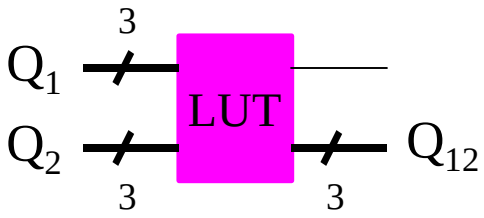



⇒ Limits Δφ as function of η

⇒ Not needed for barrel region, where B is independent of η

⇒ Need to determine necessary η precision

# Quality Assignment and Correlation




$\Rightarrow$ Need to define criterion

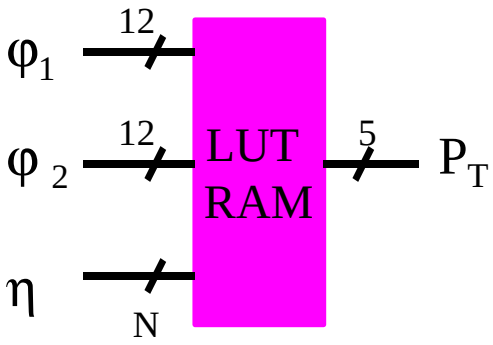

# *Track Assembly*

- The Vienna approach in assembling tracks from station pairs is independent of extrapolation details, so the logic would be applicable for all regions

- Further complications (and latency) arise if we try to account for track segments out of time or in neighboring φ sectors at this point

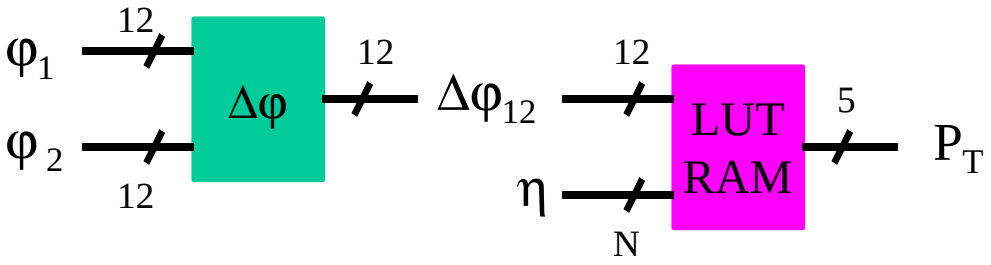
# $P_T$ Assignment

⇒ Size of single LUT may be prohibitive




⇒ $2^{12+12+N} = 17\times10^6 \times 2^N$ ($\times$ 5 bits)

⇒ Cascade logic:




⇒ Arithmetic unit adds 1 b.x. latency, but could use fast cascaded SDRAM instead


# *Features*

- Trigger logic is tunable
  - Content of memory LUT is programmable
  - Any correlation unit can be set to accept all inputs
  - For example, turn off η correlation for barrel region
- FPGA technology allows flexibility in logic design
- No extra latency in the extrapolation units to include η dependencies (just additional correlations in parallel)
- Design hopefully evolves into the same hardware for barrel, overlap, and endcap regions


# *Limitations*

- Neighboring φ sectors are not explicitly handled unless one copes with the *large* number of additional extrapolation units and signal inputs
- Track segments assigned to the wrong bunch crossing are also ignored
- Increasing the number of extrapolation units is probably the wrong approach (too many signals)
- Try to account for these minor effects in the track assembly stage to promote tracks to higher quality
  - Require at least 2 in-time stations in one sector, then consider a limited number of late or neighboring segments
- Multiple hits in a single CSC chamber are not tested for ghosts (2 track segments $\rightarrow$ 4). Requires more extrapolation units. Try to keep solution at motherboard level.


# *Further Study*

- Minimize $\eta$ precision for $\Delta\varphi$, $\eta$ correlation
  - Reduces LUT sizes
  - Simplifies $\eta$ determination for ME1/1 (tilted wires)
- Study extrapolation from CSC to DT in overlap region where DT has no $\eta$ information
- Useful to have backward $\varphi$ extrapolation ($2 \rightarrow 1$) ?
- What is criterion for track quality assignment ?
- Improve track assembly to account for neighboring $\varphi$ sectors and bunch crossings
- Any problem from ghost hits in single chamber ?
- Simulate efficiency and $P_T$ resolution (trigger rate) of track-finding algorithms