Track-Finding Processor for the Endcap Muon System

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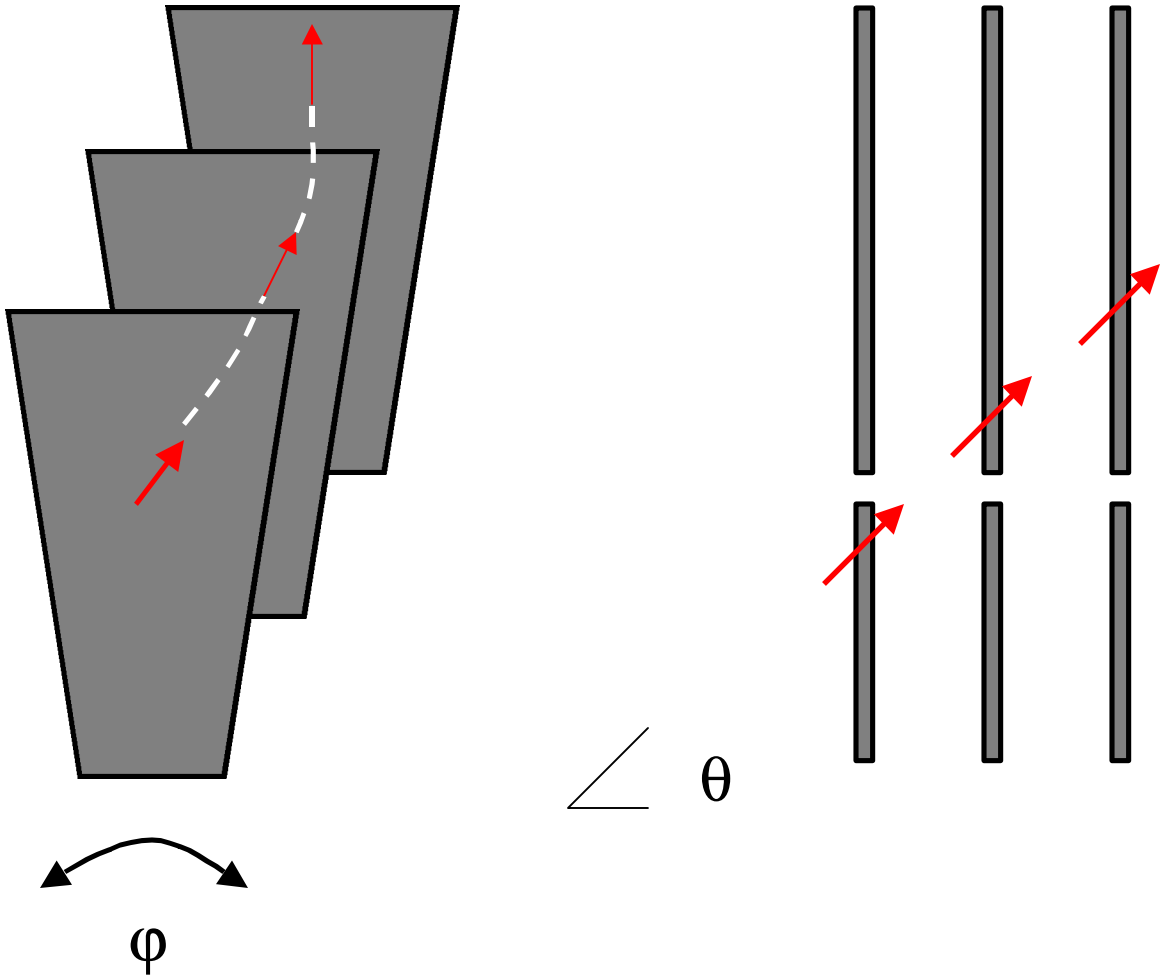
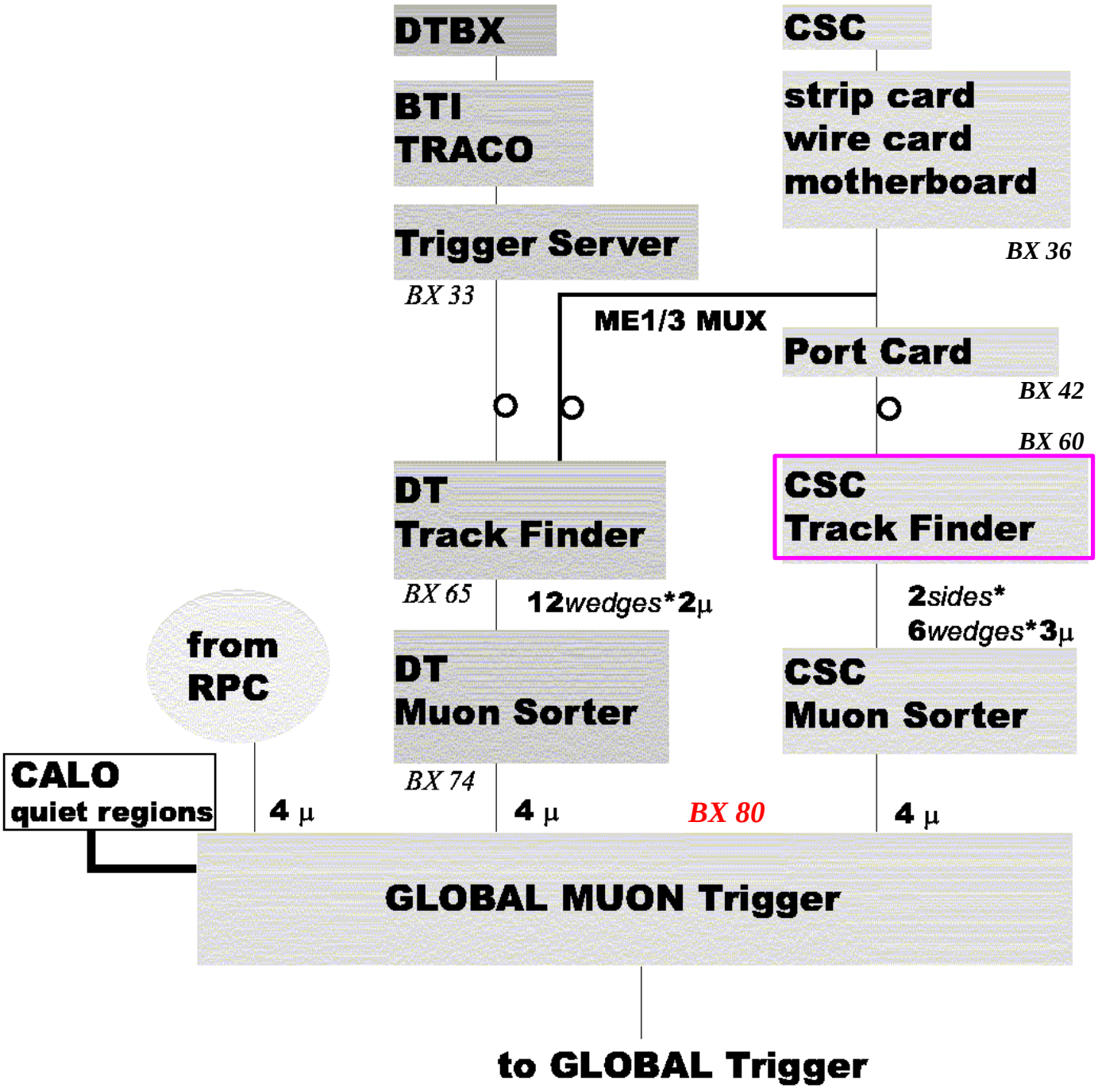
Muon Track-Finding

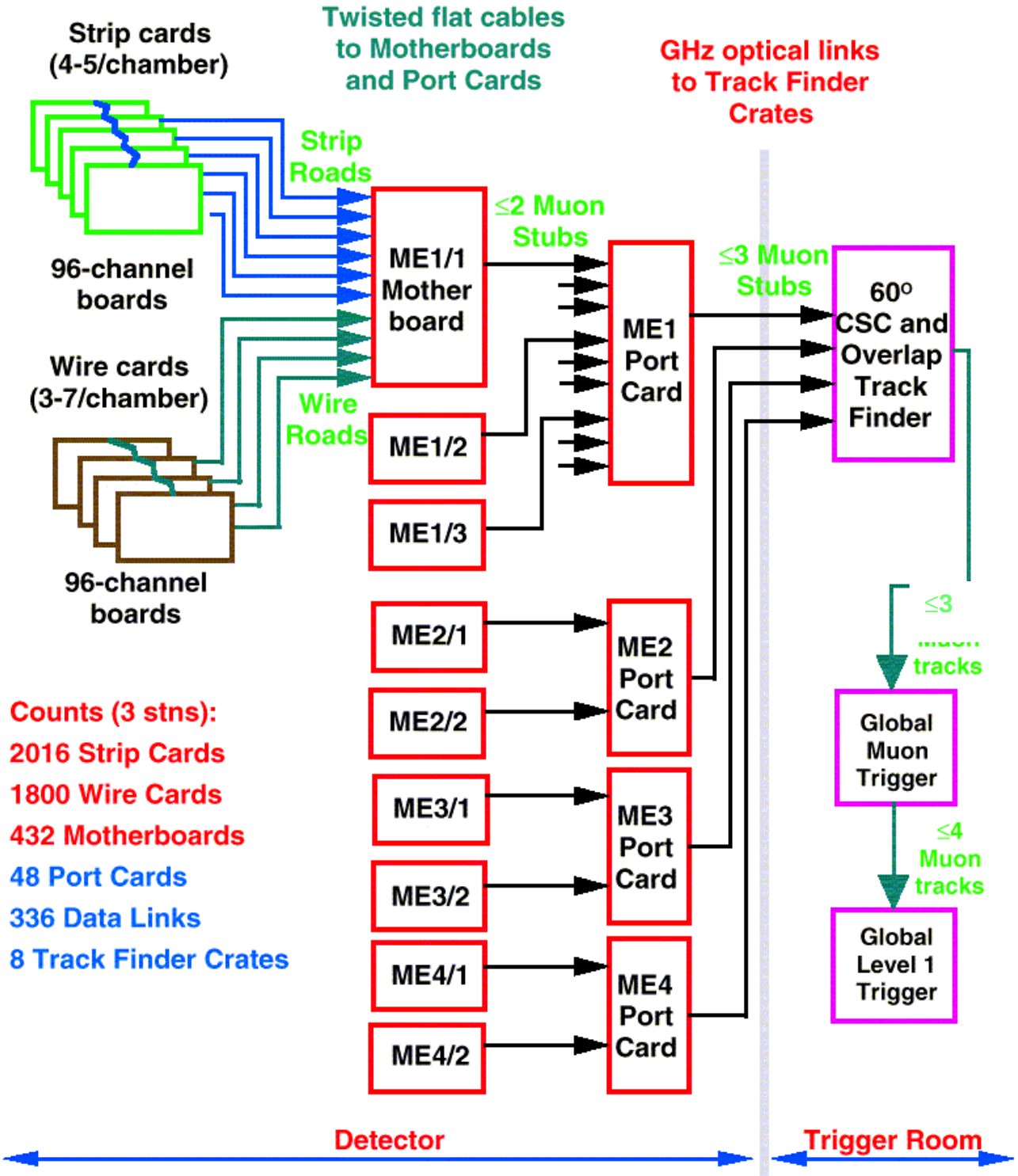
- **Link trigger primitives (stubs) into tracks**
- **Assign P_T, φ, and η**
- **Send highest P_T candidates to Global L1 trigger**



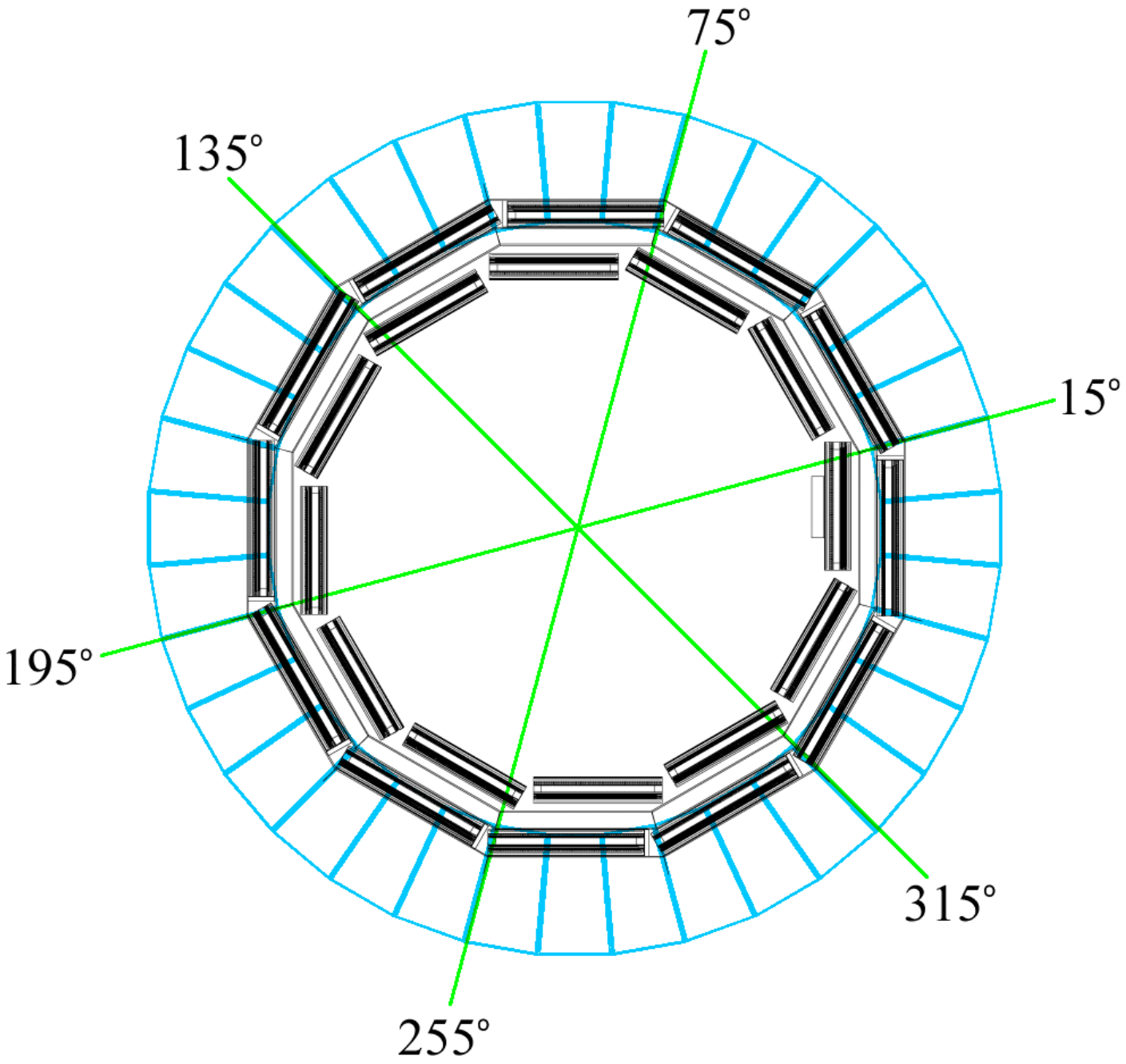
Muon Trigger Scheme



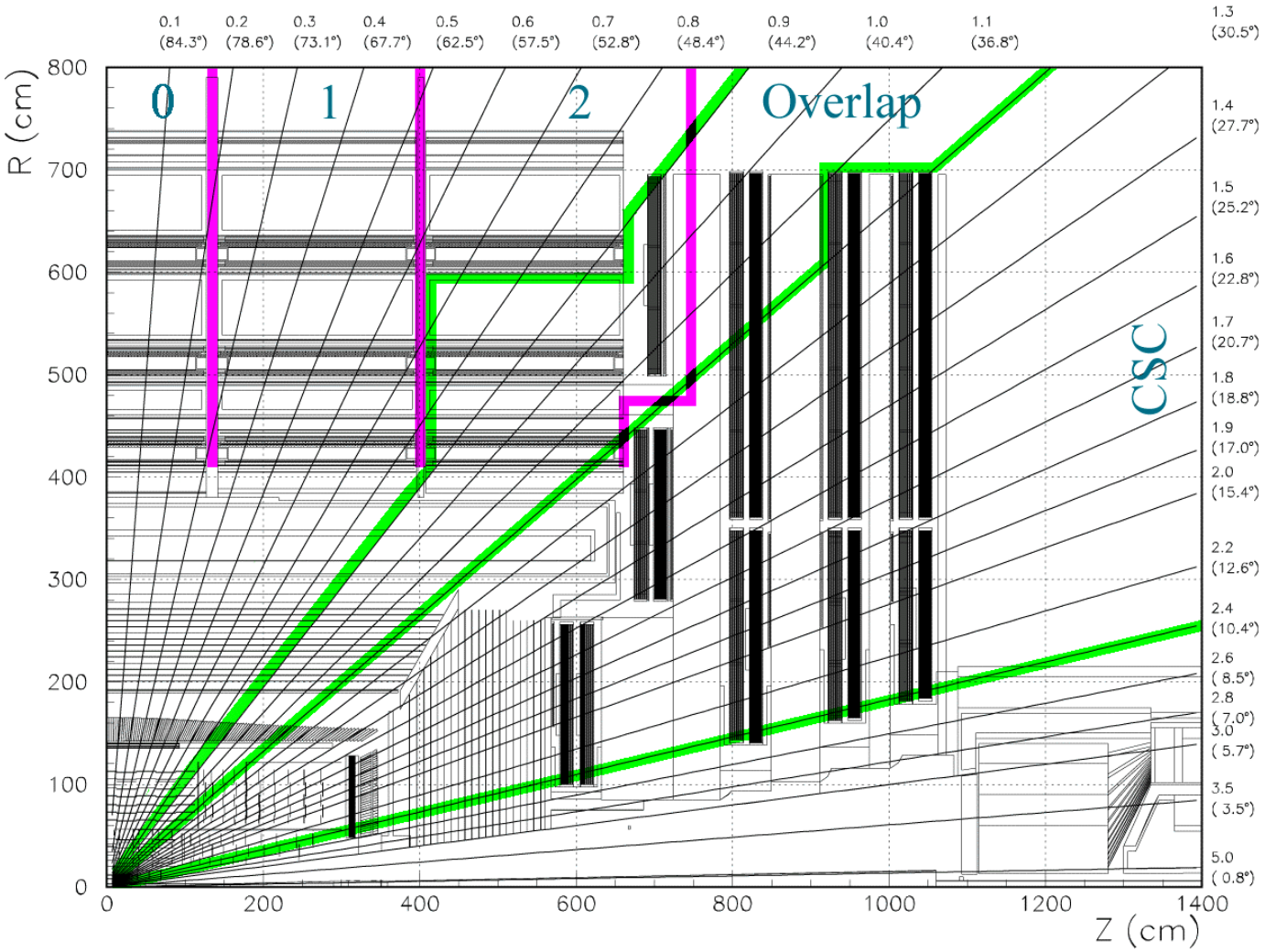
CSC Muon Trigger



CSC Sector Layout



Trigger Regions in η



Track-Finding in Overlap Region Vienna/Bologna Proposal

- Data path: ME1/3 $\rightarrow$ DT T-F
  - special link from ME1/3 motherboard, or from Sector Receiver card.
- No modification to DT T-F hardware
  - ME1/3 becomes MB4 neighbor in η
  - inputs already there
- P_T measurement determined mostly from MB1/MB2 which are barrel chambers
- Simplifies CSC T-F:
  - Reduced Sector Processor logic and I/O,
  - Less processor units required
  - Reduced I/O for Sector Receiver cards (no fan-out)
  - Fewer CSC muons to sort
  - No CSC crate interconnections
- Saves some CSC latency

Track-Finding in Overlap Region U.S. Proposal

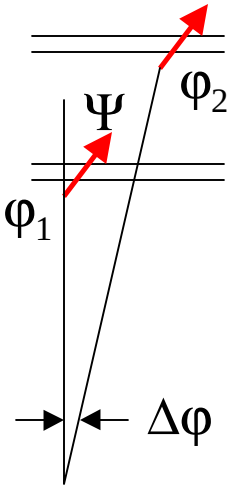
- Data path: MB1 + MB2 $\rightarrow$ CSC T-F
  - special DT Sector Receiver card or direct connection to processor
- CSC Trigger Motherboard design unchanged
- Uses η information for P_T determination
  - B-field changes by only ±5% though
- Full 3D Track-Finding in η and φ
  - reduces fakes
- Greater redundancy with ME2 in case ME1/3 misses hit
  - Large (~25%) acceptance loss from cracks between ME1/3 chambers

Keep option to cover overlap region with CSC T-F open. Design Sector Processor which can operate in either CSC or overlap crate. Offers complementary approach to difficult region.

Sector Receiver Functionality

- Receives 6 stubs via optical links from 2 Port Cards
- Synchronizes the data
  - No additional synchronization performed by the Sector Processor
- Reformats the data
  - LCT bit pattern $\rightarrow \eta, \varphi, \Psi$
- Applies alignment corrections to φ coordinate
  - Depends on φ and η
- Communicates to Sector Processor via point-to-point backplane or connector
- Fan out signals to neighboring processors if U.S. handles overlap region or ME1/3 data is sent to DT Sector Processor

Required Precision of Data



- Azimuthal angle φ:
  - LCT resolution is 0.1 strip
  - 12 bits / 60° ⇒ 1 bit / 0.26 mrad (0.1 strip)
- Bend angle Ψ:
  - Range is ±45° with 0.5 strip minimum bend
  - 6 bits / ±45° ⇒ 1 bit / 60 mrad
  - Projection of Ψ_{min} ⇒ Δφ ~ 10 mrad
- $\Delta\varphi = \varphi_2 - \varphi_1$:
  - Maximum deflection is <15°
  - 11 bits full precision (12 bits - 2 bits + sign)
  - **6 bits / 15° ⇒ 1 bit / 8 mrad**
- Polar angle η:
  - Range is 2.4 - 0.9 = 1.5 units
  - B-field variation < ±4% for 0.05 unit bins
  - 5 bits / 1.5 units ⇒ 1 bit / 0.05

Quantity	DT	CSC	T-F	P_T
φ	12 bits	12 bits	7 bits	12 bits
Δφ	13 bits	13 bits	6 bits	11 bits
ψ	8 bits	6 bits	6 bits	6 bits
η	8 bits*	11 bits	5 bits	5 bits
Quality	3 bits	3 bits	3 bits	—

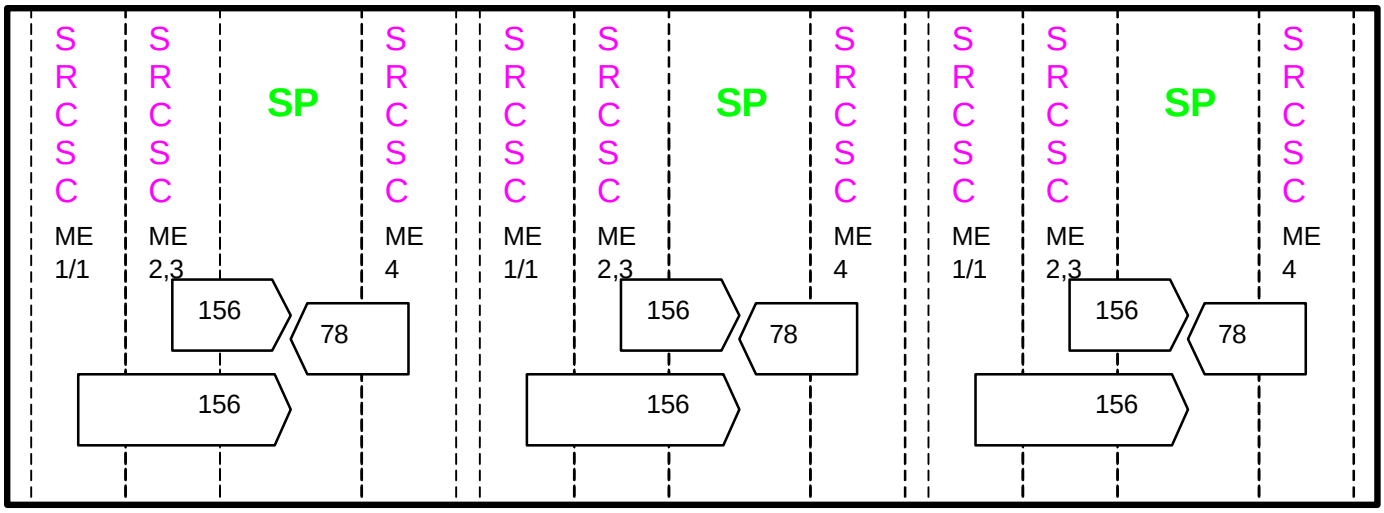
Track Segments per Sector

Region	Station	Chamber	Segments per sector	No. of φ sectors	No. of segments	Extrap-olations
CSC	1	ME1	3	2	6	81
	2	ME2	3	1	3	
	3	ME3	3	1	3	
	4	ME4	3	1	3	
OVL	1	MB1	2	2	4	106
	2	MB2	2	2	4	
	3	ME1	3	2	6	
	4	ME2	3	1	3	

Inputs to CSC Sector Processor

- 1 CSC stub = 12 φ bits + 6 Ψ bits + 5 η bits + 3 Q bits = 26 bits
- 1 Port Card sends 3 stubs
- 1 Sector Receiver accepts 2 Port Cards = 6 stubs
- 1 Sector Processor accepts 6 + 3 + 3 + 3 = 15 stubs (divided between 2.5 Sector Receivers)
- 15 stubs × 26 bits = 390 bits

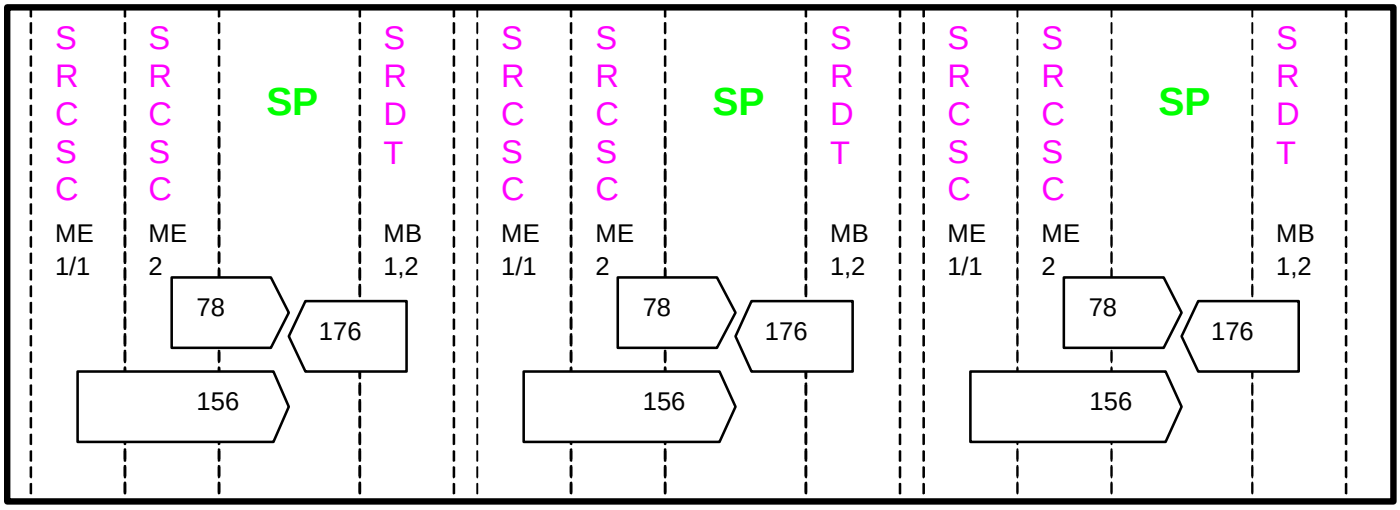
CSC crate:



Inputs to OVL Sector Processor

- 1 CSC stub = 26 bits
- 1 DT stub = 11 φ bits + 8 Ψ bits + 3 Q bits = 22 bits
- 1 Sector Processor accepts 4+4 DT stubs and 6+3 CSC stubs
- (8 DT stubs × 22 bits) + (9 CSC stubs × 26 bits) = 410 bits

OVL crate:



Track-Finding Algorithm

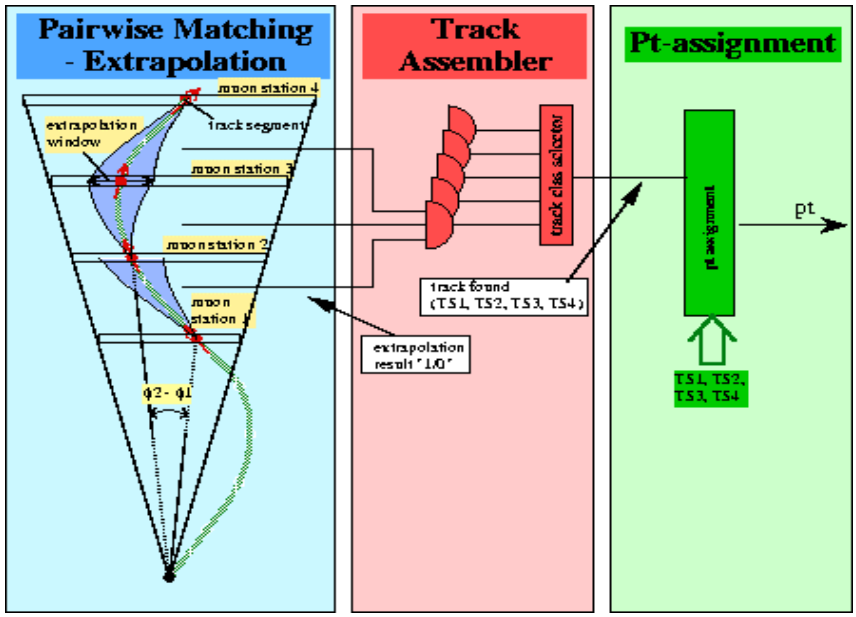
- Sector Processor must identify muons from ~400 input bits

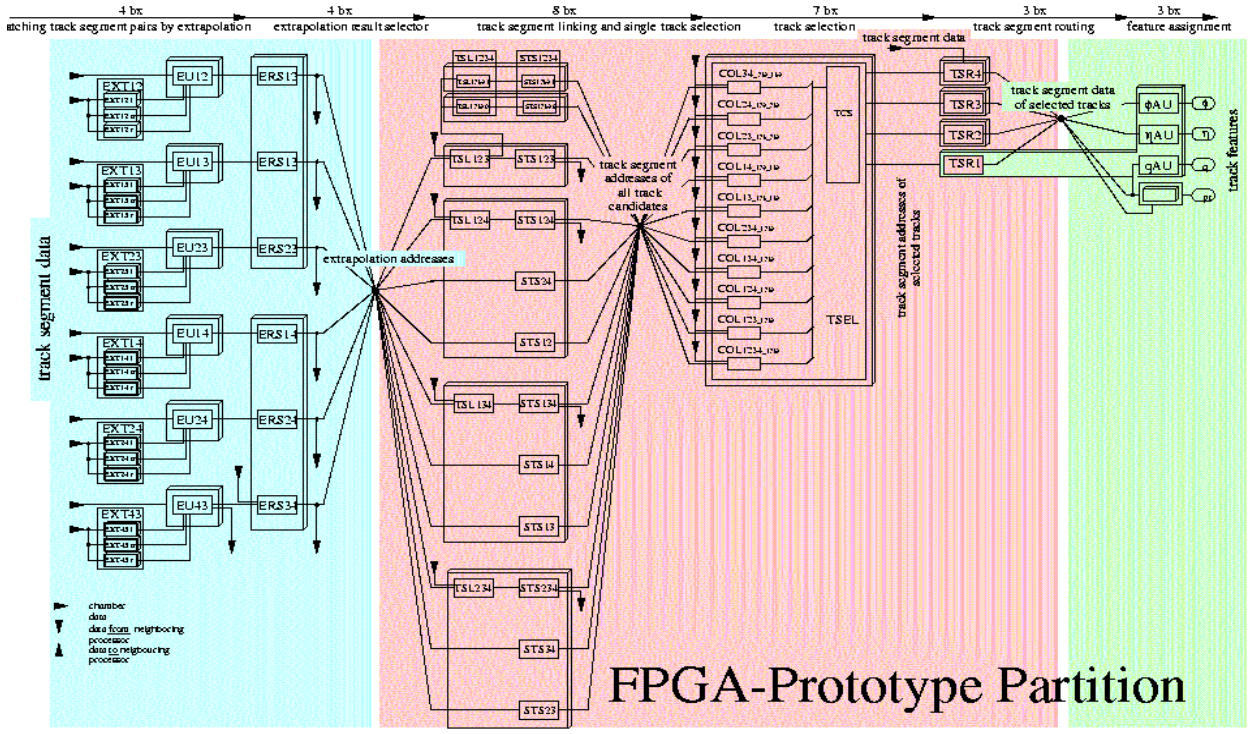
- Follow approach of Vienna design:

1. Perform all possible station-to-station extrapolations in parallel
2. Assemble 3- and 4-station tracks from 2-station extrapolations
3. Cancel redundant tracks if 3 or 4 stations in length
4. Select the three best candidates
5. Calculate P_T, φ, η and send to CSC muon sorter:

Quantity	Precision
η	6 bits
φ	8 bits
Muon sign	1 bit
P_T	5 bits (nonlinear)
Quality	2 bits

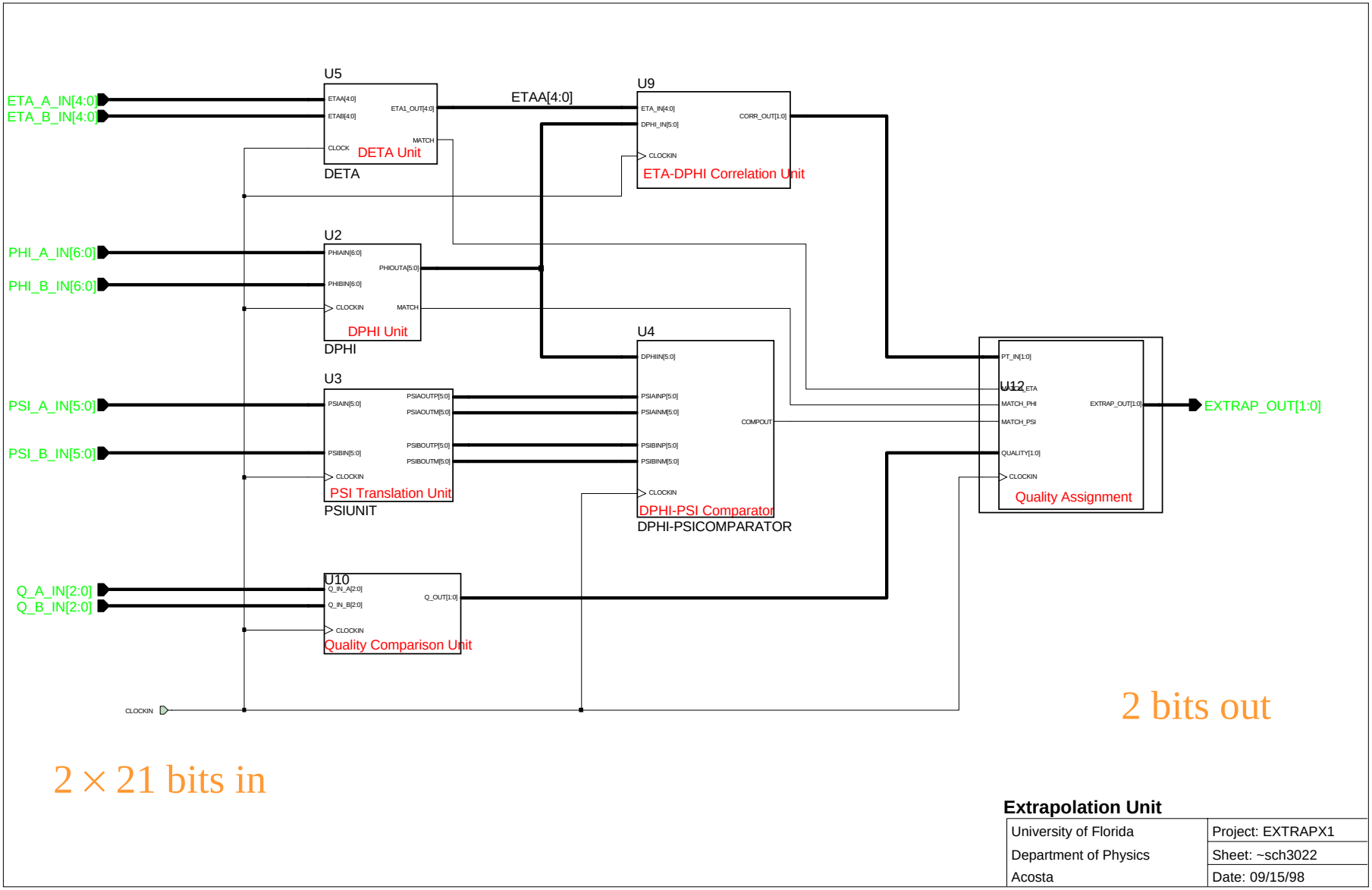
Vienna Approach to Track Finding



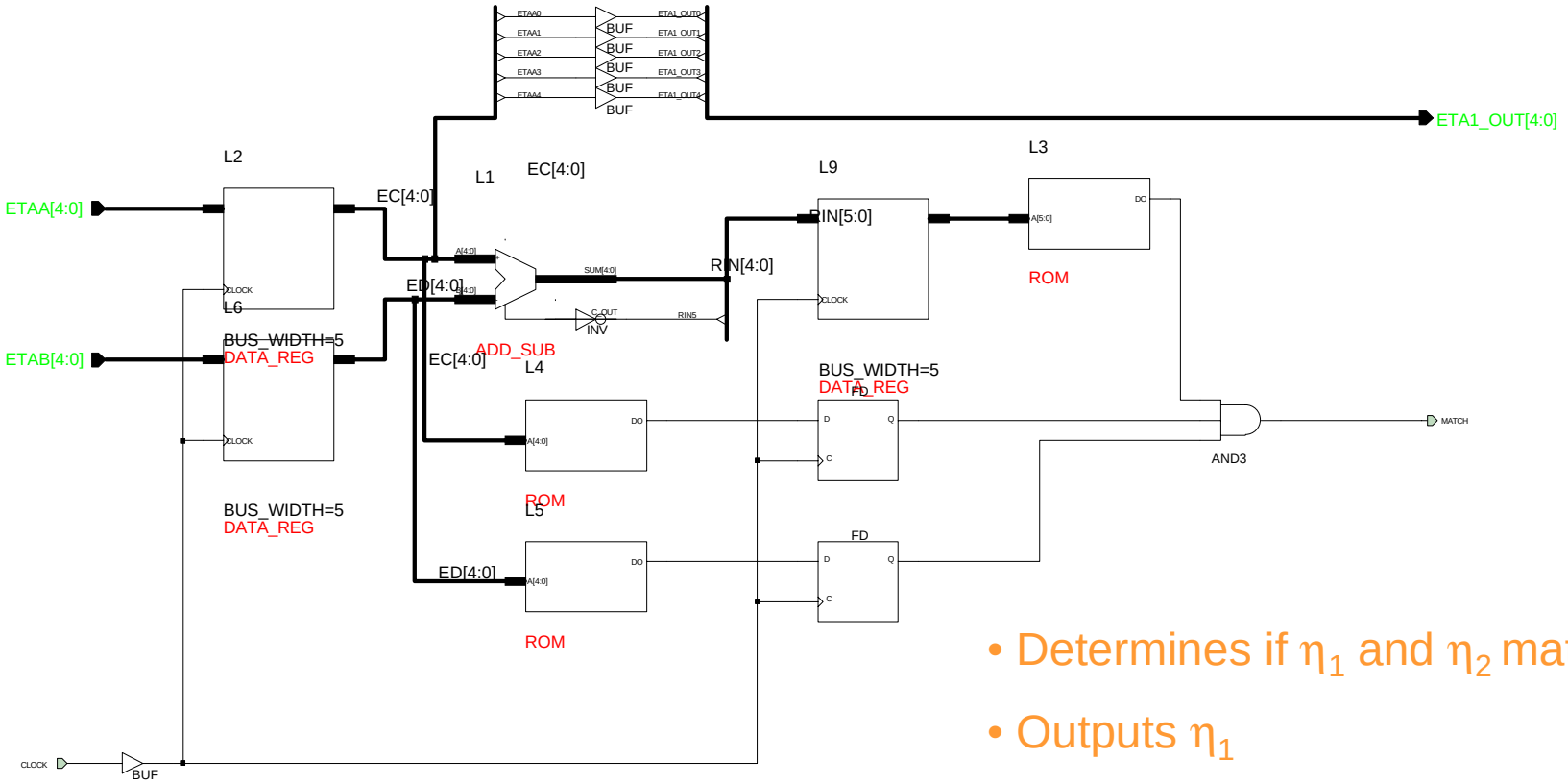


Generalize scheme to include η dependence in endcap and overlap regions for matching and Pt-assignment

Extrapolation Logic



Δη Calculation Unit



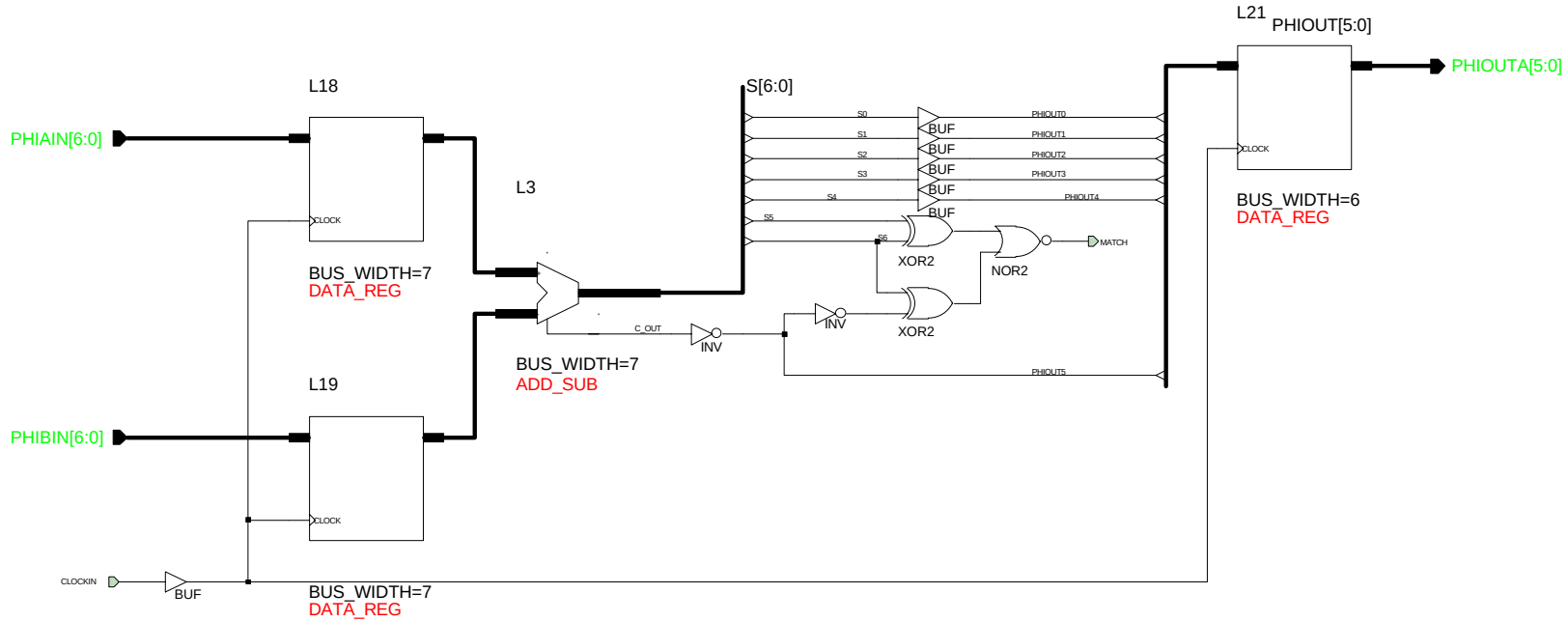
- Determines if η_1 and η_2 match
- Outputs η_1

DETA Unit

University of Florida	Project: EXTRAPX1
Department of Physics	Macro: DETA
Acosta	Date: 09/15/98

Δφ Calculation Unit

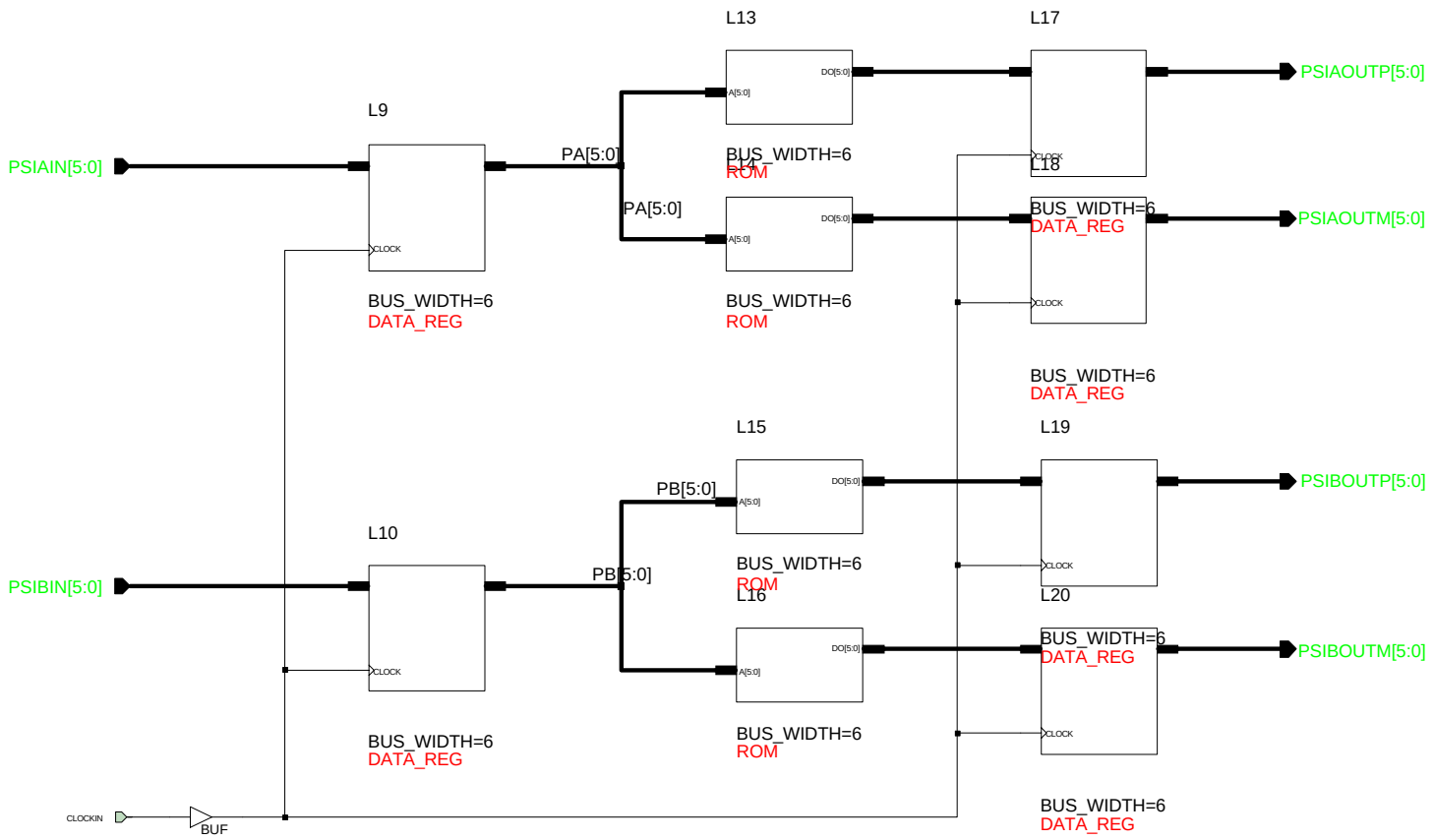
- Calculates φ difference
- Limits difference to <15°



DPHI Unit

University of Florida	Project: EXTRAPX1
Department of Physics	Macro: DPHI
Acosta	Date: 09/15/98

Ψ Translation Unit

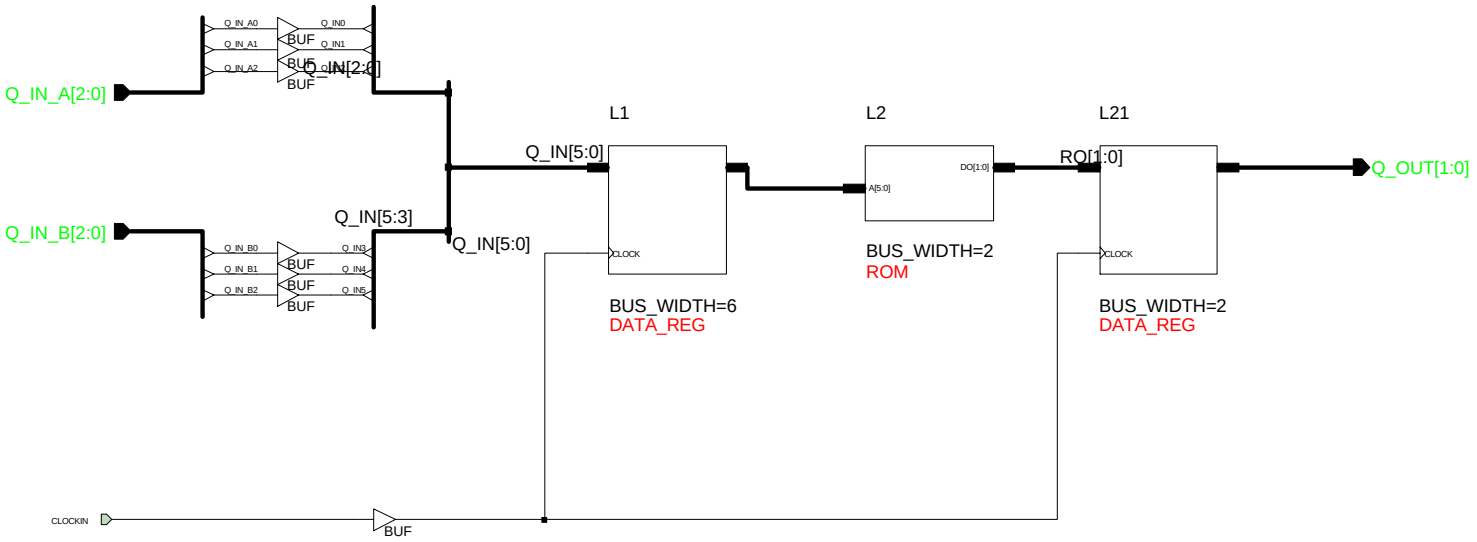


Translates bend angles Ψ_1 and Ψ_2 into ranges in $\Delta\varphi$

PSI Translation Unit

University of Florida	Project: EXTRAPX1
Department of Physics	Macro: PSIUNIT
Acosta	Date: 09/15/98

Quality Comparison Unit

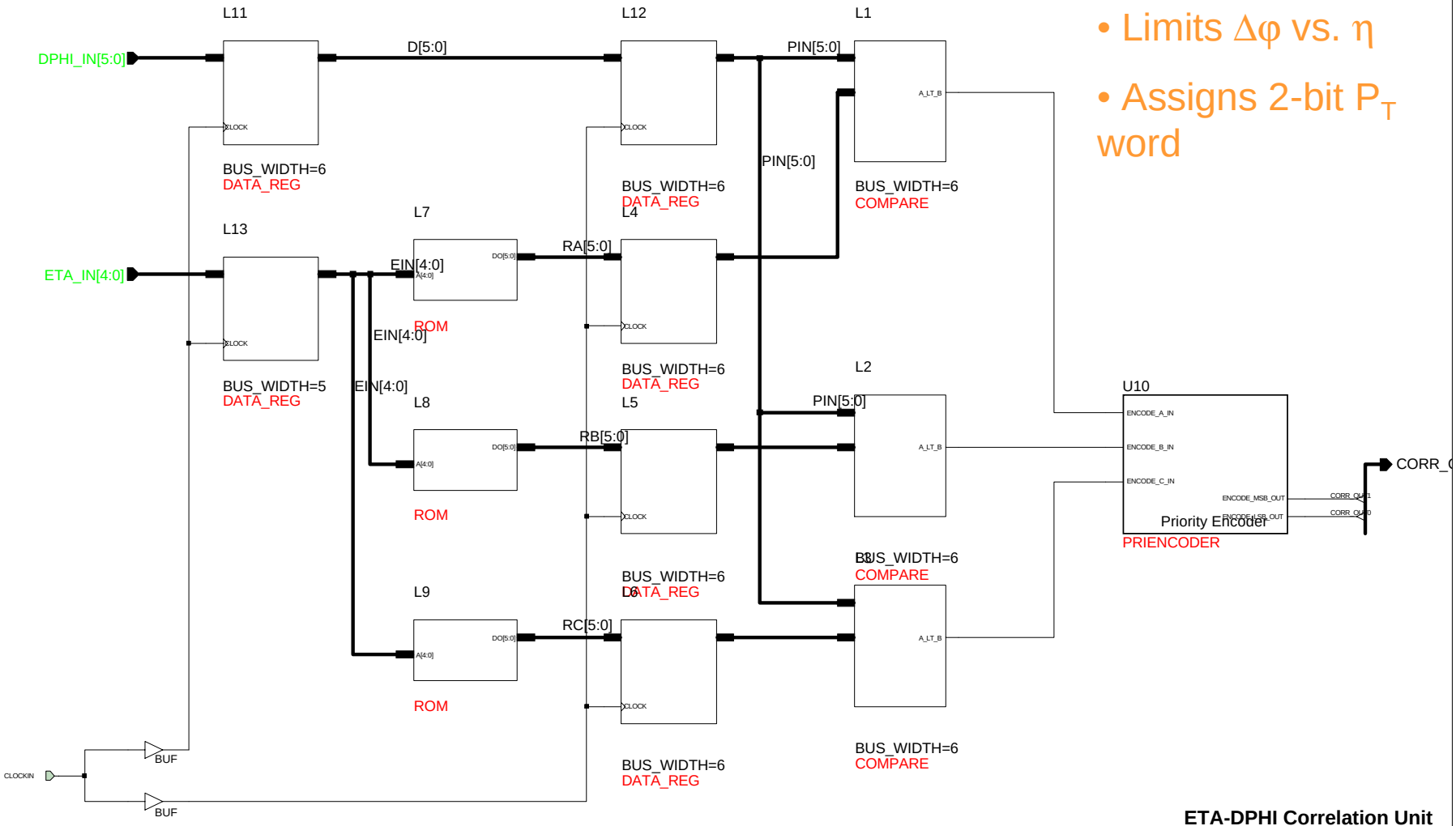


Applies any quality cuts and assigns combined quality

Quality Comparison Unit

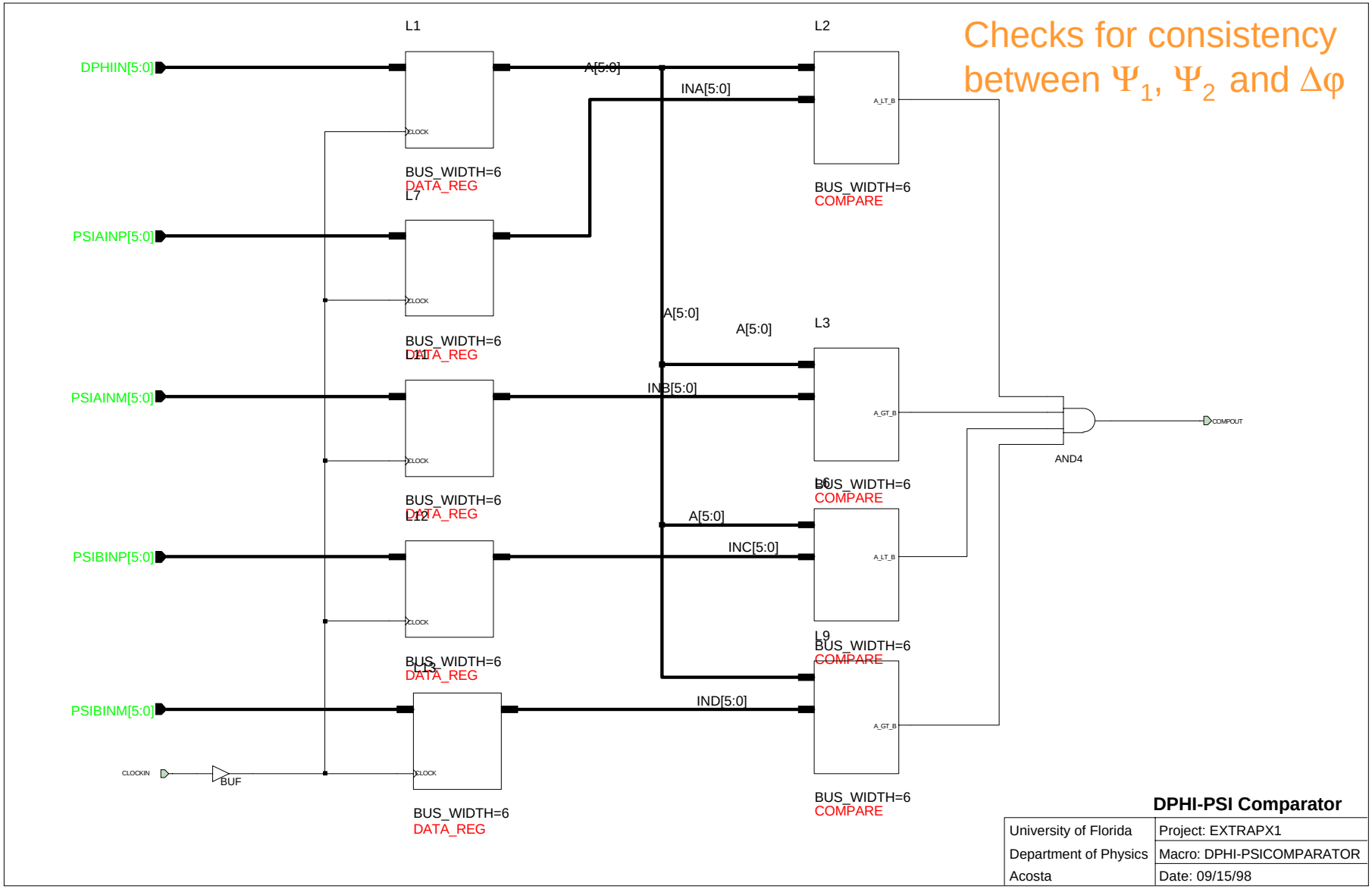
University of Florida	Project: EXTRAPX1
Department of Physics	Macro: QUALCOMPAR
Acosta	Date: 09/15/98

η , Δφ Correlation Unit

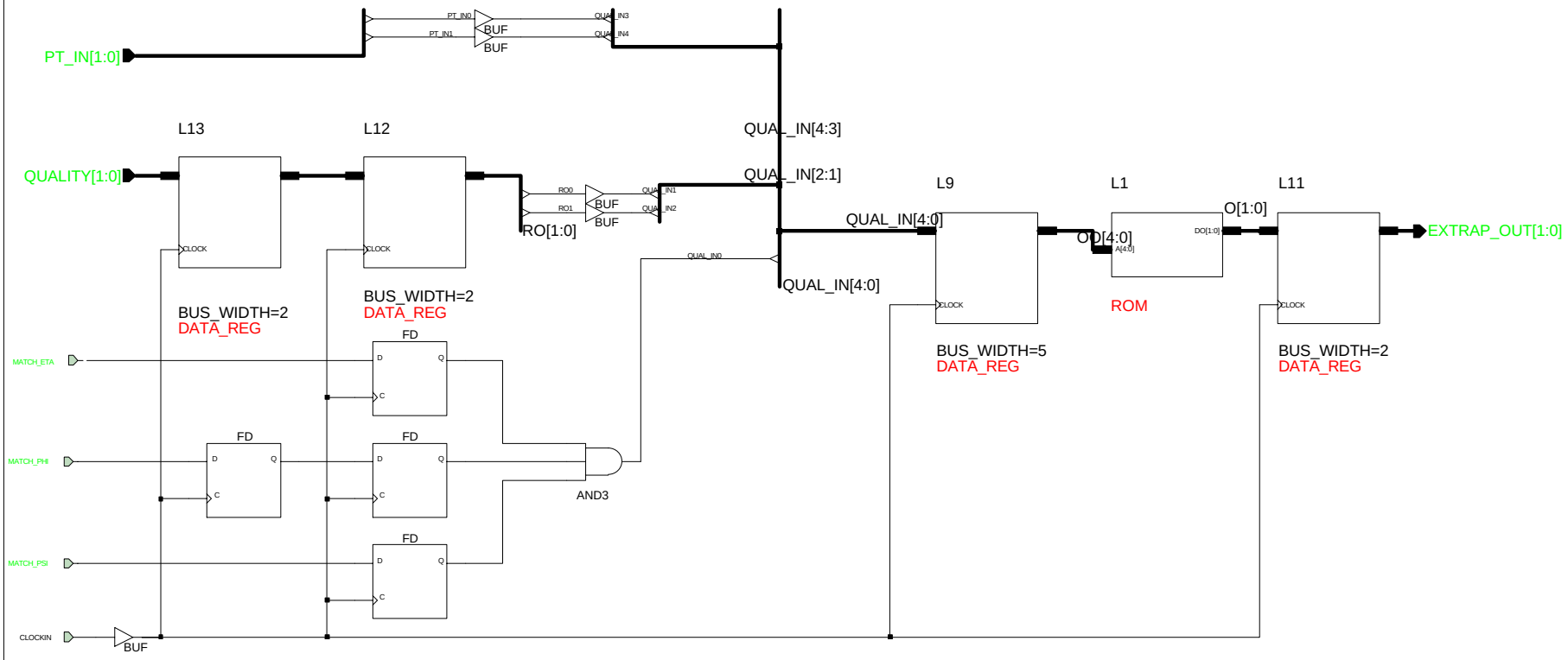


- Limits Δφ vs. η
- Assigns 2-bit P_T word

Ψ, $\Delta\varphi$ Correlation Unit



Quality Assignment Unit



Assigns internal 2-bit quality word for extrapolation result (0 = no match)

Quality Assignment

University of Florida	Project: EXTRAPX1
Department of Physics	Macro: QUALASSIGNMENT
Acosta	Date: 09/15/98

FPGA Logic Size

- One extrapolation unit (correlation of two stubs) takes approximately 200 logic blocks in Xilinx (~5000 gates) including all look-up memories

- Current ideas on partitioning indicate that about 25 extrapolations must be done in one FPGA
  - Need about 250 I/O pins
  - Need 125000 gates $\Rightarrow$ Xilinx XC40125XV
  - Largest FPGA available, highest cost
  - Performance/cost trend is rapidly increasing, however
  - State-of-the-art FPGAs may run logic at 80MHz, which would save latency

- Extrapolation logic is density limited, not I/O limited

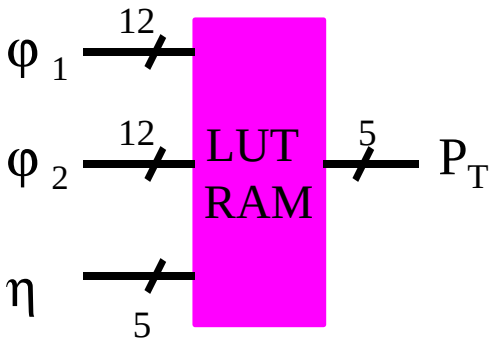
Track Assembly Logic

- The scheme to assemble 2-station extrapolations into longer tracks is under study.

- Presumably this step is similar to the Vienna design, except that additional cuts based on internal quality bits may be applied (such as P_T consistency)

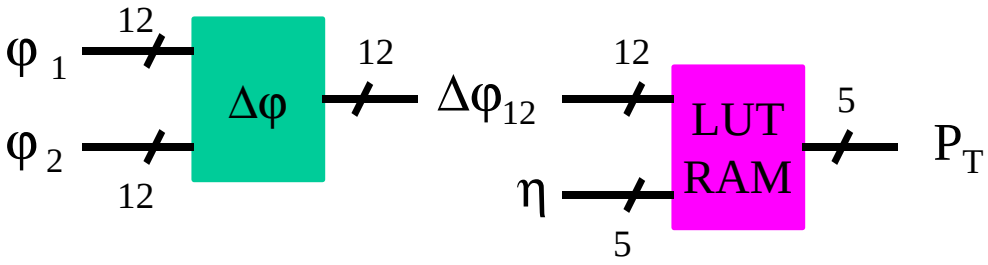
P_T Assignment

⇒ Size of single LUT is prohibitive



⇒ $2^{12+12+5} = 0.5 \times 10^9$ ($\times$ 5 bits)

⇒ Cascade logic:



⇒ Arithmetic unit adds 1 b.x. latency, but could use fast cascaded SDRAM instead

Features of CSC Sector Processor

- Trigger logic is tunable
  - Content of memory LUT is programmable
  - Any correlation unit can be set to accept all inputs
  - For example, track-finding in η can be switched off
- FPGA technology allows flexibility in logic design
- No extra latency with respect to DT-SP in the extrapolation units to include η dependencies (just additional correlations in parallel)
- Design should evolve into the same hardware for the overlap and endcap regions (semi-unified design)
  - Similar number of inputs
  - Complementary approach to overlap region

Differences from Vienna Design

- 3D vs. 2D Track-Finder
  - η information incorporated into extrapolation logic, rather than handled separately
  - Stronger rejection of fake tracks
- P_T assignment uses η information
- No inputs from neighboring φ sectors or η wheels
  - Chambers project in φ, and Port Card collects all η
- Less input to processor (400 signals vs. 800) even with η information
- Design is limited by the size of the logic and look-up memories rather than by the I/O count

CSC Sector Processor Limitations

- Ghost capability not implemented
  - Extrapolation logic increases 3-fold provided we predetermine which two stubs come from the same chamber (more latency), otherwise 9-fold increase
  - Alignment corrections will be invalid
  - More internal bits for bookkeeping

- Out-of-time station hits not implemented
  - Extrapolation logic increases by a factor 2N-1 for N b.x. (3-fold for 2 b.x.)
  - Straightforward to implement, no extra latency

Muon Sorting

- Latest Vienna/Bologna proposal requires two stages of muon sorting following the Sector Processor :
  1. "Wedge sorter" reduces muon candidates from Sector Processors to best 4
  2. Global Muon Trigger "sorter" collects 4 candidates each from DT, CSC, and RPC and send best 4 to Global L1 trigger

- How many muons to sort in (1) for CSC-only?
  - 2 μ / 60° × 360° × 2 endcaps = 24 μ
    (same as for DT wedge sorter, use same hardware?)
  - 3 μ / 60° × 360° × 2 endcaps = 36 μ
- How many muons to sort in (1) for CSC + OVL?
  - 2 μ / 60° × 360° × 2 endcaps × 2 crates = 48 μ
  - 3 μ / 60° × 360° × 2 endcaps × 2 crates = 72 μ

- Possible to combine stages (1) and (2) ?
  - Might save latency

- Bologna will design DT wedge sorter and Global Muon Trigger depending on funding
- Who designs CSC sorter? How to fund?

Future Work

- Validate Track-Finder scheme with CMSIM study
  - Check for holes in acceptance
  - Calculate P_T resolution
  - Determine trigger rate
  - Check efficiency of di-muon (and tri-muon) trigger

- Tune parameters of Track-Finder
  - Quality assignment algorithms
  - Number of internal quality bits
  - Forward and backward extrapolation in φ
  - Number of η bits for track-finding in η
  - Sorting criteria

- Start prototype design
  - Board layout
  - I/O connections (backplane design, choice of connectors)
  - VME Crate (most likely start with CDF VIPA crate)