The Track-Finding Processor for the Level-1 Trigger of the CMS Endcap Muon System

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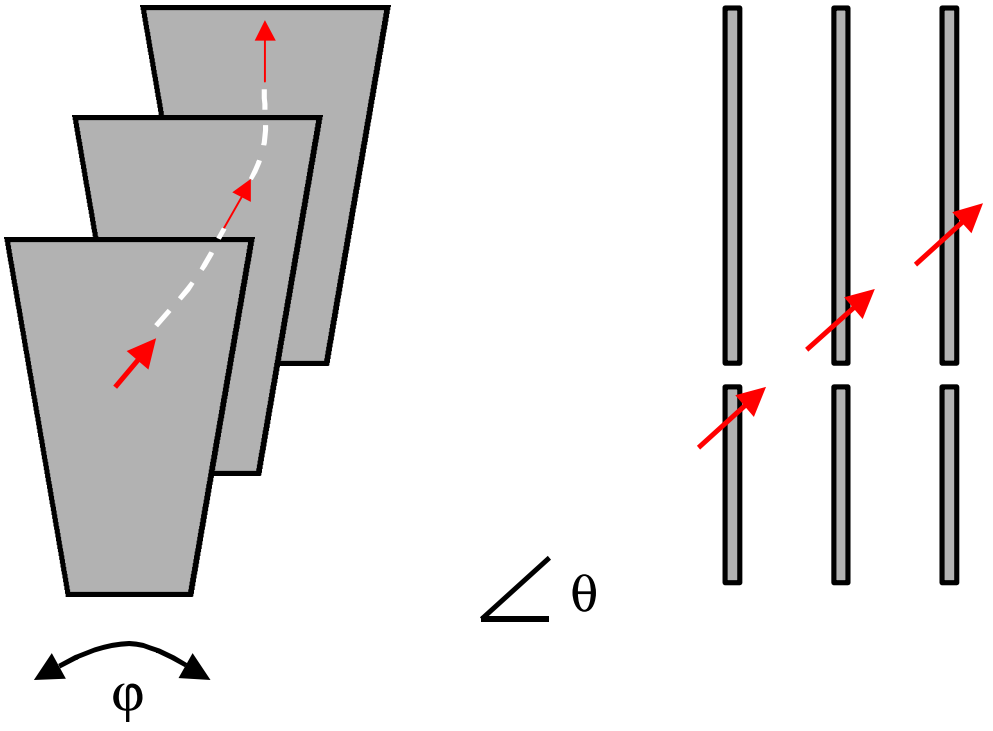
Muon Track-Finding

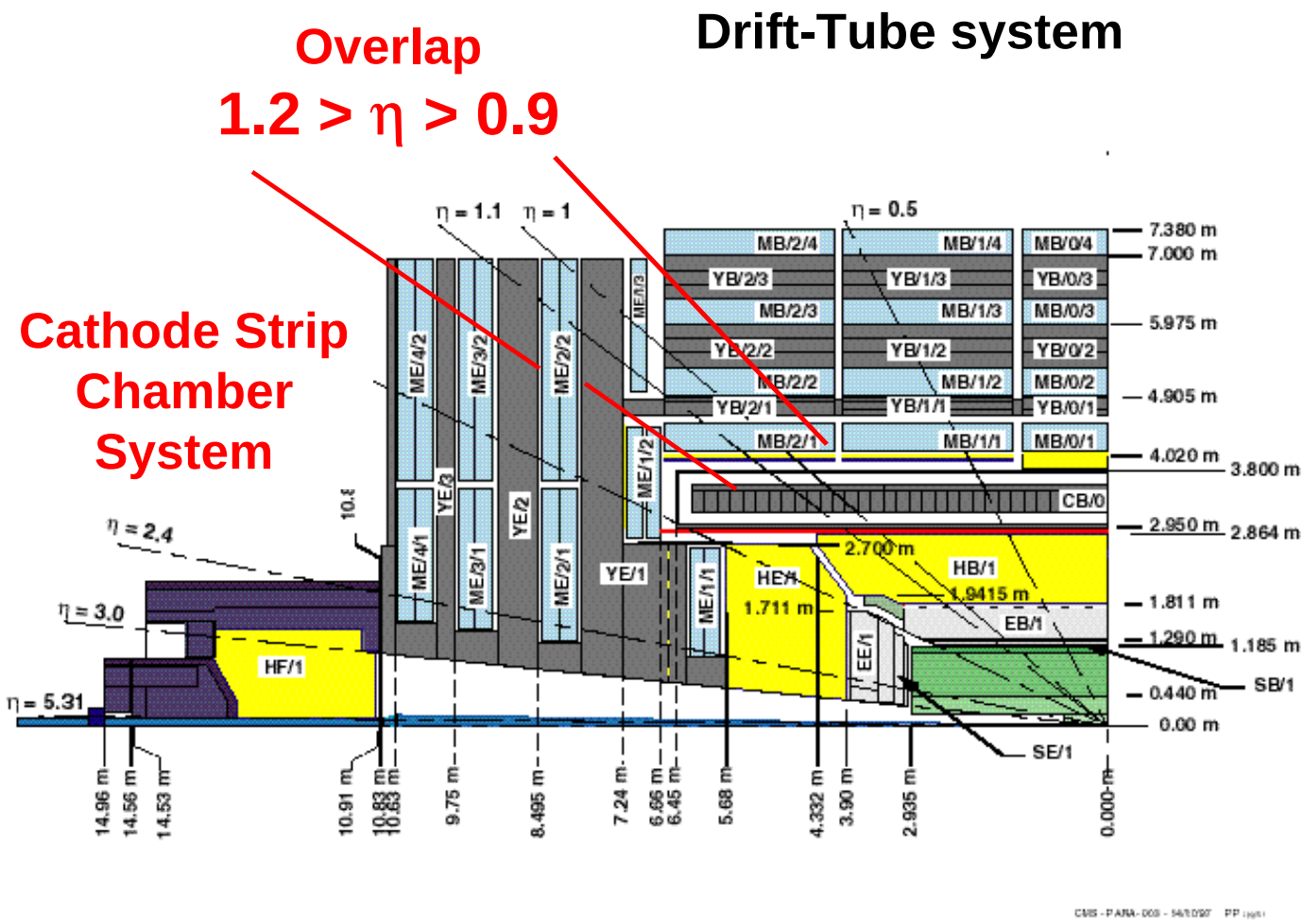
- Perform 3D track-finding from trigger primitives
- Measure P_T , φ, and η
- Transmit highest P_T candidates to Global Level-1



Track-Finder Requirements

- High efficiency with low P_T threshold
- Single muon trigger rate < few kHz at $L=10^{34}\ cm^{-2}s^{-1}$
  - Should have large safety factor
- P_T resolution ≈ 20%
  - Require φ, η information from 3 muon stations
- Multi-muon capability
  - ≤ 3 muons per 60° azimuthal sector
  - Best 4 muons overall sent to Global Level-1 Trigger
- Pipelined and deadtime-less
  - 40 MHz B.X. frequency
- Minimal latency
  - < 16 B.X. (400 ns)
- Programmable
  - FPGA and RAM implementation

Trigger Regions in h



- 4 muon stations in each endcap
- Each station contains 6 layers of CSC chambers
- P_T measured from fringe field of 4 T solenoid using 3D track segments in each station

Trigger Regions in j

Track-Finding performed in independent 60° sectors

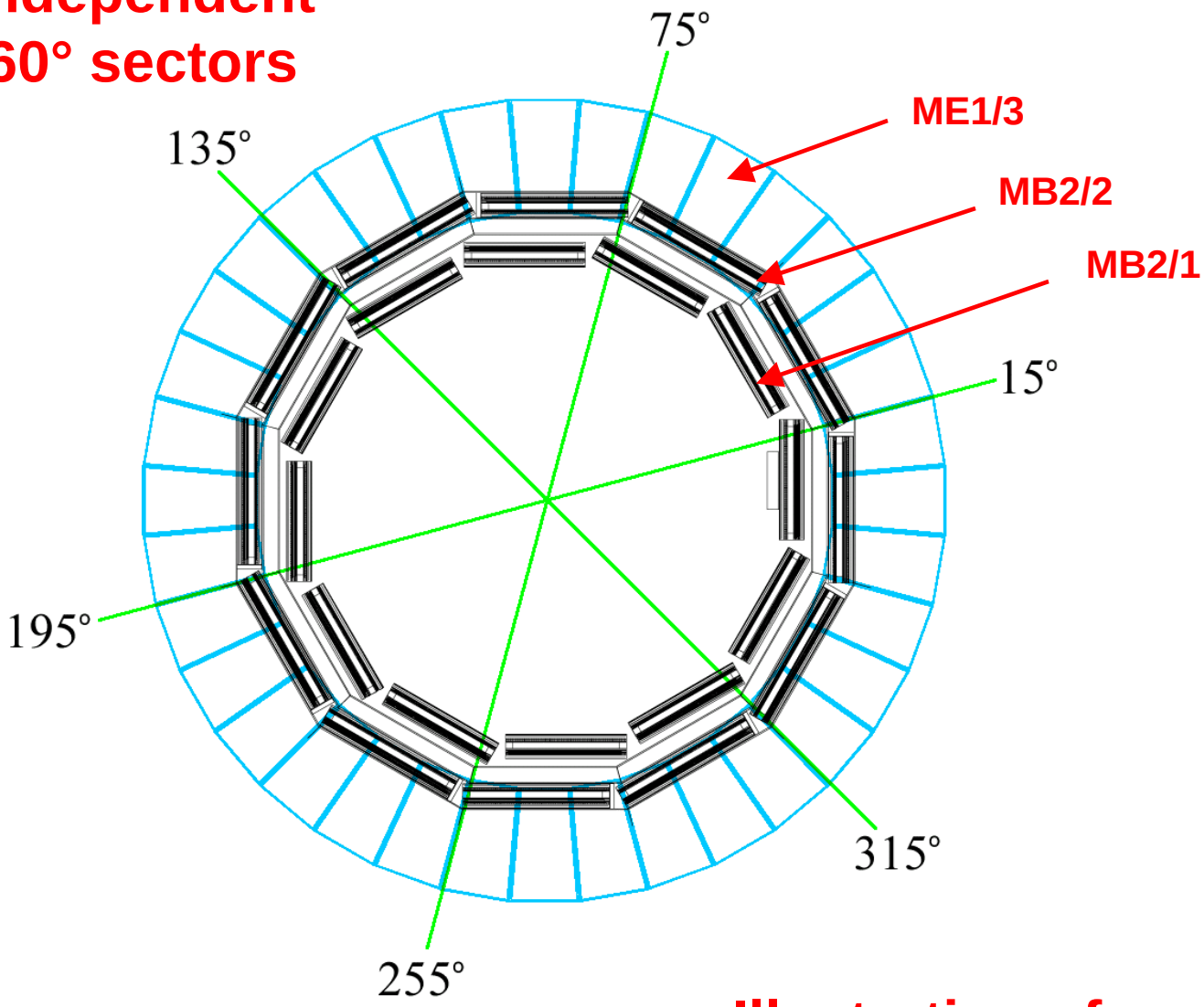


Illustration of overlap region

Why Two Muon Track-Finders?

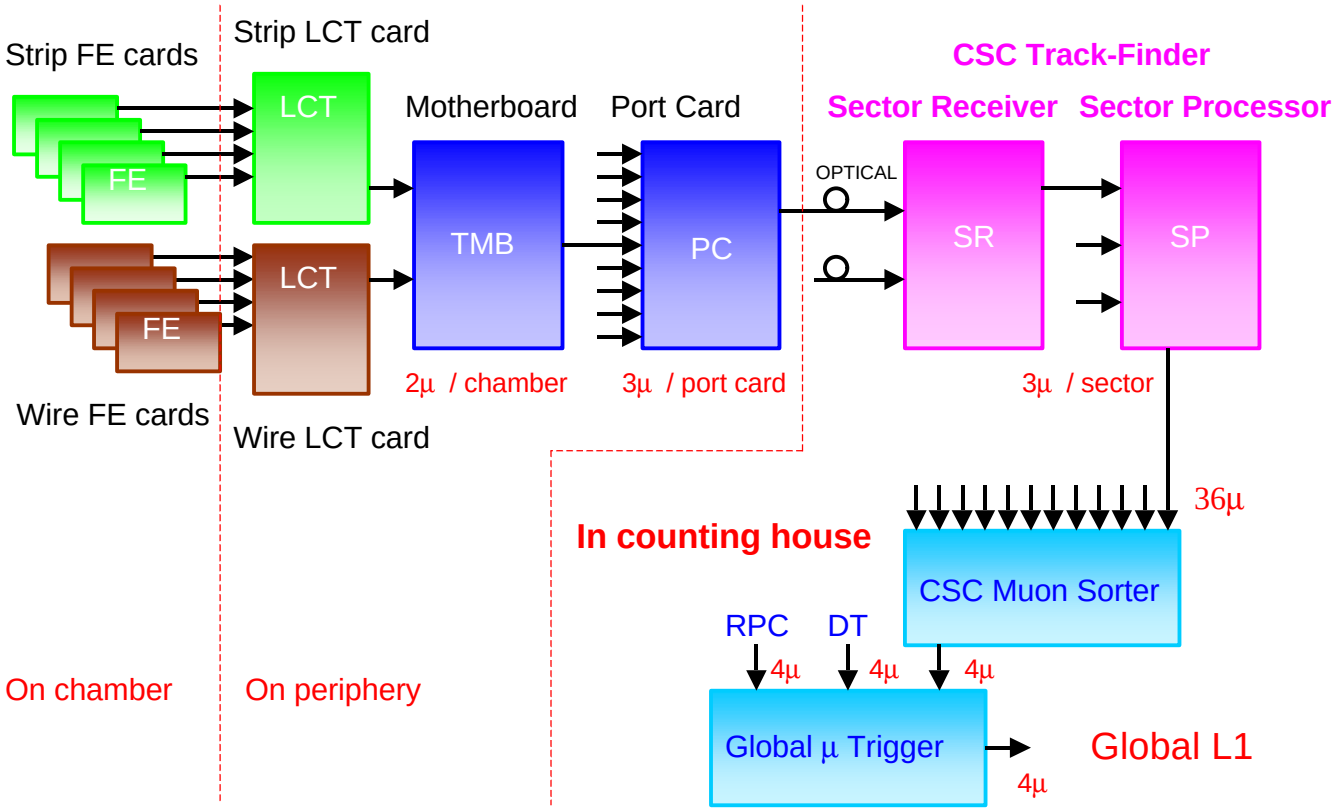
- The Barrel Track-Finder:
  - intrinsically 2D
    - road-finding in φ only (expect low rates)
    - uniform magnetic field in central region
  - large number of neighbor interconnections
    - chambers are staggered, non-projective

- The Endcap Track-Finder:
  - intrinsically 3D
    - road-finding in φ and η to reduce backgrounds
    - non-uniform magnetic field in endcap
  - No interconnections between trigger sectors
    - chambers are projective in φ
    - small bending in endcap

- Therefore, different needs in each region imply two different designs

- Must ensure that fake double triggers do not occur in region of overlap

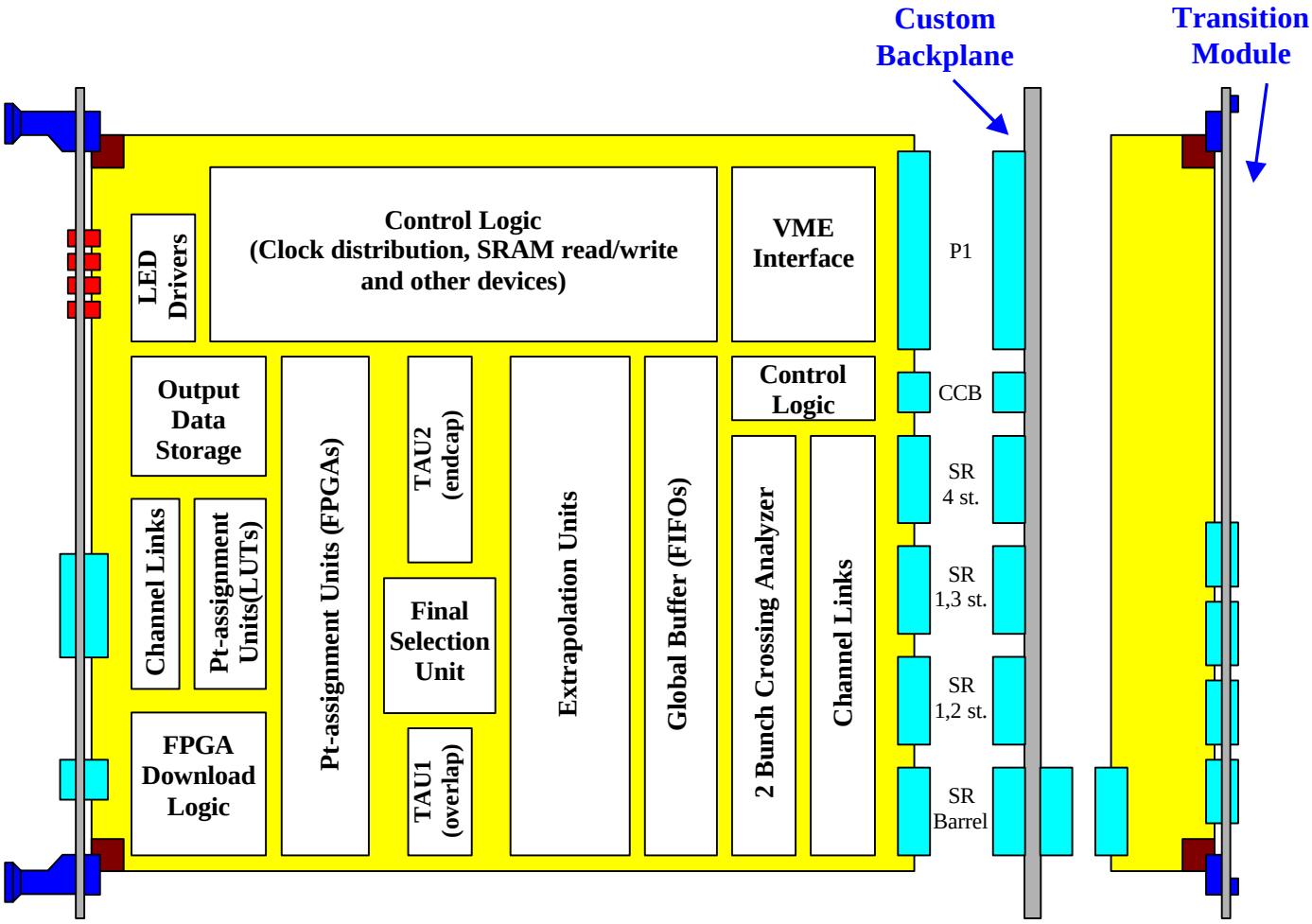
Level-1 Trigger Scheme



Track-Finder Architecture

- Track-Finder implemented as 12 Sector Processors
- Each Sector Processor:
  - Implemented on a 9U VME card
  - Processes 15 CSC segments and 8 DT segments
  - Identifies ≤ 3 muons per 60°
- CSC data received by 3 Sector Receiver cards
  - Each receives 6 track segments on optical links
  - Reformats data to φ, φ_b , η
  - Applies alignment corrections
  - Communicates to Sector Processors via custom point-to-point backplane
  - Presently under development at UCLA
- DT data sent to transition board at back of crate
- Custom point-to-point backplane:
  - Delivers ~600 bits every 25 ns (3 GB/s)
  - Operates at 280 MHz to reduce connections:
    - National Channel Link 28:4 serialization
  - Presently being prototyped in Florida

Sector Processor Layout

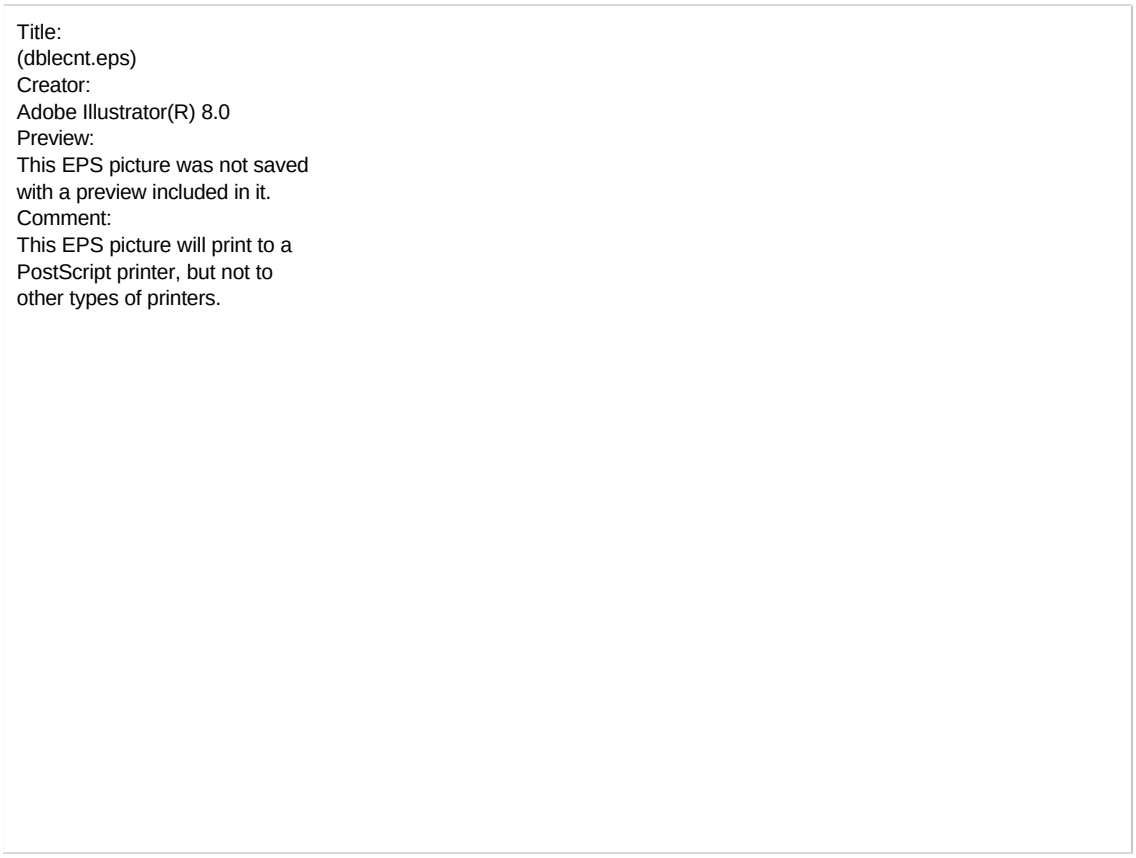


Sector Processor Logic

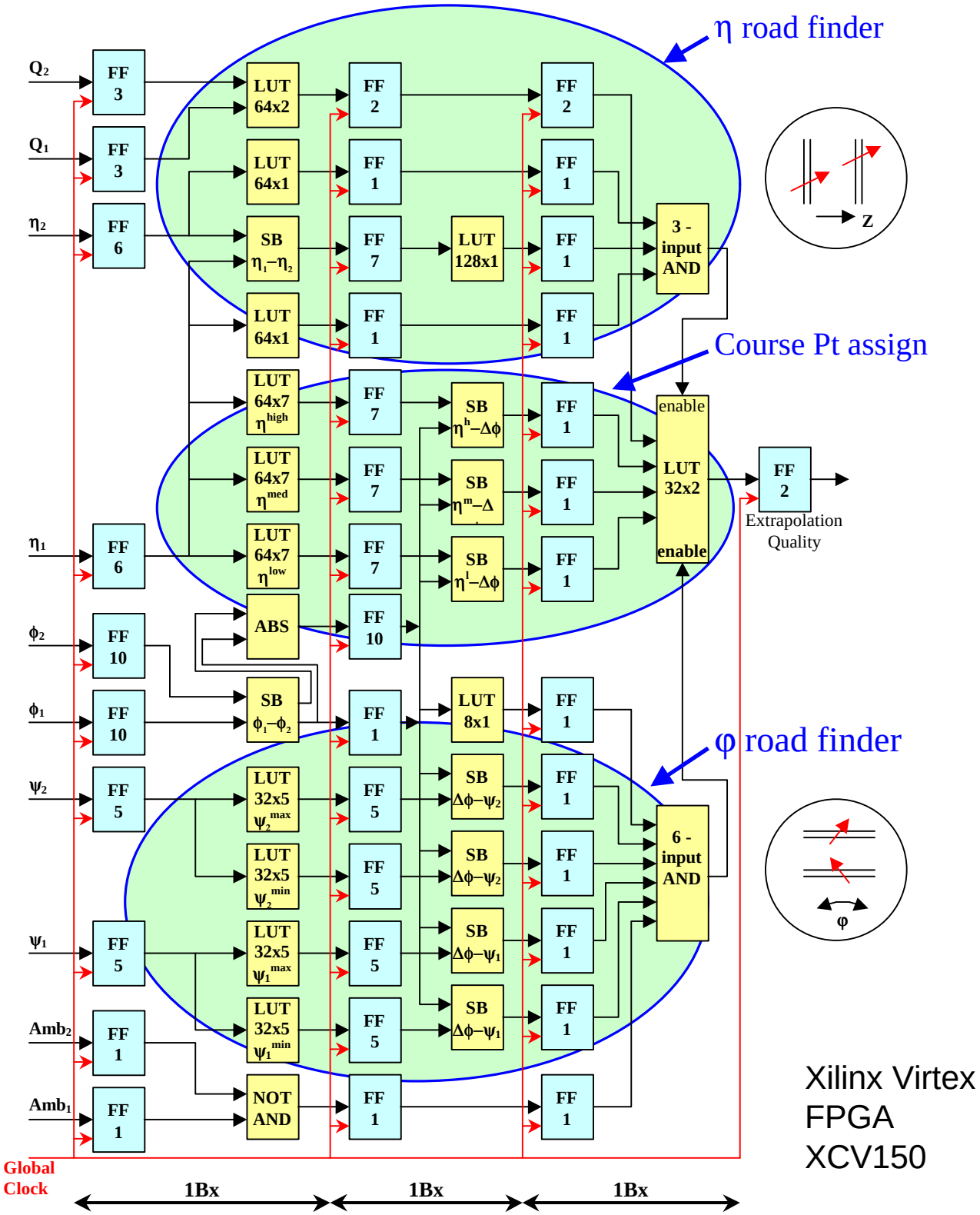
- Latch input and hold for possibly more than one B.X.
  - Allows for timing errors from trigger primitives
- Perform all possible station-to-station extrapolations in parallel
  - Simultaneously search roads in φ and η
- Assemble 3- and 4-station tracks from 2-station extrapolations
- Cancel redundant short tracks if track is 3 or 4 stations in length
- Select the three best candidates
- Calculate P_T , φ, η and send to CSC muon sorter

Two Bunch Crossing Mode

- Input data can be latched for 2 B.X. to accommodate timing errors from trigger primitives
- Sector Processor still reports trigger at correct B.X.



Extrapolation Unit

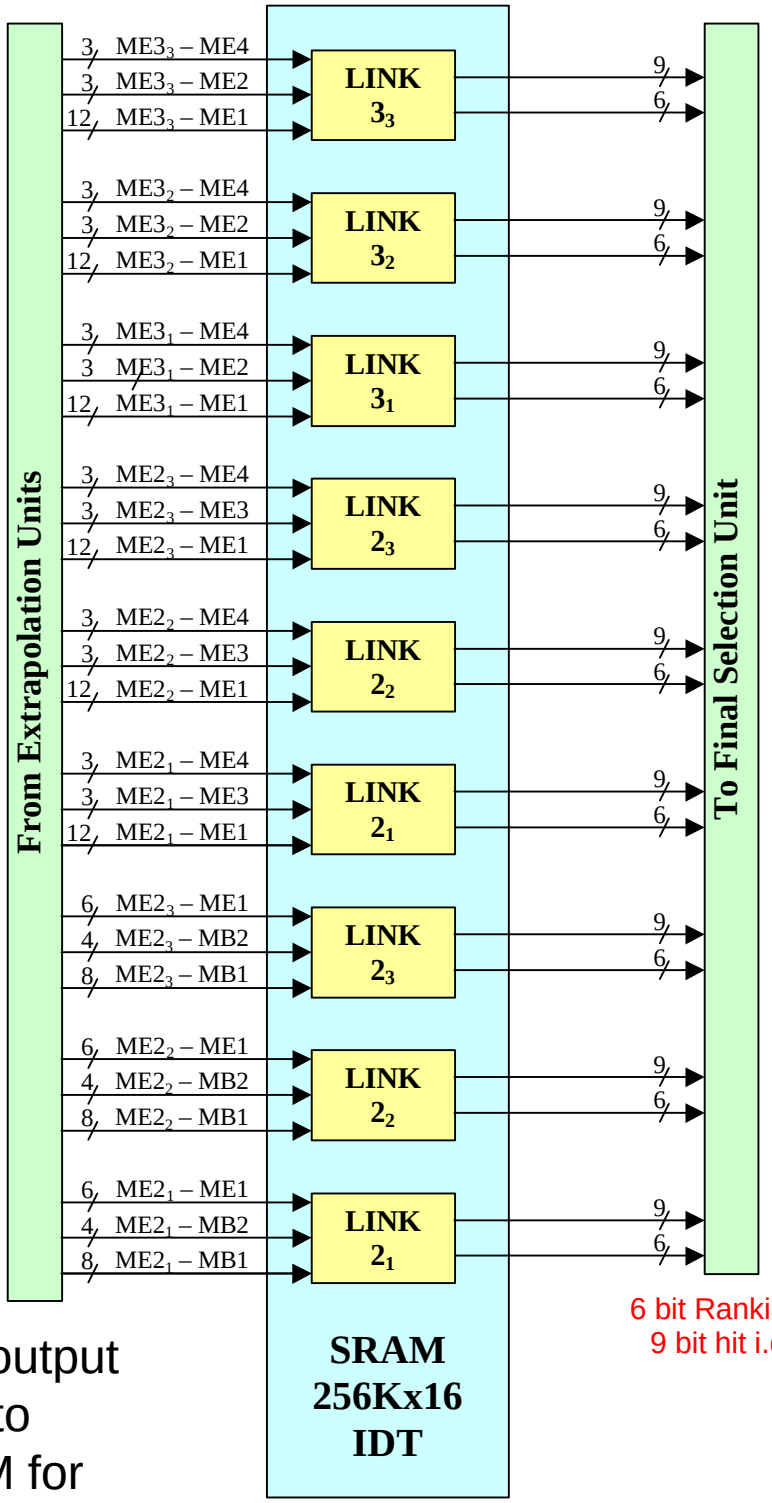


Xilinx Virtex FPGA XCV150

Track Assembly Procedure

Title:
(streams.eps)
Creator:
Adobe Illustrator(R) 8.0
Preview:
This EPS picture was not saved
with a preview included in it.
Comment:
This EPS picture will print to a
PostScript printer, but not to
other types of printers.

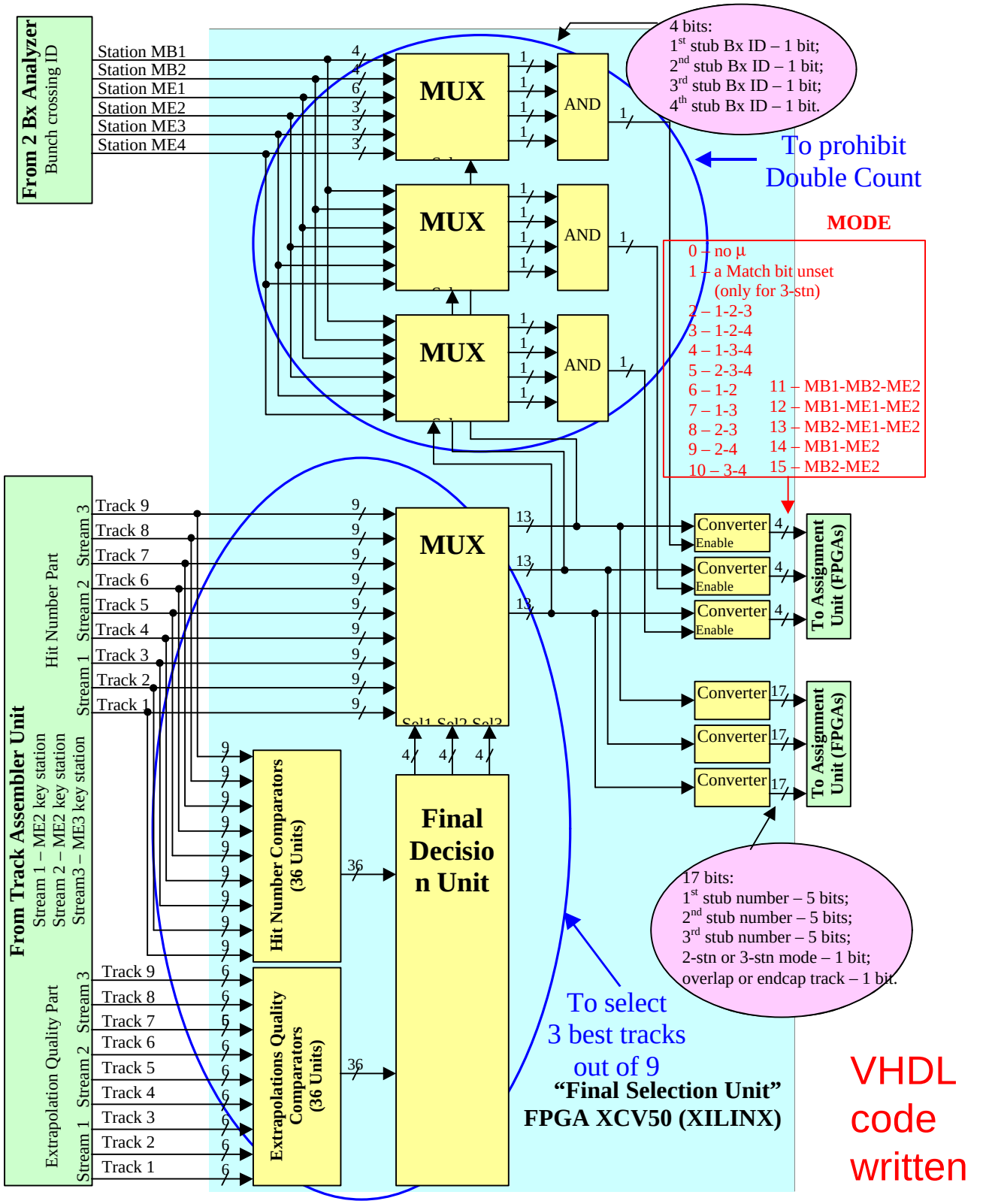
Track Assembler Unit



6 bit Ranking &
9 bit hit i.d. :

Extrapolation output small enough to address SRAM for quick decision

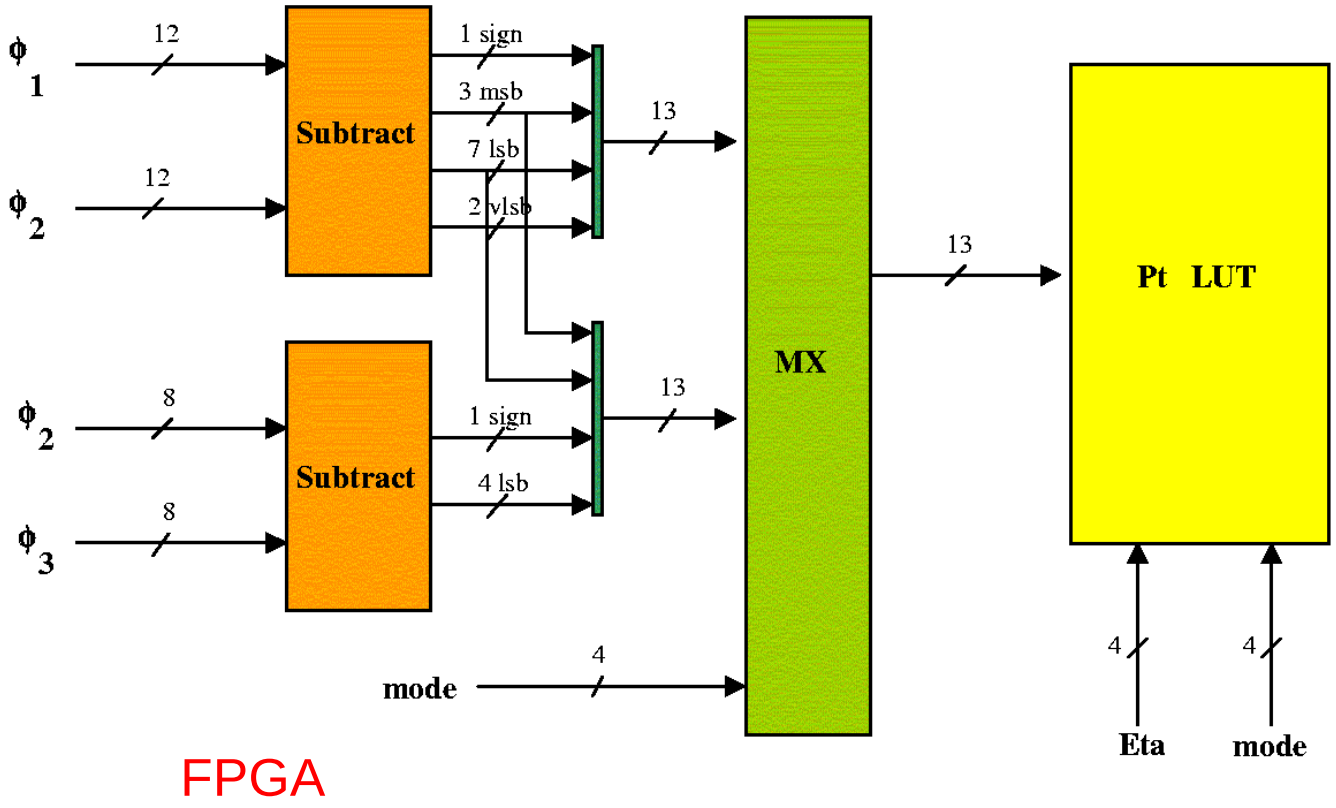
The Final Selection Unit
A Sorter with Cancellation Logic



Assignment Unit

- Determines φ, η, P_T of the selected 3 best muons
- P_T assignment uses φ, η measurements from 2 or 3 stations
  - $\delta P_T/P_T \sim 30\%$ with only 2 stations
  - $\delta P_T/P_T \sim 20\%$ with 3 stations ⇒ improves Level-1 rate reduction
- Implemented with FPGA preprocessing followed by large SRAM look-up table

2Mb×16 SRAM



FPGA

Summary of CSC Track-Finder

- Conceptual design complete
- 12 Sector Processors cover CSC and CSC/DT overlap
  - $1.0 < \eta < 2.4$ and $\Delta\phi = 60°$ on one board
- Track-finding algorithms are three-dimensional
  - Improves background suppression
- P_T assignment includes ϕ,η measurements from 3 stations
  - $\delta P_T/P_T \sim 20\%$ (30% with only 2 stations)
  - Significantly improves rate reduction at Level-1
- Inputs can be latched for 2 B.X.
  - Tolerates timing errors from trigger primitives
- Latency expected to be only 14 B.X.
- Fully re-programmable
- Xilinx Virtex FPGAs and SRAM used
- Board layout and backplane design started