Muon Trigger Electronics in the Counting Room

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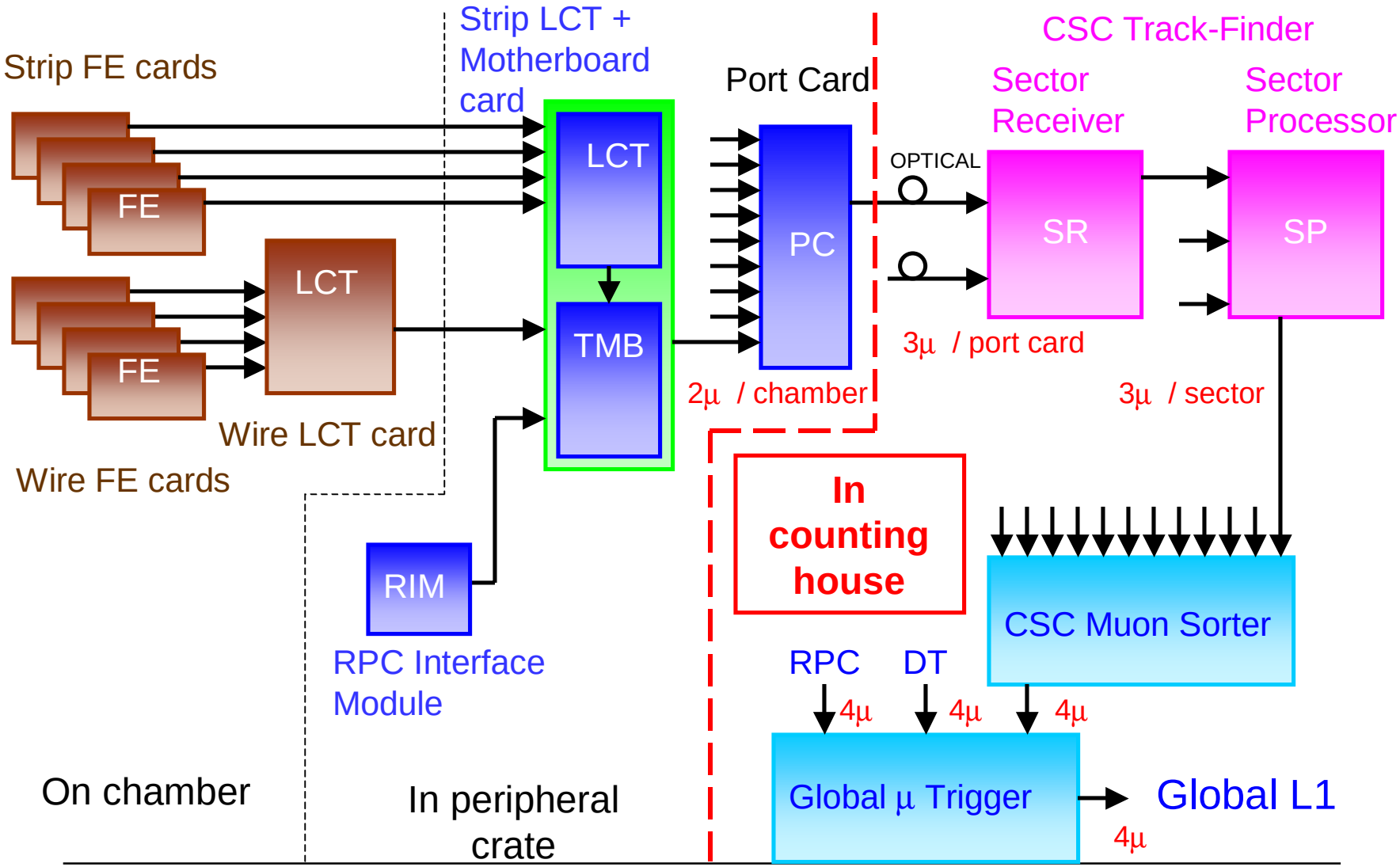
Outline

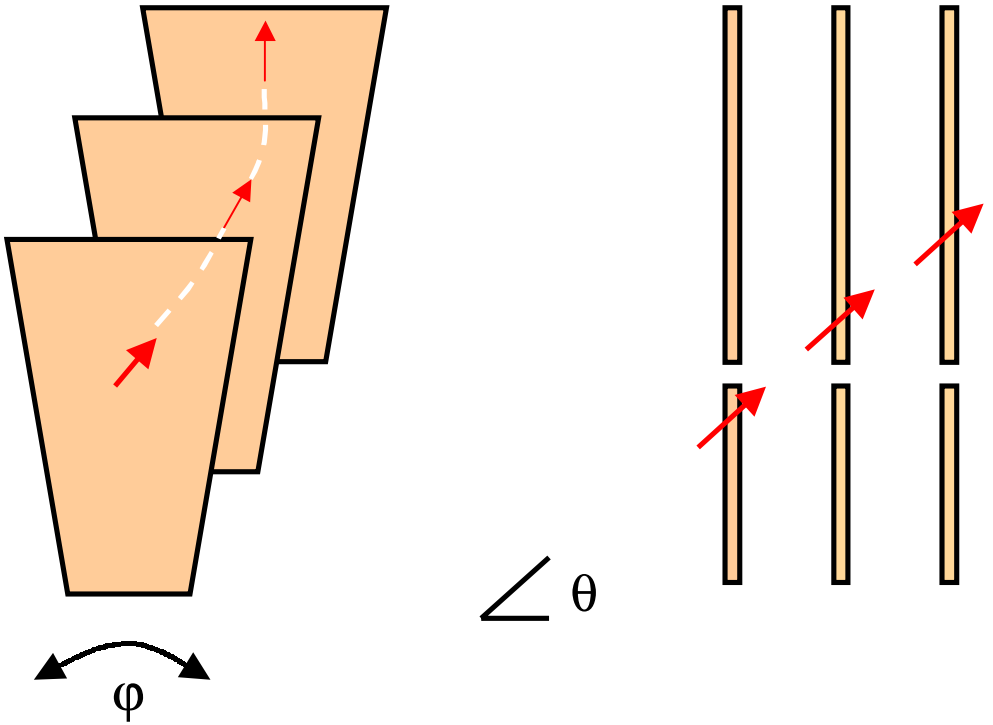
- Overview of the CSC trigger system
- Sector Receiver (WBS: 3.1.1.2)
- Sector Processor (WBS: 3.1.1.3, 3.1.1.4)
- Backplane (WBS: 3.1.1.7)
- Muon Sorter (WBS: 3.1.1.15)
- Schedule

CSC Muon Trigger Scheme



Muon Track-Finding

- Link trigger primitives into tracks
- Assign p_T, φ, and η
- Send highest quality candidates to Global L1



CSC Track-Finder Requirements

High Efficiency

Low Trigger Rate:

- Single muon rate < several kHz at $L = 10^{34}cm^{-2}\ s^{-1}$

Resolution: $\sigma_{Pt} / P_t = 20\%$

- Requires η information (non-uniform B-field)
- Requires ≥3 CSC stations

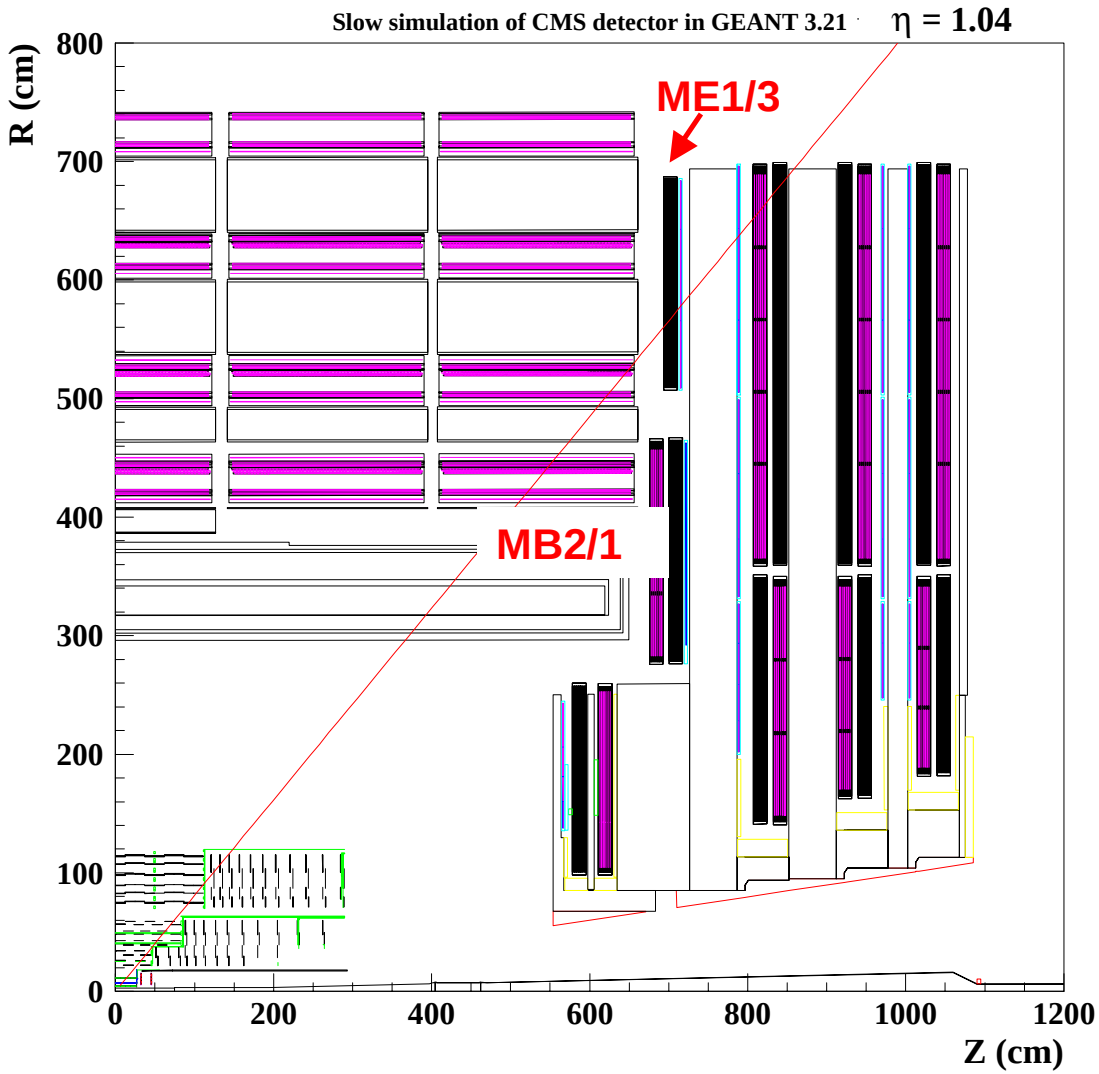
Multi-muon Identification:

- ≤ 3 muons per 60° sector
- ≤ 4 muons total for both endcaps

Programmable

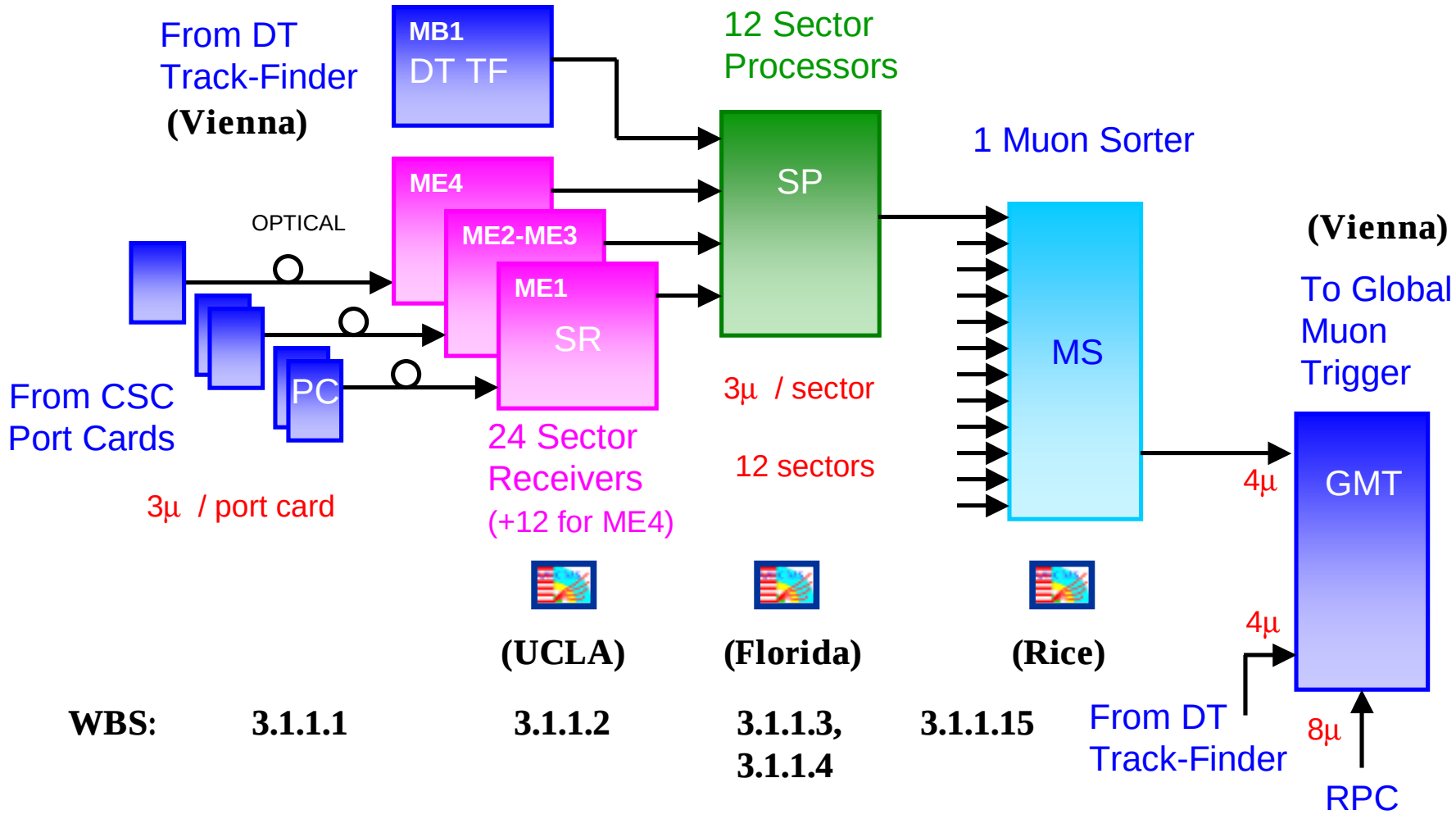
Minimal latency

Separation of DT/CSC Coverage



- Hard boundary defined η=1.04
- Separate Track-Finders optimized for each system
- Information shared across boundary for maximum efficiency
- Agreement with Vienna reached on DT/CSC interface Feb'00

The CSC Track-Finder



Sector Receiver Functionality

UCLA

3.1.1.2

1. **Receive 6 μ segments via 12 optical links from 2 Muon Port Cards**
   - Require 3 Sector Receivers for one 60° sector
2. **Synchronize the data**
3. **Reformat the data into track segment variables**
   - LCT bit pattern $\rightarrow \eta, \varphi, \varphi_b$, ...

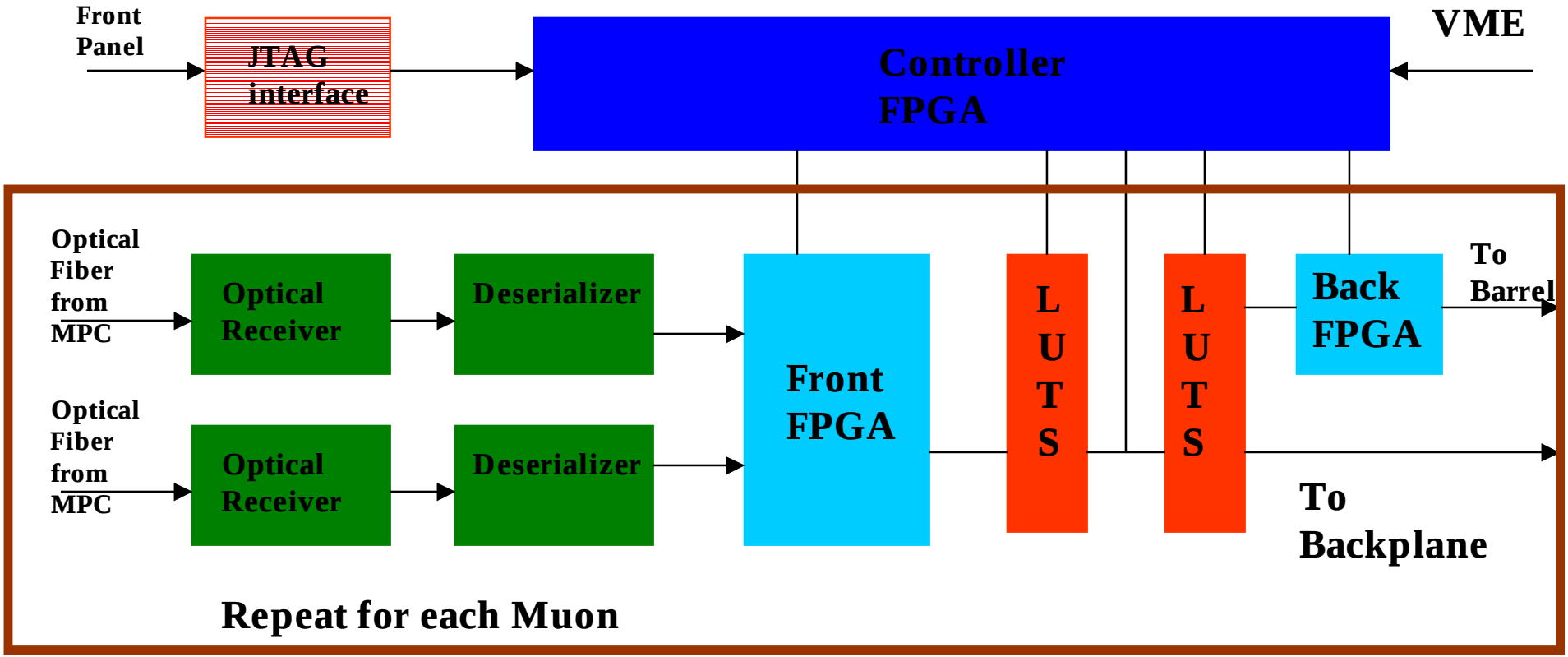
} **via LUTs**

4. **Apply corrections for alignment**
5. **Communicate to Sector Processor via custom backplane (Channel Link)**
6. **Fan out ME1/3 μ segments to DT Track-Finder**

Sector Receiver Logic

UCLA

3.1.1.2



Sector Receiver

UCLA

3.1.1.2

- **Fell behind schedule after postdoc departure.**
- **Personnel added in December/January:**
  - **Robert Cousins, physicist, 50% time**
  - **Vladislav Sedov, electronics engineer, 90% time**
    (10% residual work on ALCT board)
  - **Also using paid consultant for some FPGA work**
    (UCLA CS Ph.D. candidate)
- **Schematics now well underway.**
- **Long-lead-time parts ordered.**
- **Layout planned by beginning of May.**
- **Plan to be ready for summer Track Finder test.**

Sector Processor Functionality

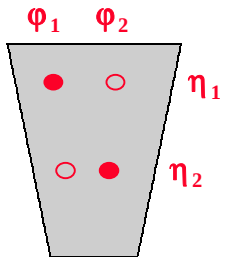
Florida

3.1.1.3, 3.1.1.4

1. **Accumulate** track segments for possibly more than one B.X.
2. **Extrapolate** in 3D from one station to another for all possible track segment combinations
3. **Assemble** tracks from extrapolation results
4. **Select** best 3 tracks and cancel ghosts
5. **Assign** track parameters: p_T, φ, η, quality

New since last Review:

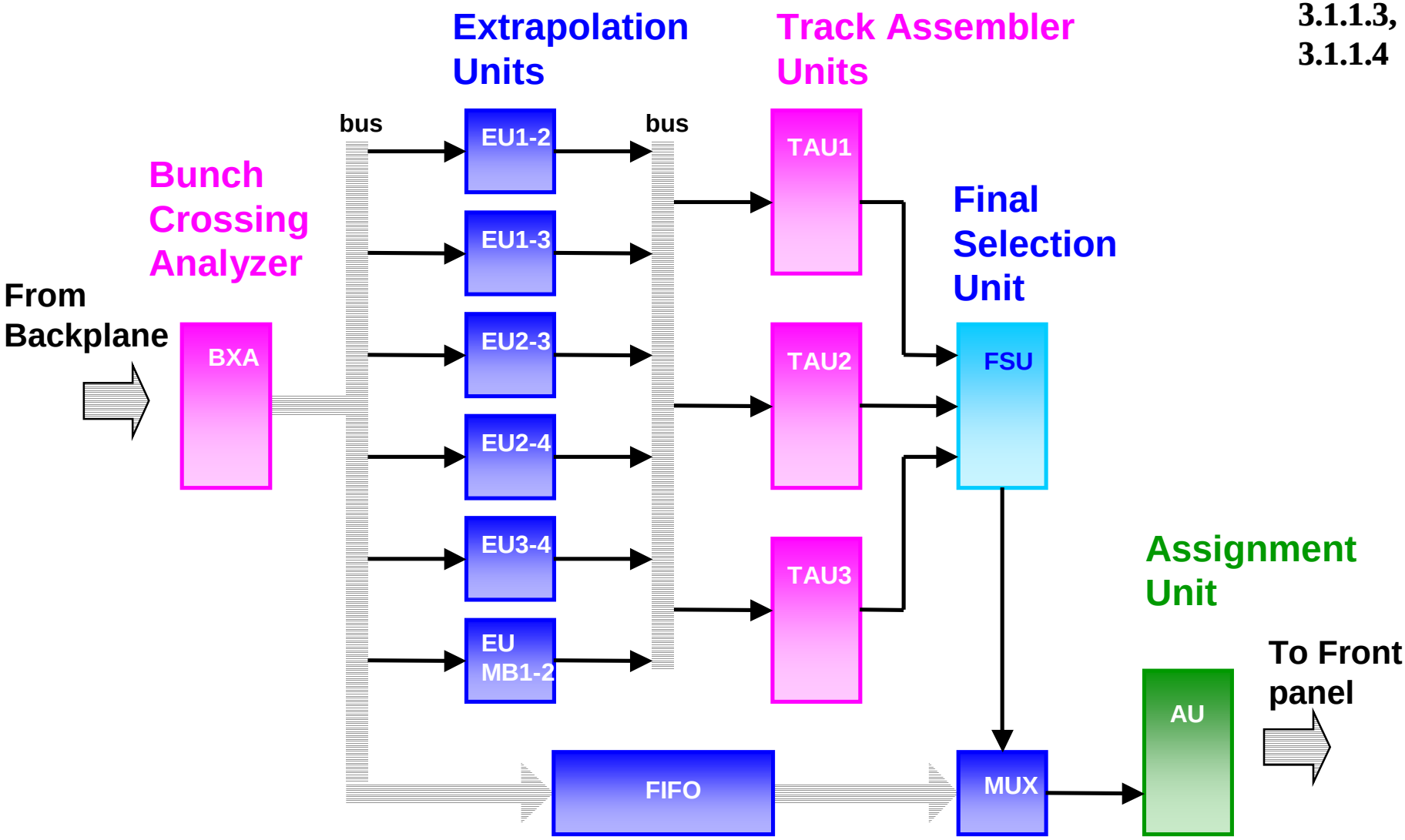
- **Combined DT/CSC overlap region onto same board as CSC-only region (add MB1–ME2 extrap.)**
- **Improved P_T assignment technique**
- **Ghost-busting when 2 muons enter 1 CSC chamber (try all combinations)**



Sector Processor Logic

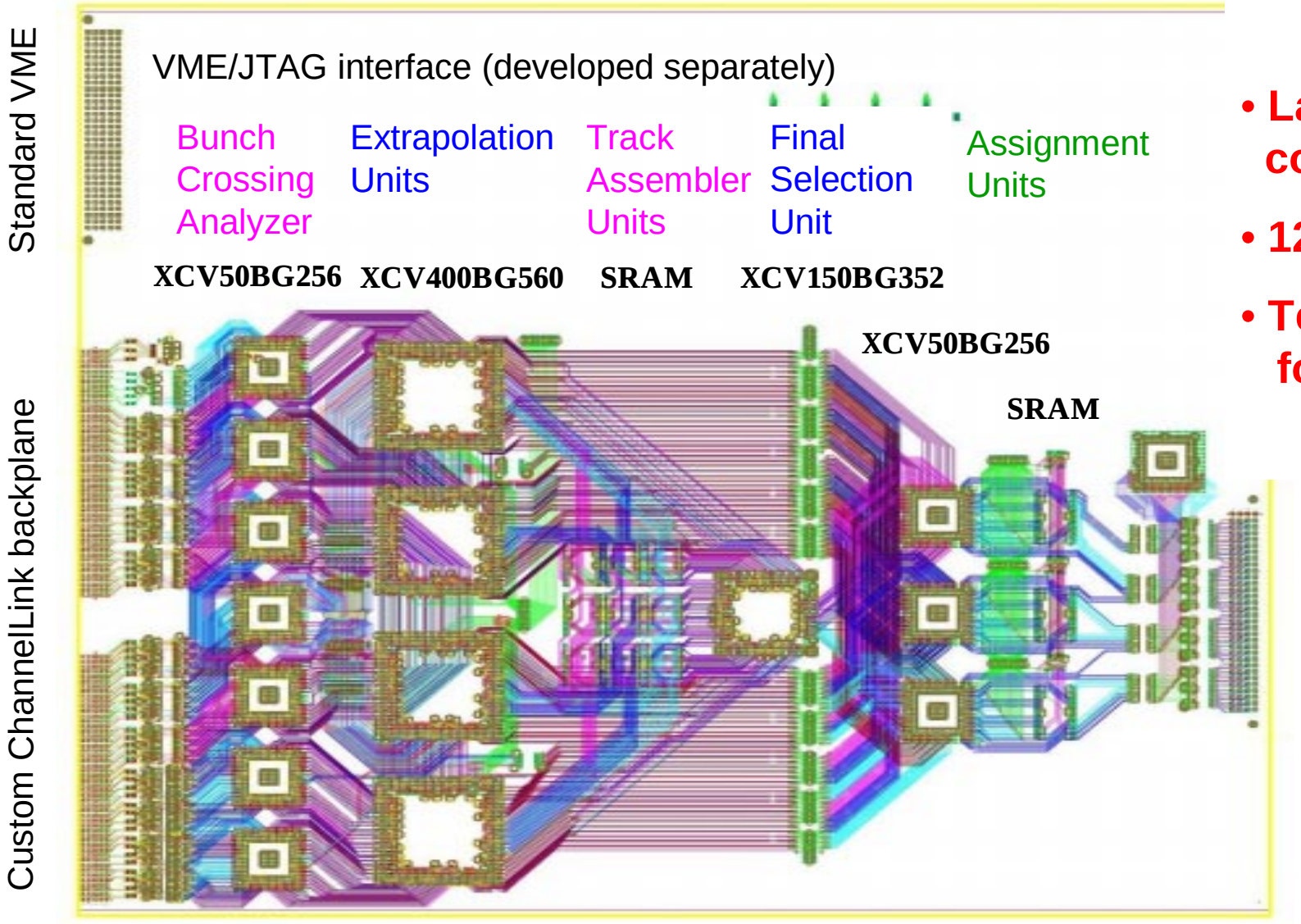
Florida

3.1.1.3,
3.1.1.4



SP Prototype Layout

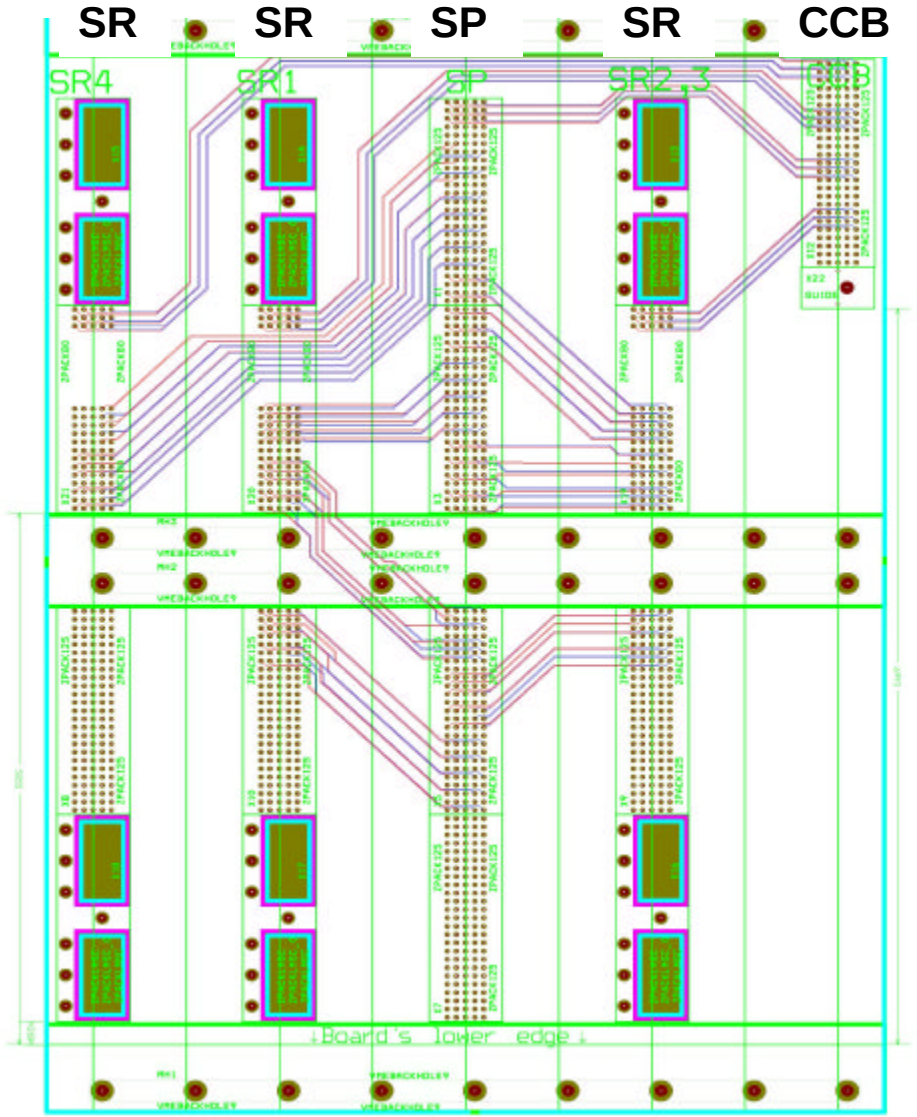
Florida



- **Layout complete**
- **12 layers**
- **Tests set for 6/1/00**

Prototype Crate Layout

3.1.1.7



One sector is half of Track-Finder crate

Six crates for entire system

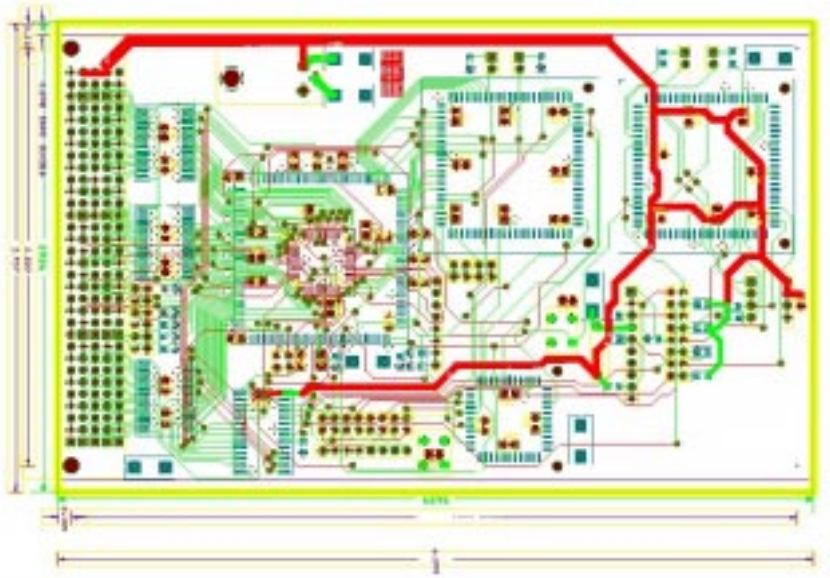
Fully routed for summer tests

Smaller prototype tested already

Pre-Prototype Tests

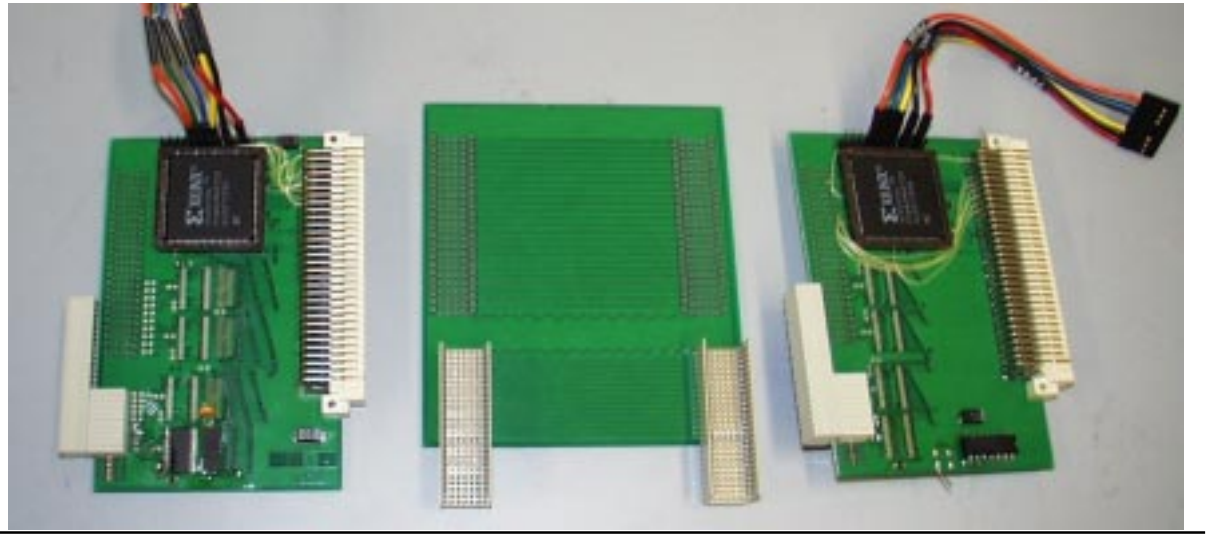
VME / JTAG interface for SR and SP:

Software & hardware for FPGA and SRAM downloading through VME works



Channel Link backplane and connector tests:

No errors found up to 58 MHz clock (400 MHz on backplane)



Muon Sorter Functionality

Rice

3.1.1.15

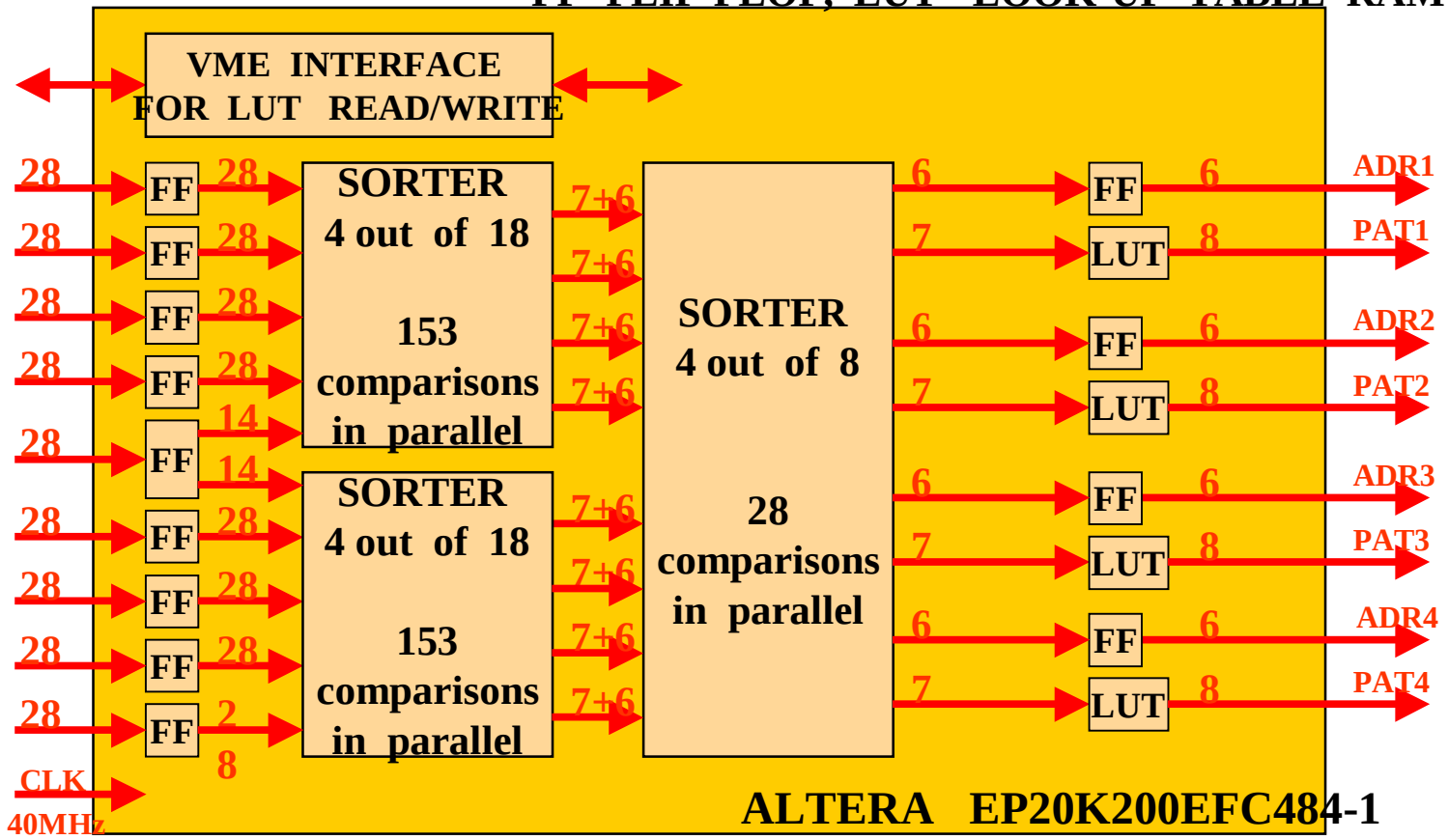
1. **Receive 36 muons from 12 Sector Processors**
   - 36 $\times$ 18 bits = 648 bits (& control bits)
2. **Sort and rank the best 4 muons**
   - Sort is based on 7 bits (5 bits for p_T and 2 bits for quality)
3. **Send the output to the Global Muon Trigger for association with RPC and DT triggers**
   - 4 $\times$ 22 bits = 88 bits

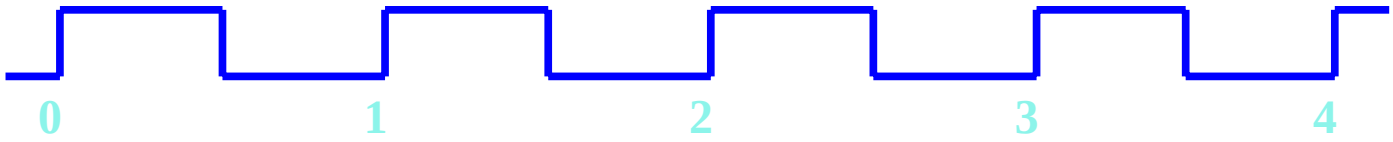
New since last Review:

- **Reduction in muon count from 72 to 36 (inclusion of CSC/DT overlap in Sector Processor) allows sorting to be accomplished in one FPGA**

Muon Sorter Logic

FF- FLIP-FLOP, LUT - LOOK-UP TABLE RAM 3.1.1.15



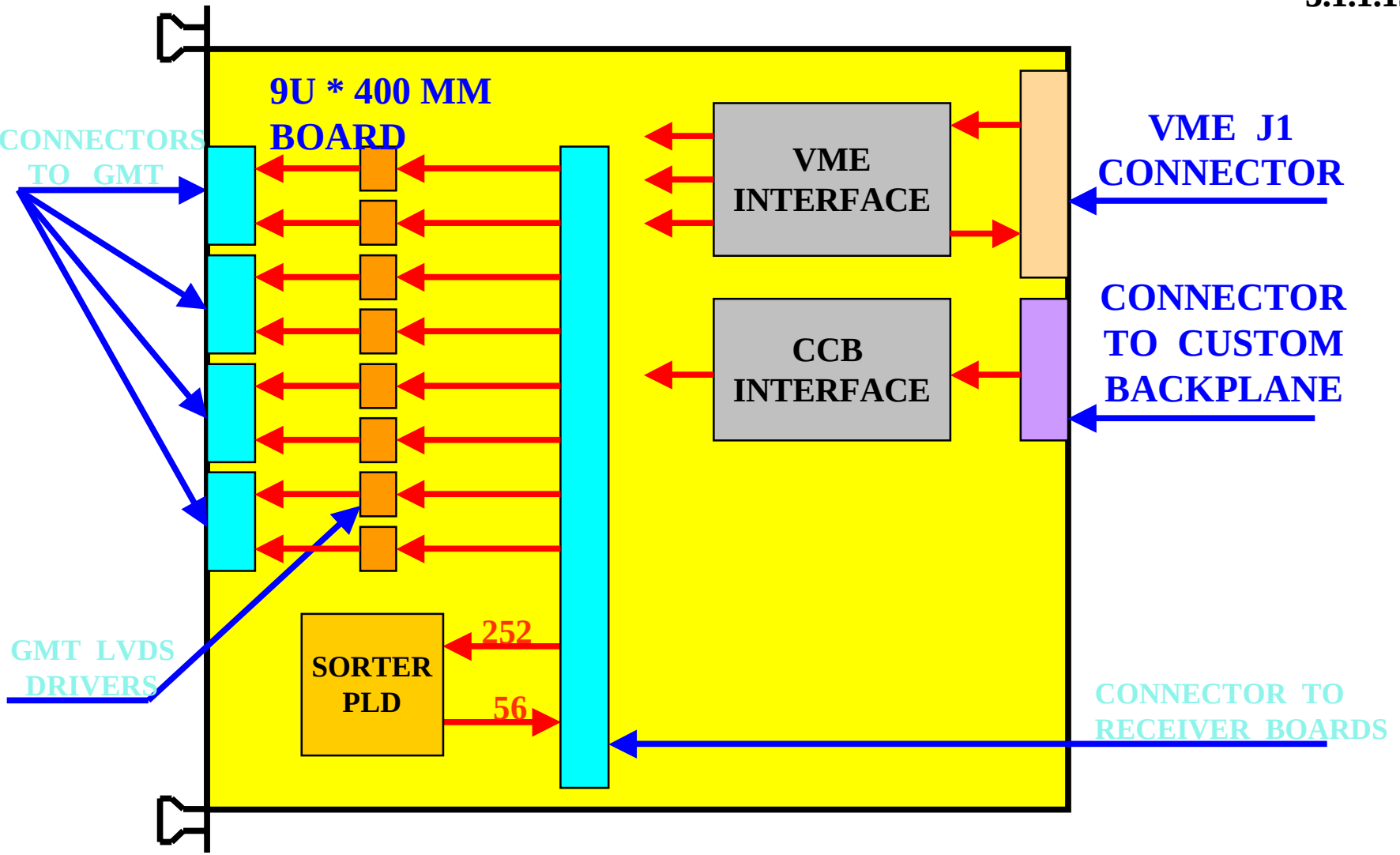


"4 out of 36" SINGLE-CHIP SORTER BLOCK DIAGRAM AND TIMING

Sorter Board Block Diagram

Rice

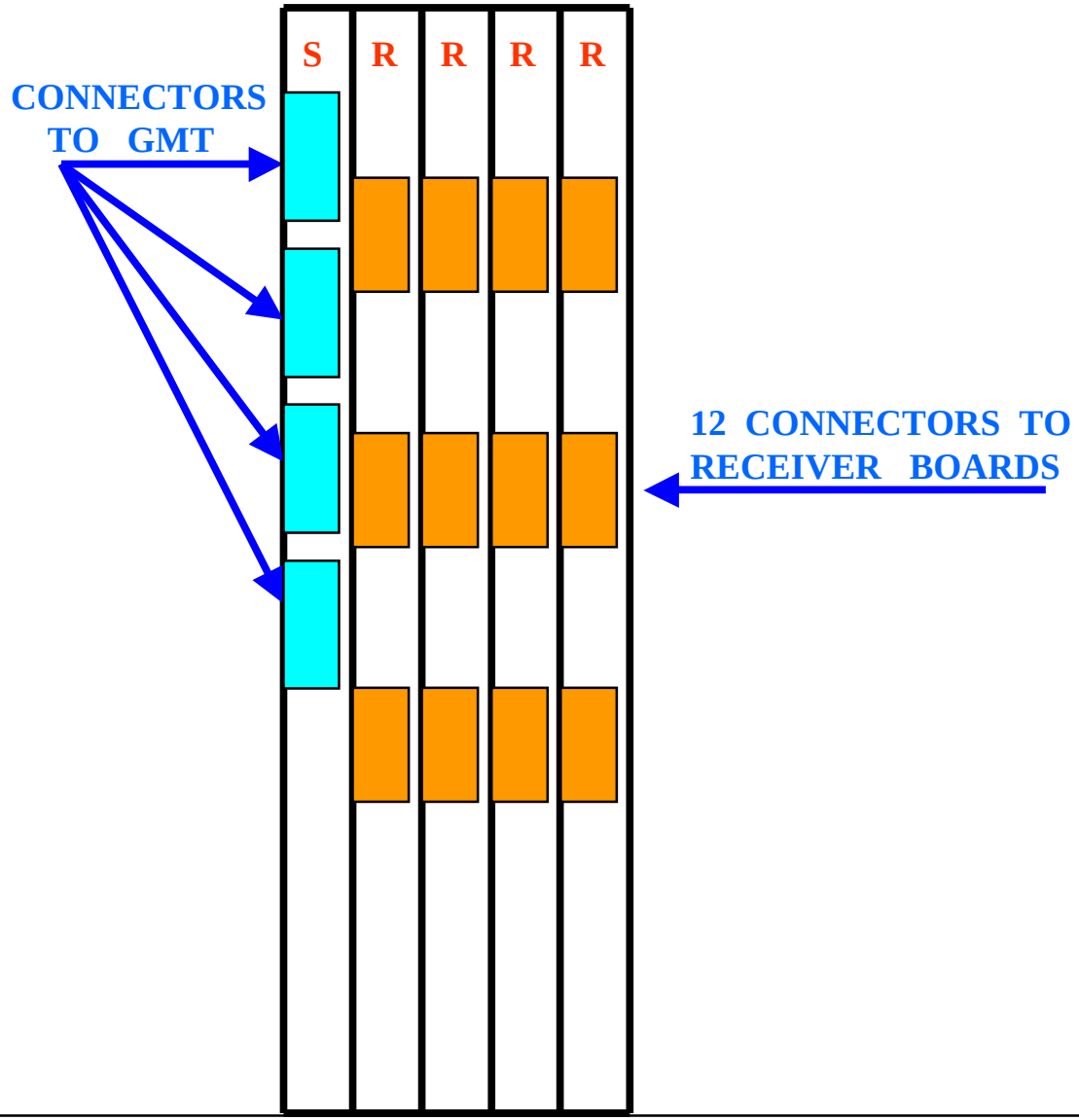
3.1.1.15



Muon Sorter Crate Layout

Rice

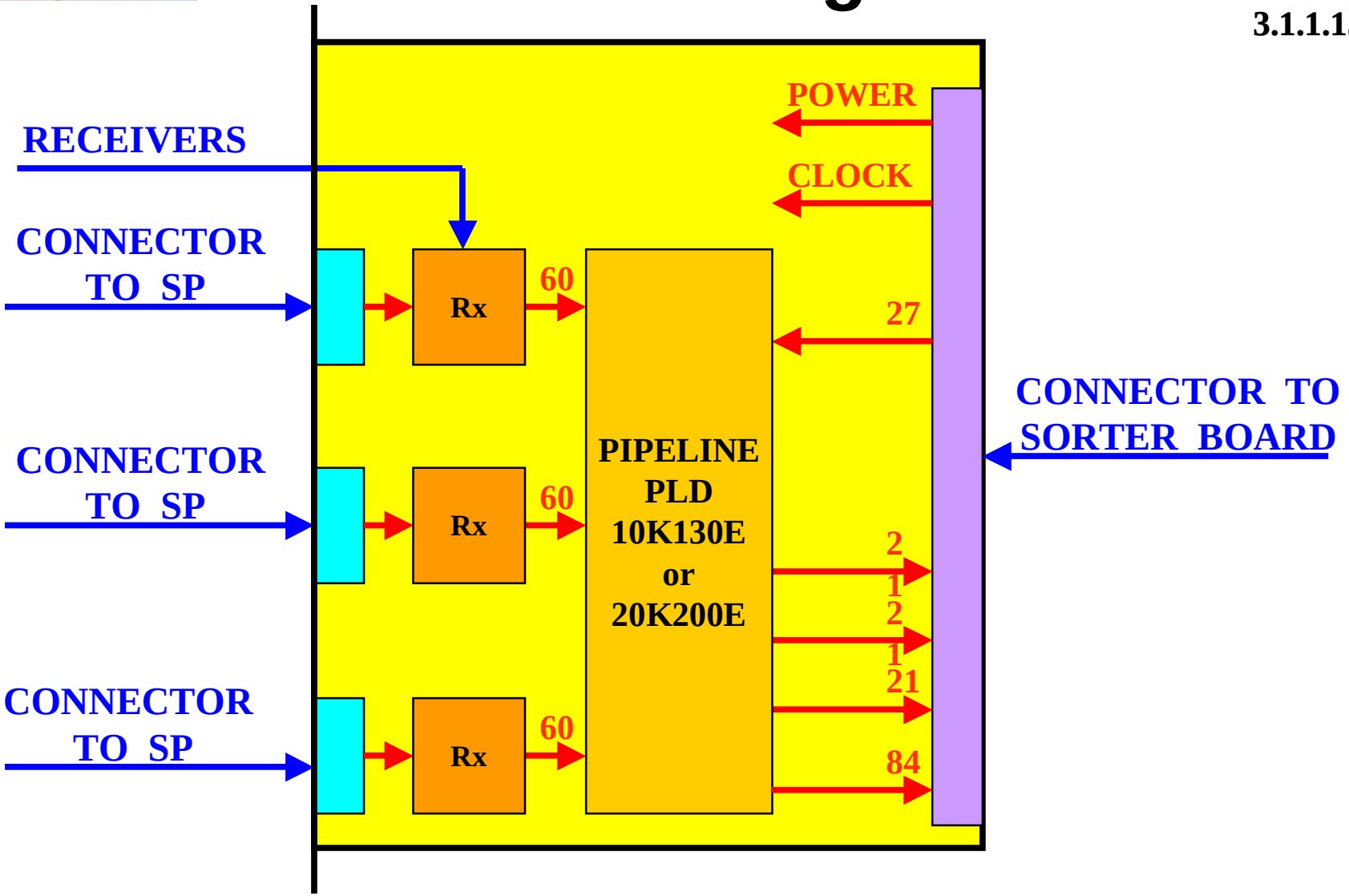
3.1.1.15



Sorter Receiver Board Block Diagram

Rice

3.1.1.15



Summer Plans

Crate test with prototype SR, SP, CCB (and TMB, MPC) scheduled for summer 2000

- Bench tests start June 1
- Integration tests start July 1
- Will test optical link connections and trigger algorithms at 40 MHz, verify output and latency

All designs are proceeding well, and we should be able to make milestone

- Conceptual design, schematics, and some layouts already exist

Development of test software started

Allocated Resources

- **UCLA (Sector Receiver)**
  - Robert Cousins, physicist, co-PI, 0.5 FTE
  - Jay Hauser, physicist, co-PI, 0.5 FTE
  - Benn Tannenbaum, physicist, 0.5 FTE
  - Vladislav Sedov, electronics engineer, 0.9 FTE
  - Consultant for some FPGA work (UCLA CS Ph.D. candidate)
- **Florida (Sector Processor)**
  - Darin Acosta, physicist, PI, 0.5 FTE
  - Song Ming Wang, physicist, 0.5 FTE
  - Alex Madorsky, electronics engineer, 1 FTE
  - Victor Golovtsov, electronics engineer, 1 FTE
  - Boris Razmyslovich, electronics engineer, 1 FTE
  - Alex Atamanchook, electronics engineer, 0.5 FTE
- **Rice (Sorter, Port Card)**
  - B. Paul Padley, physicist, PI, 0.5 FTE
  - Mike Matveev, electronics engineer, 1 FTE
  - Ted Nussbaum, electronics engineer, 0.5 FTE
  - Nick Adams, electronics engineer, 0.5 FTE

Conclusions

Some schedule slippage with Sector Receiver (and Port Card) due to personnel shortage and optical testing

Additional engineering resources assigned:

- UCLA: hired new engineer and consultant
- Rice: hired new engineer (and test optics for SR)
- Florida: hired new engineer & collaborate with 3 engineers at PNPI (provide VME interface for SR)

Additional physicist resources assigned:

- UCLA: Bob Cousins joins, and DOE base support for postdoc
- Florida: DOE base support for postdoc

So, things will definitely heat up in Florida this summer for the pilot test!