Muon Trigger Electronics in the Counting Room

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DOE/NSF Review

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Outline

Overview of System Design

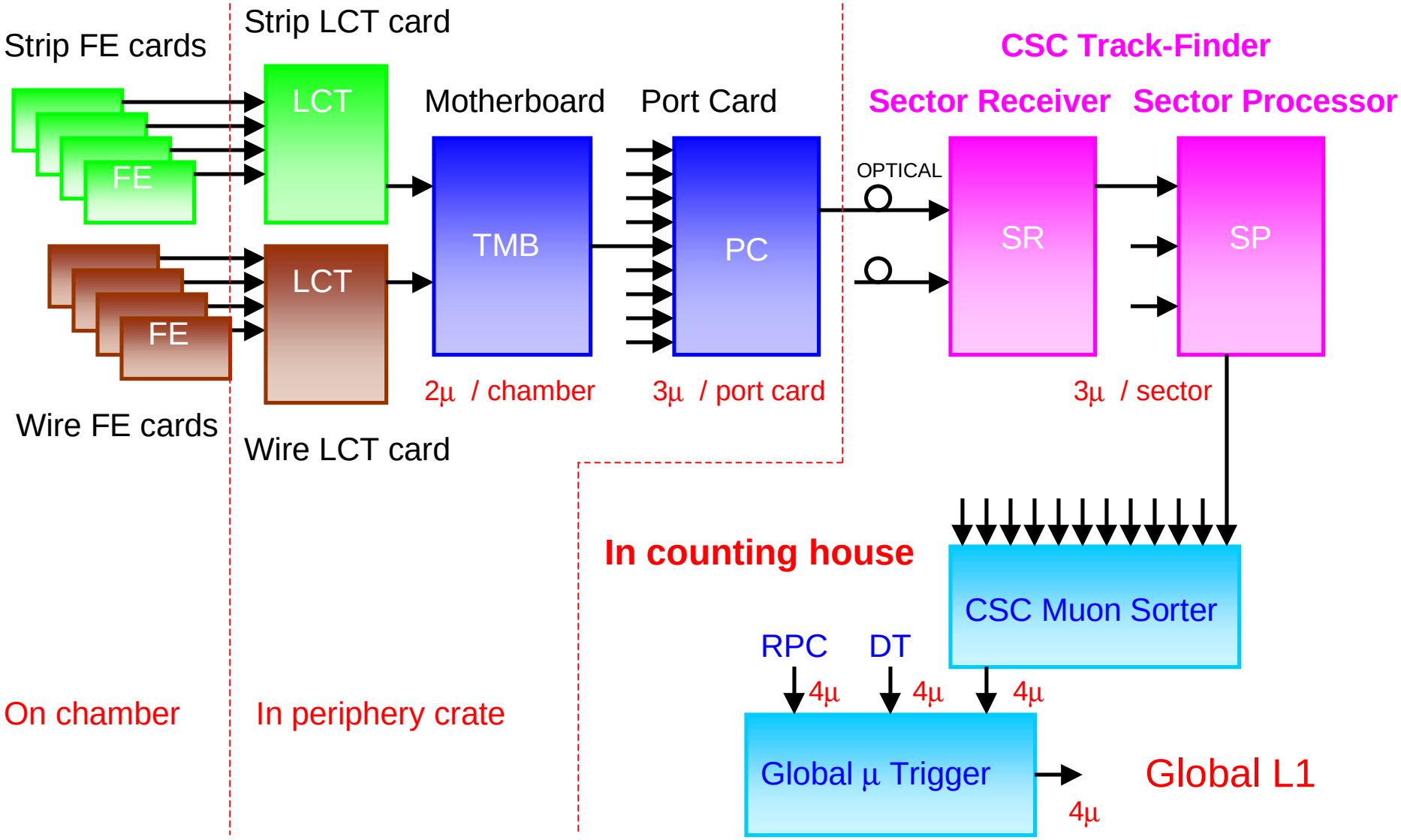
- Evolution since May 98 Lehman Review

Issues Concerning CSC/DT Interface

Progress

Plans

CSC Muon Trigger Scheme

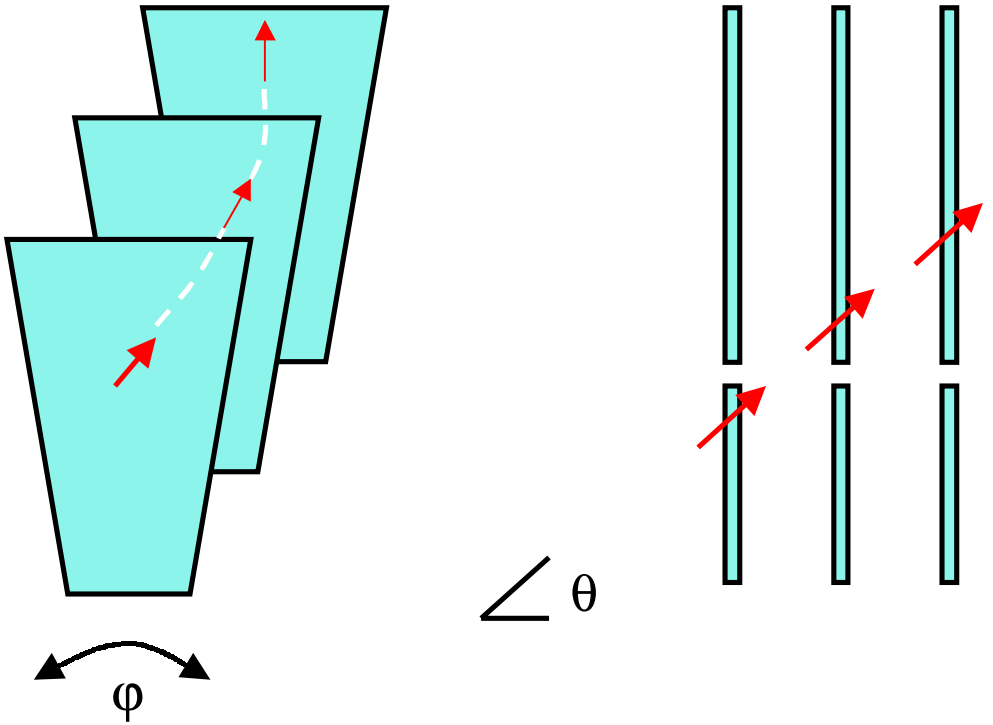


Muon Track-Finding

Link trigger primitives into tracks

Assign P_T, φ, and η

Send highest P_T candidates to Global L1



CSC Track-Finder Requirements

High efficiency

Trigger Rate:

- Single muon rate < few kHz at $L = 10^{34}\text{cm}^{-2}\ \text{s}^{-1}$

Resolution:

- $\sigma_{Pt} / P_t \leq 30\%$ (*Requires η information*)

Selection:

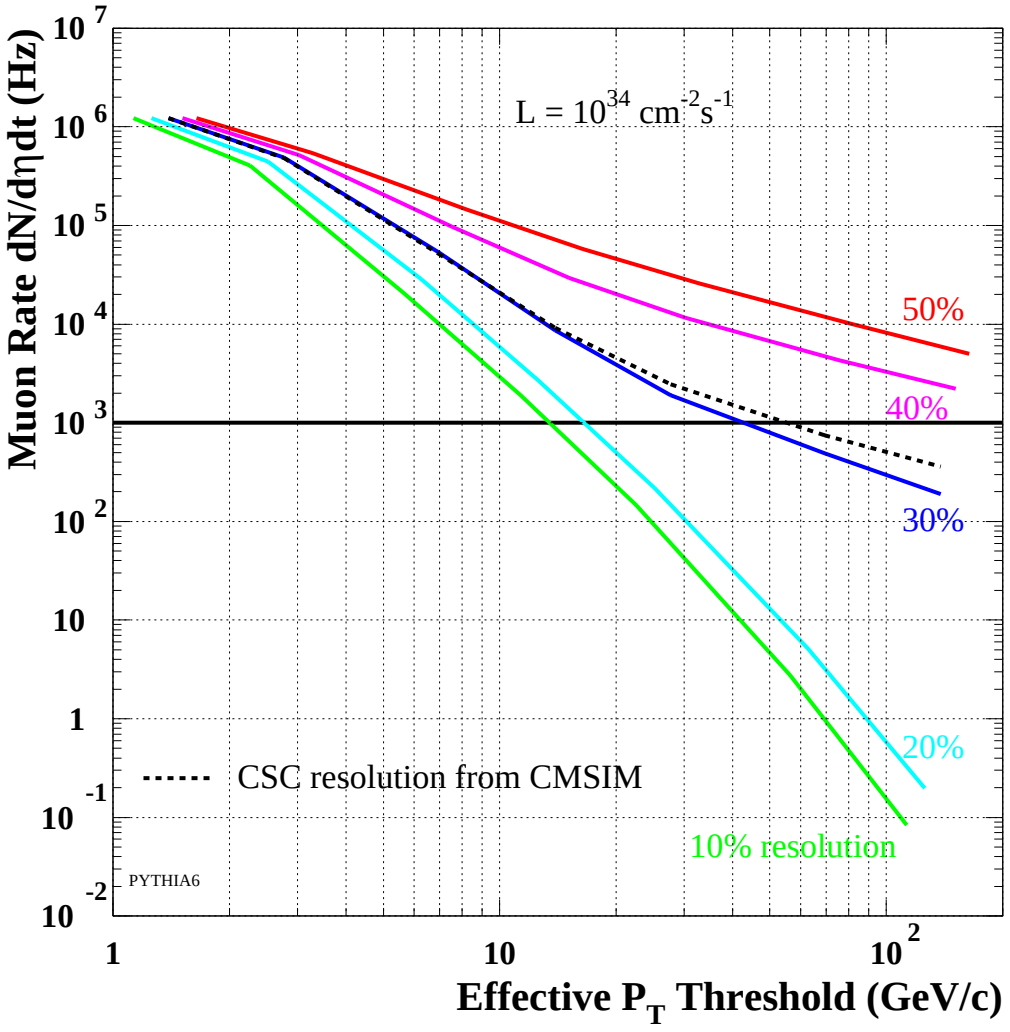
- $\leq$ 3 muons per 60° sector

Redundancy

- Require only 2 stations out of 3 (or 4)

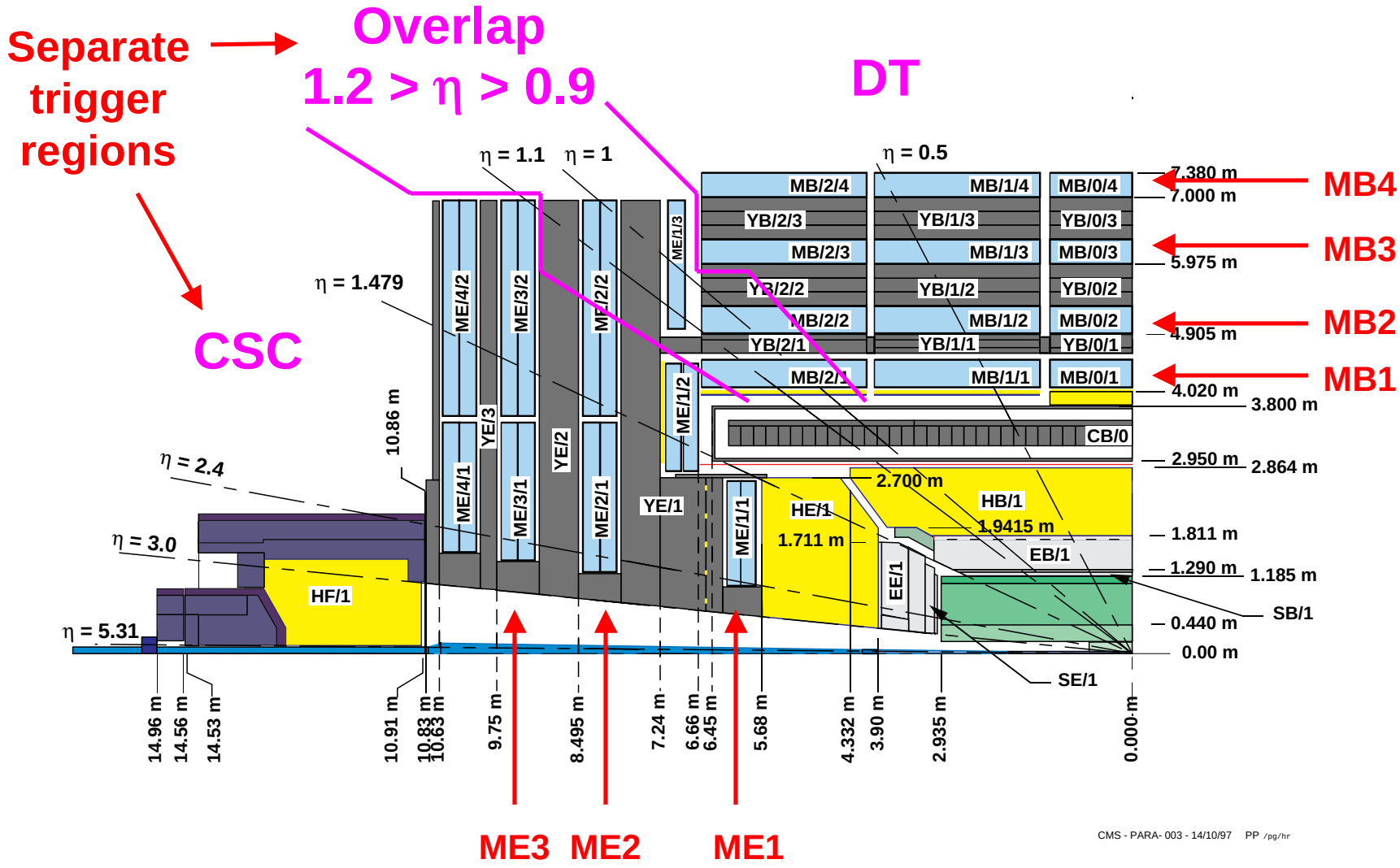
Minimal latency, pipelined, programmable

CSC Muon Trigger Rates



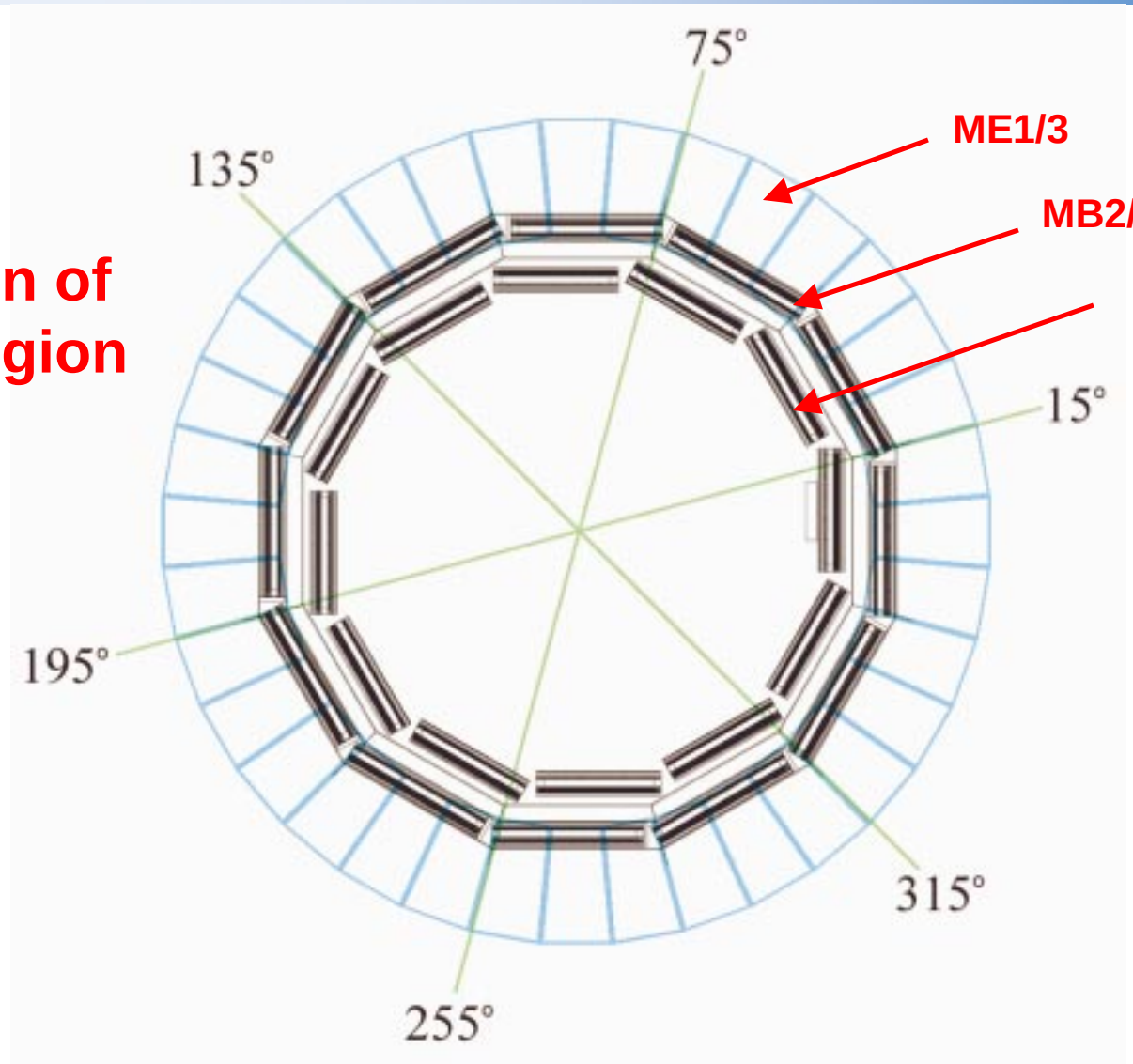
- Single μ rate from Pythia, convoluted with efficiency curve
- Thresholds set for 90% efficiency
- Require rates < 1 kHz per unit rapidity
- Not satisfied for P_T resolution worse than 30%

Trigger Regions in η



Trigger Regions in φ

Illustration of overlap region

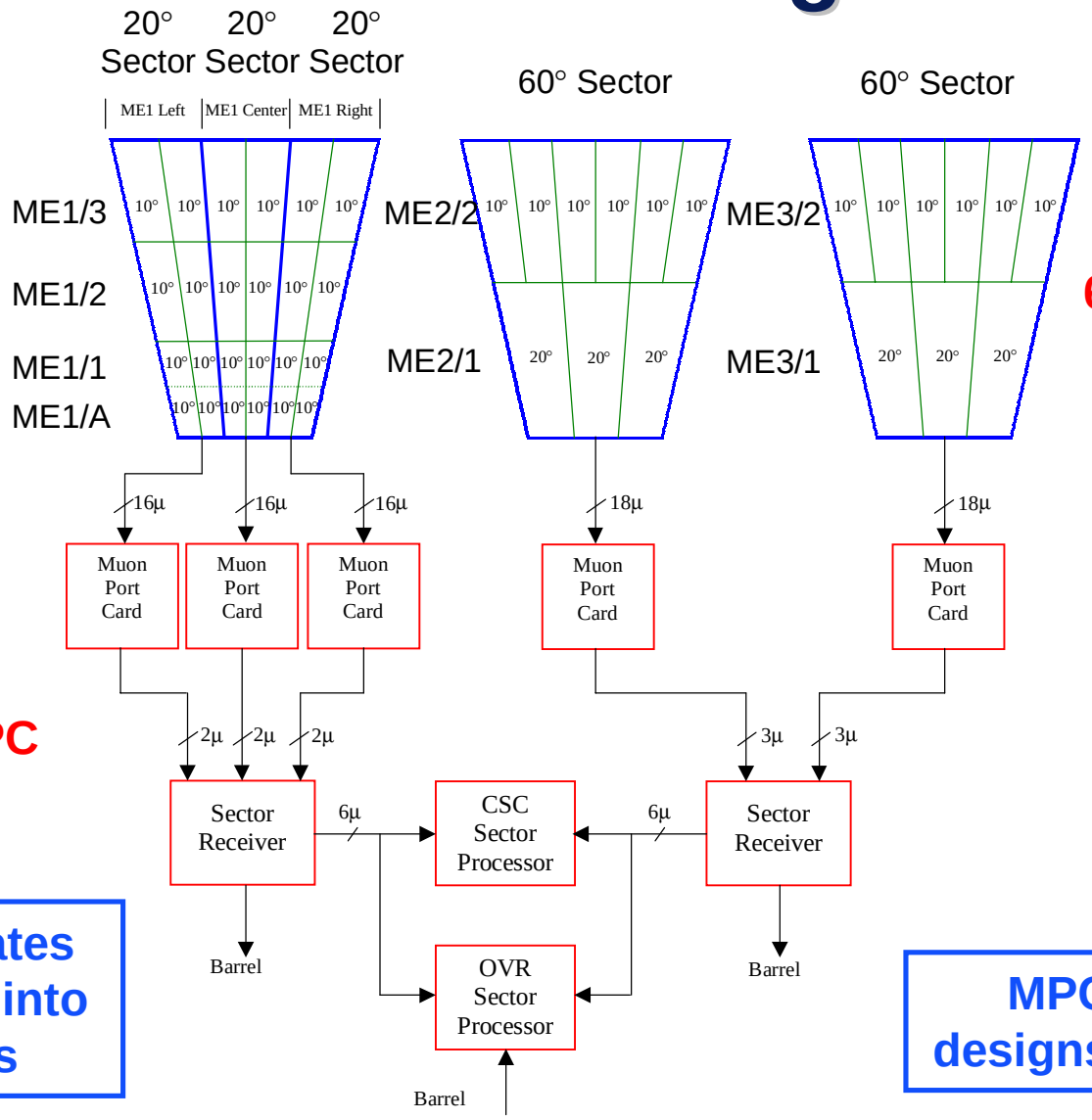


Overlap Region Issues

- **CSC *and* DT segments are required for efficient coverage of $0.9 < |\eta| < 1.2$**
- **Agreement with Vienna and Bologna on Barrel/Endcap boundary**
  - Barrel and Endcap Track-Finders are fundamentally different (2D vs. 3D)
  - Information sent both ways
    - **MB2/1+MB2/2 $\Rightarrow$ CSC T-F ME1/3+ME2/2 $\Rightarrow$ DT T-F**
  - Programmable sharp η boundary
    - **Avoids duplication of single muon in overlap region**
  - Separate sorting of CSC and DT muons

Sector Partitioning for ME1 has Changed

30° → 20° sectors



2 → 3 MPC

3 → 2 µ / MPC

ME2 and ME3 60° sectors are unchanged

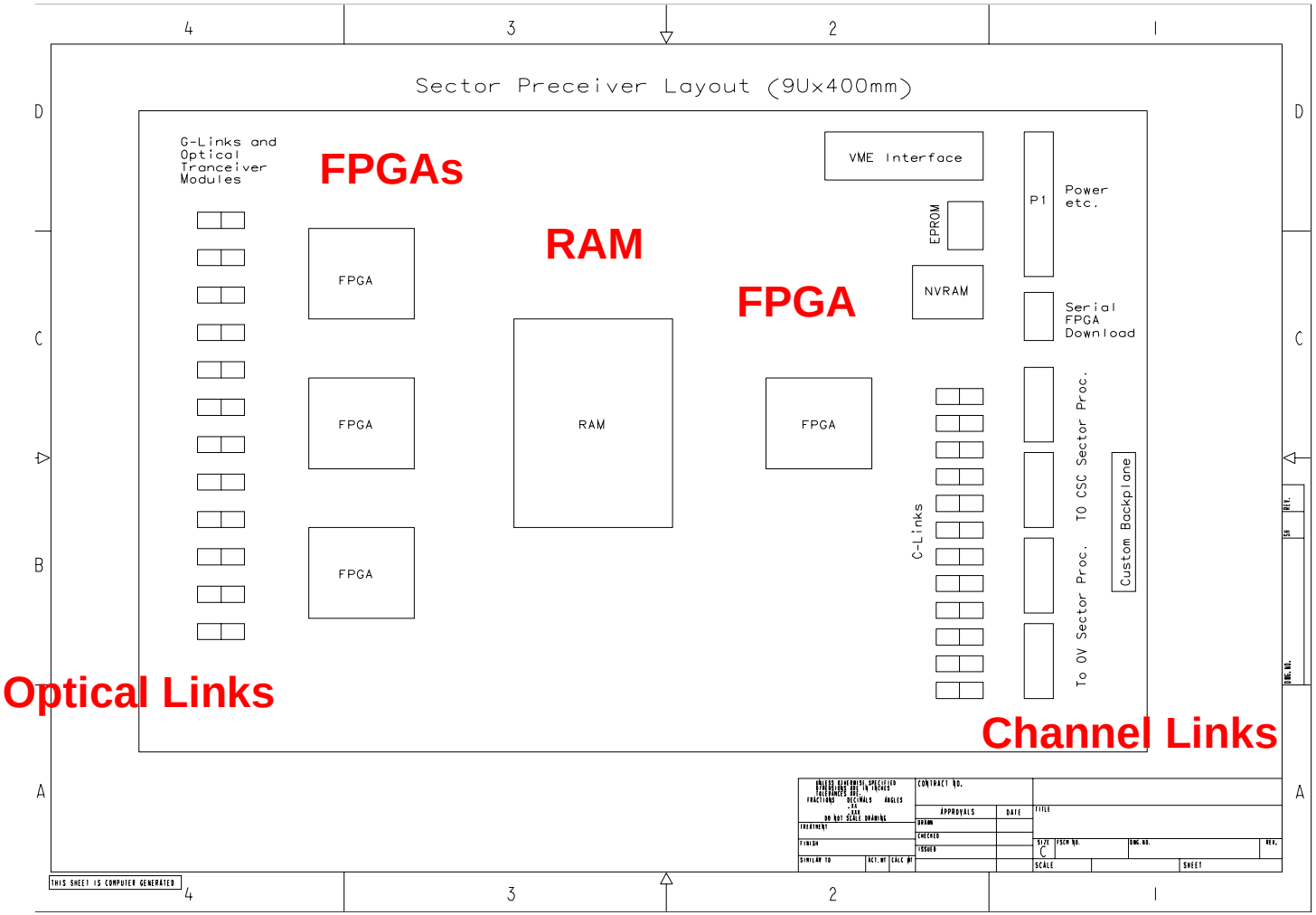
Accommodates split of ME1/1 into two regions

MPC and SR designs preserved

Sector Receiver Functionality

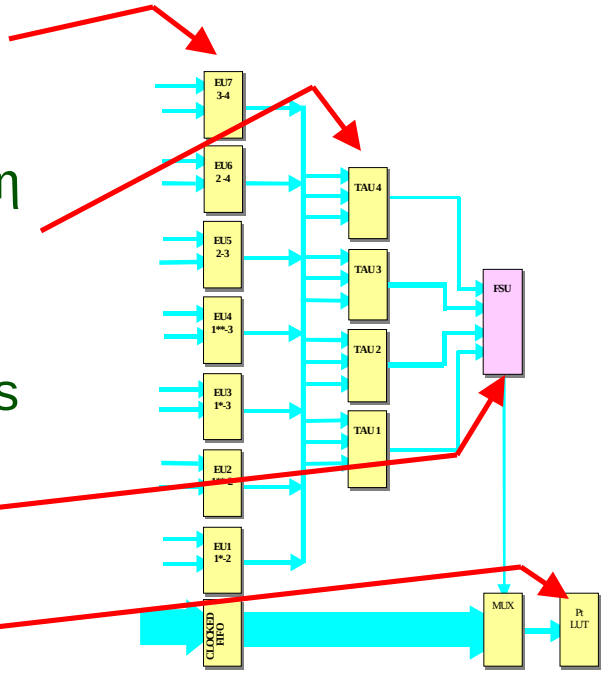
- **Receives 6 μ segments via 12 optical links from 2 Muon Port Cards (3 in ME1)**
- **Synchronizes the data**
- **Reformats the data**
  - LCT bit pattern $\rightarrow \eta, \varphi, \Psi, \ldots$ } **via LUT**
- **Applies alignment corrections**
- **Design changes since last review:**
  - Communicates to Sector Processors via custom backplane (Channel Link)
  - Fans out signals to DT Track-Finder
  - No longer repeats signals to Sector Receivers in overlap crates

Sector Receiver Block Diagram

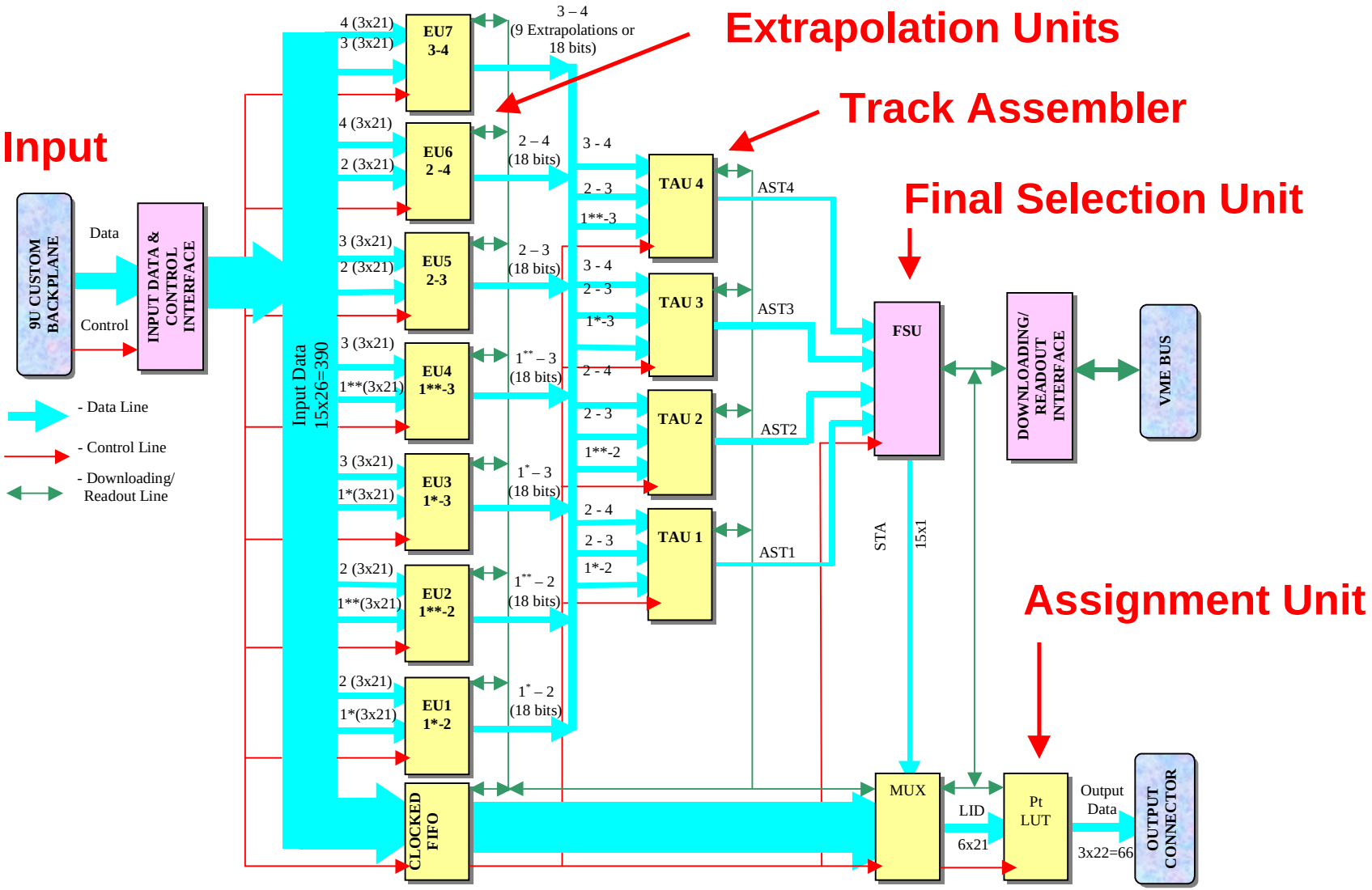


Sector Processor Functionality

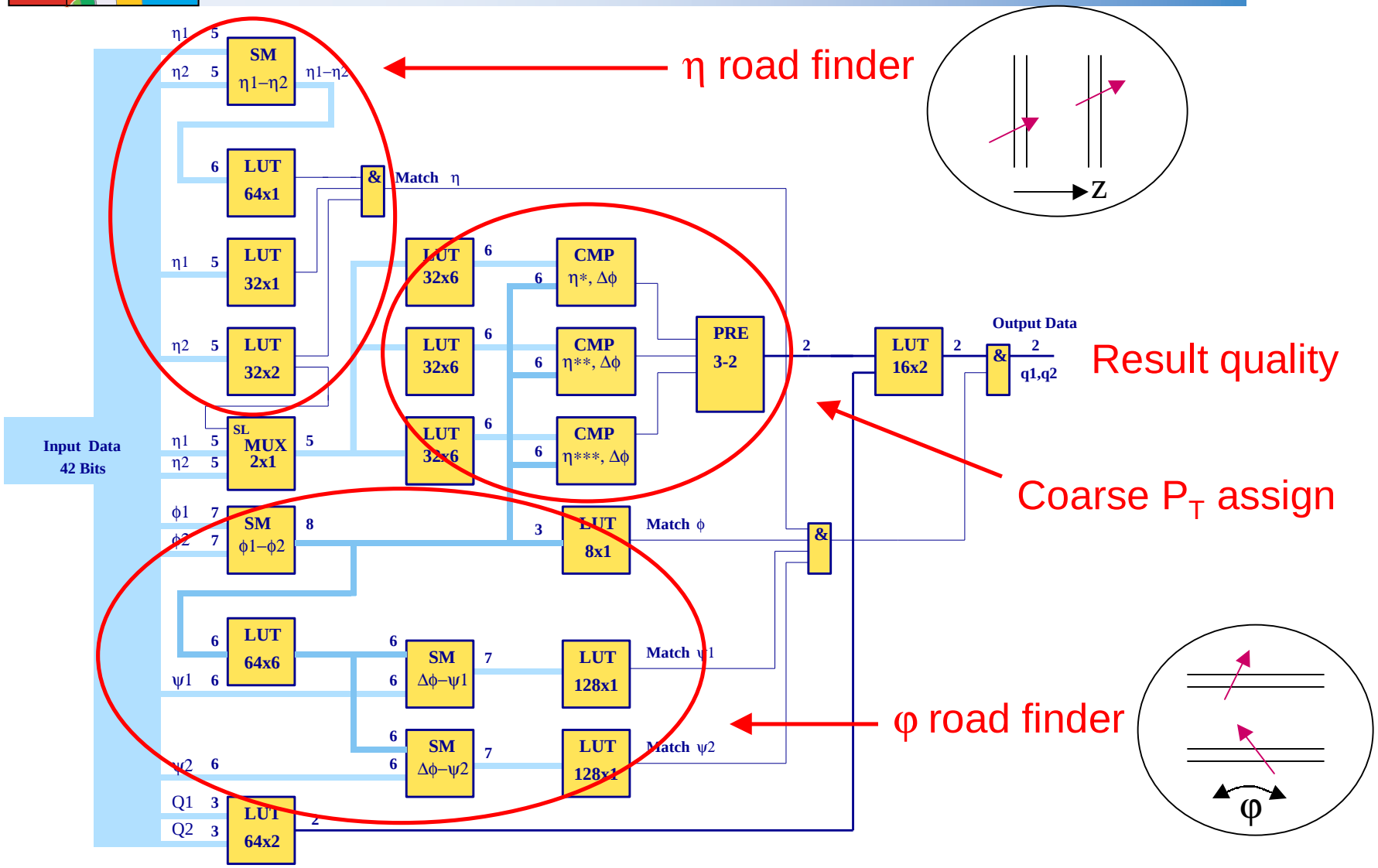
- **Initial system design is *new* since 5/98 review**
  - Functional block diagram developed
  - FPGA and board partitioning started
- **Identify and measure muons from ~ 600 bits every 25ns (3 GB/s)**
  - Perform all possible station-to-station extrapolations in parallel
  - Simultaneously search roads in φ and η
  - Assemble 2-, 3- and 4-station tracks from 2-station extrapolations
  - Cancel redundant short tracks if track is 3 or 4 stations in length
  - Select the three best candidates
  - Calculate P_T, φ, η and send to CSC muon sorter: 22 bits × 3 = 66 bits



Sector Processor Block Diagram



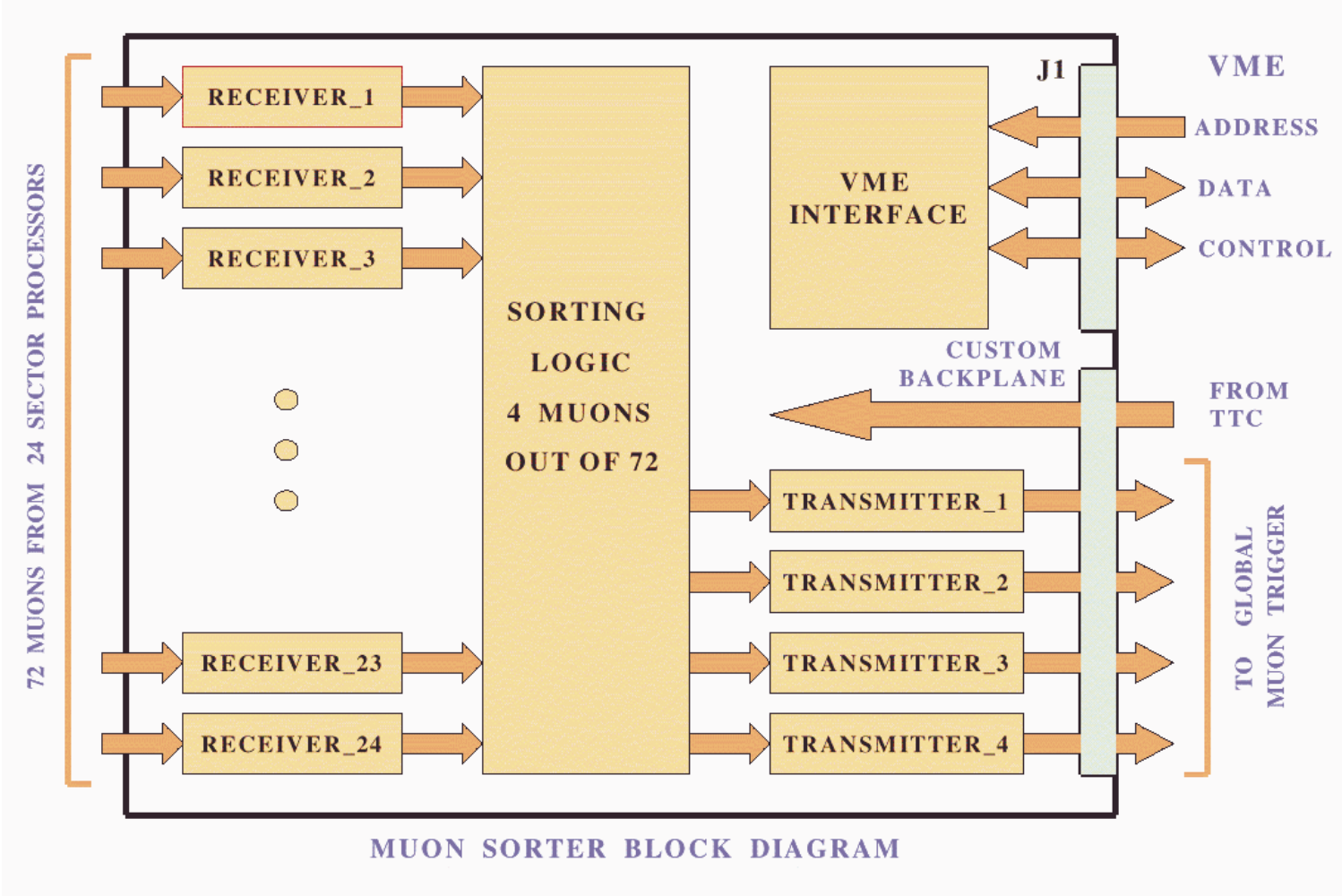
Extrapolation Unit Detail



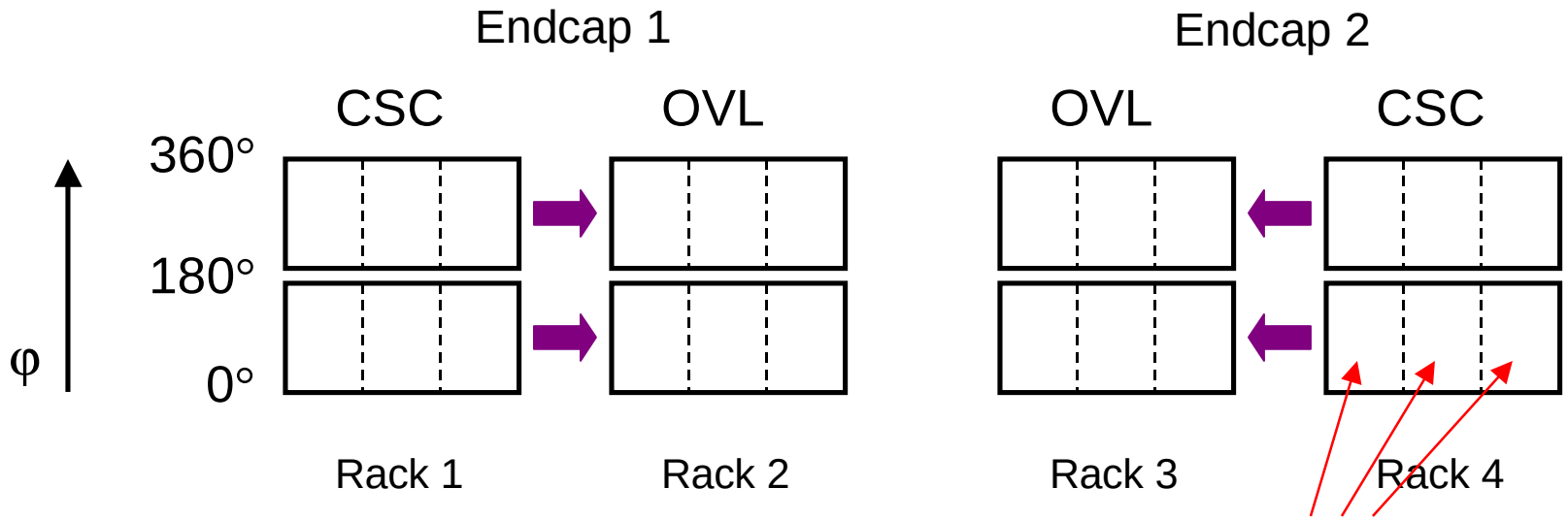
Muon Sorter Functionality

- **New processor added since last review**
- **The 3 highest rank muons from each Sector Processor are sent to the *CSC muon sorter*, which selects the 4 highest rank**
- **Total muon count:**
  - 3 muons $\times$ 6 sectors $\times$ 2 endcaps $\times$ 2 regions = 72 muons for CSC and OVL regions
- **Sort is based on 7 bits (5 bits for P_T and 2 bits for quality)**
  - Basic sorting unit design (4 best out of 8) is complete
- **Input: 72×22 bits = 1584 bits**
- **Output: 4×22 bits = 88 bits**
  - Sent to Global L1 Muon Trigger for association with RPC and DT triggers

Muon Sorter Block Diagram



Old CSC Track-Finder Crate Organization



CSC Counting House electronics:

Three 60° sectors per crate

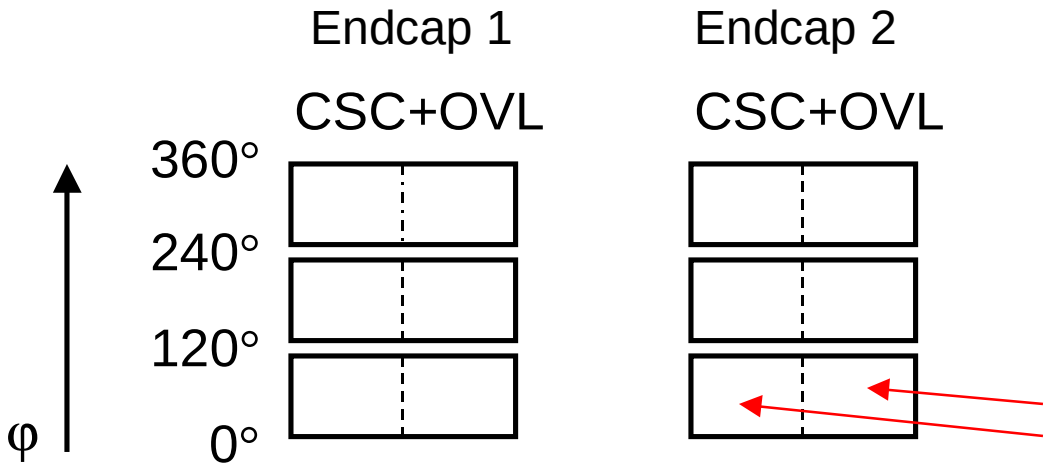
Racks: 4

Crates: 8 (including power supply, controller, CCC)

Sector Receivers: 48

Sector Processors: 24

New CSC Track-Finder Crate Organization



CSC and overlap regions now handled in same crate

Two 60° sectors per crate

CSC Counting House electronics:

Racks: 3 or 4

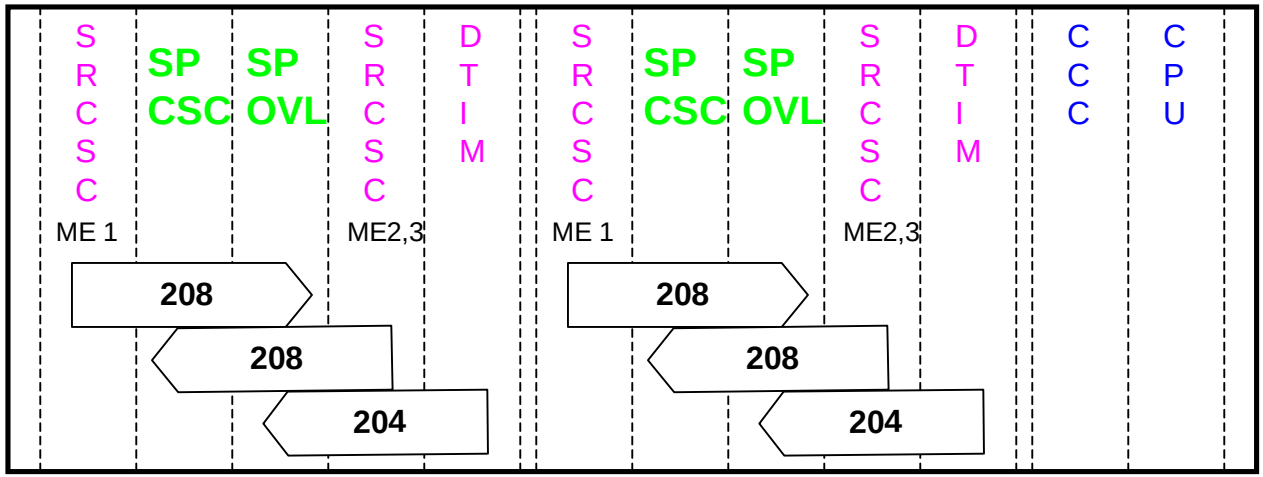
Crates: 6 (was 8)

Sector Receivers: 24 (was 48)

Sector Processors: 24

Muon Sorter: 1 (new)

New Layout for CSC Track-Finder Crate



- **Two 60° sectors housed in one 9U VME crate with custom backplane**
- **Each SR-CSC sends 6 CSC muon stubs × 34 bits and 4 bits BXN = 208 bits**
- **Each DT-IM sends 8 DT muon stubs × 25 bits and 4 bits BXN = 204 bits**

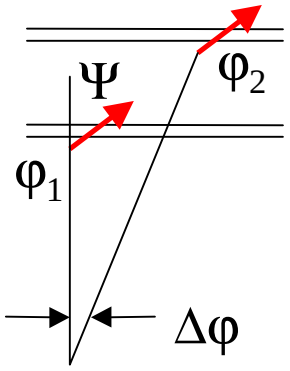
Required Precision of Data

Azimuthal angle φ:

- 12 bits / 60° ⇒ 1 bit / 0.26 mrad (0.1 strip)

Bend angle Ψ:

- 6 bits / ±45° ⇒ 1 bit / 60 mrad



Polar angle η:

- 6 bits / 1.5 units ⇒ 1 bit / 0.025

Quality:

- 3 bits

Chamber i.d.:

- 6 bits

Accelerator μ flag: 1 bit

34 bits per CSC segment to Sector Processor

Track Segments per 60° Sector

Region	Station	Chamber	Segments per sector	No. of φ sectors	No. of segments	Extrap-olations
CSC	1	ME1	2	3	6	81
	2	ME2	3	1	3	
	3	ME3	3	1	3	
	*4**	*ME4**	*3**	*1**	*3**	
					12, 15*	
OVL	1	MB1	2	2	4	106
	2	MB2	2	2	4	
	3	ME1	2	3	6	
	4	ME2	3	1	3	
					17	

Segments sent by Muon Port Cards to Sector Receivers via optical links.

Processed by Sector Processor

Design Progress

- **Full conceptual design from trigger primitives to Global L1 Trigger**
  - Bit counts fully documented
  - Crate design underway
  - Sector Receiver functionality defined
  - Sector Processor algorithms defined
  - Sort algorithms defined
- **Simulation of Track-Finder performance underway**
  - resolution, efficiency, rate, chamber misalignment
- **Prototyping started**

Milestones / Schedule

√ **D387 – 1999 Mar, Sector Receiver Initial System Design**

√ **D331 – 1999 Mar, Sector Processor Initial System Design**

D390 – 1999 Sep, Sector Receiver Prototype Design

D332 – 1999 Sep, Sector Processor Prototype Design

started

D391 – 2000 Jan, Sector Receiver Prototype

D334 – 2000 Jan, Sector Processor Prototype

D335 – 2000 Apr, Sector Receiver / Processor Crate Test

tests to do:

MPC → SR optical link test

2 × SR + SP + CCC crate test

3 × MPC + 2 × SR + SP + CCC sector test