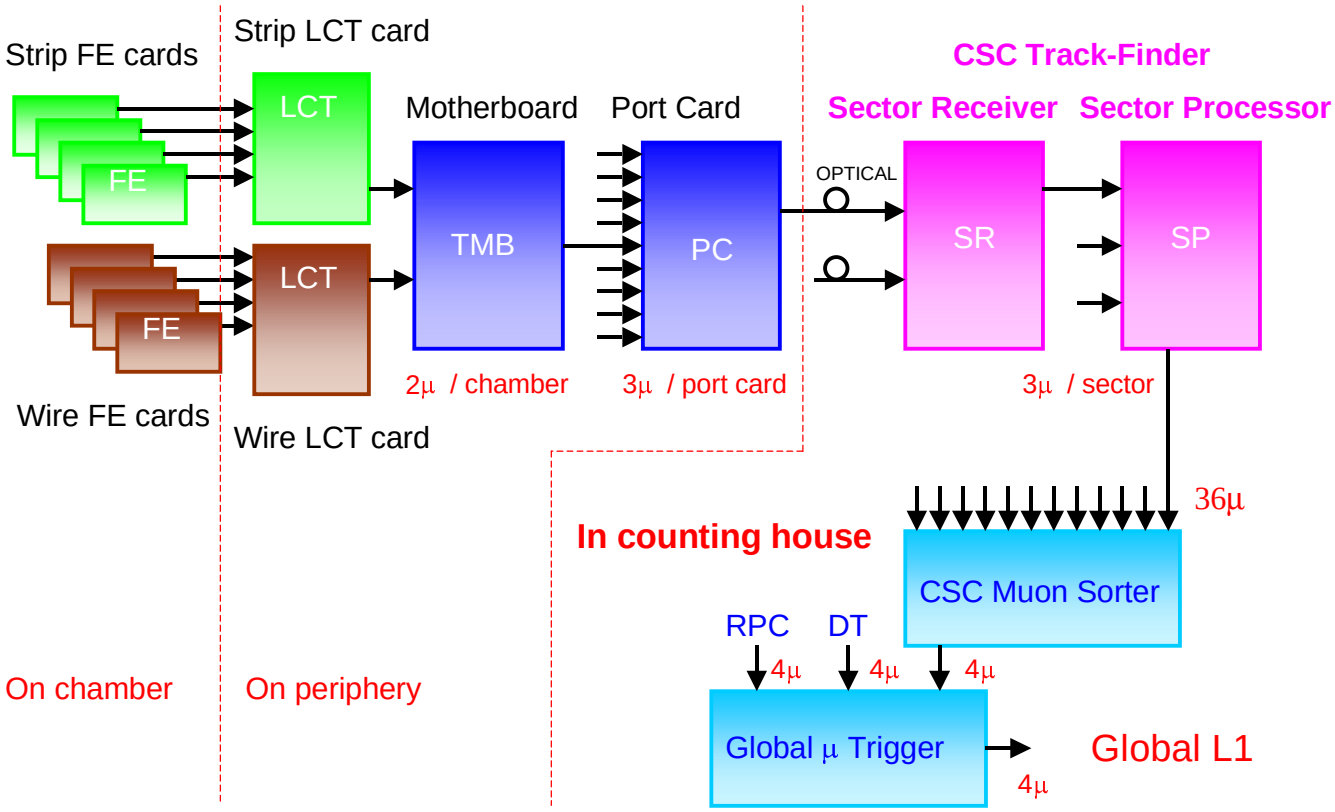
Status of the Level-1 CSC Track-Finder

D.Acosta, A.Madorsky, B.Scurlock, S.M.Wang
University of Florida

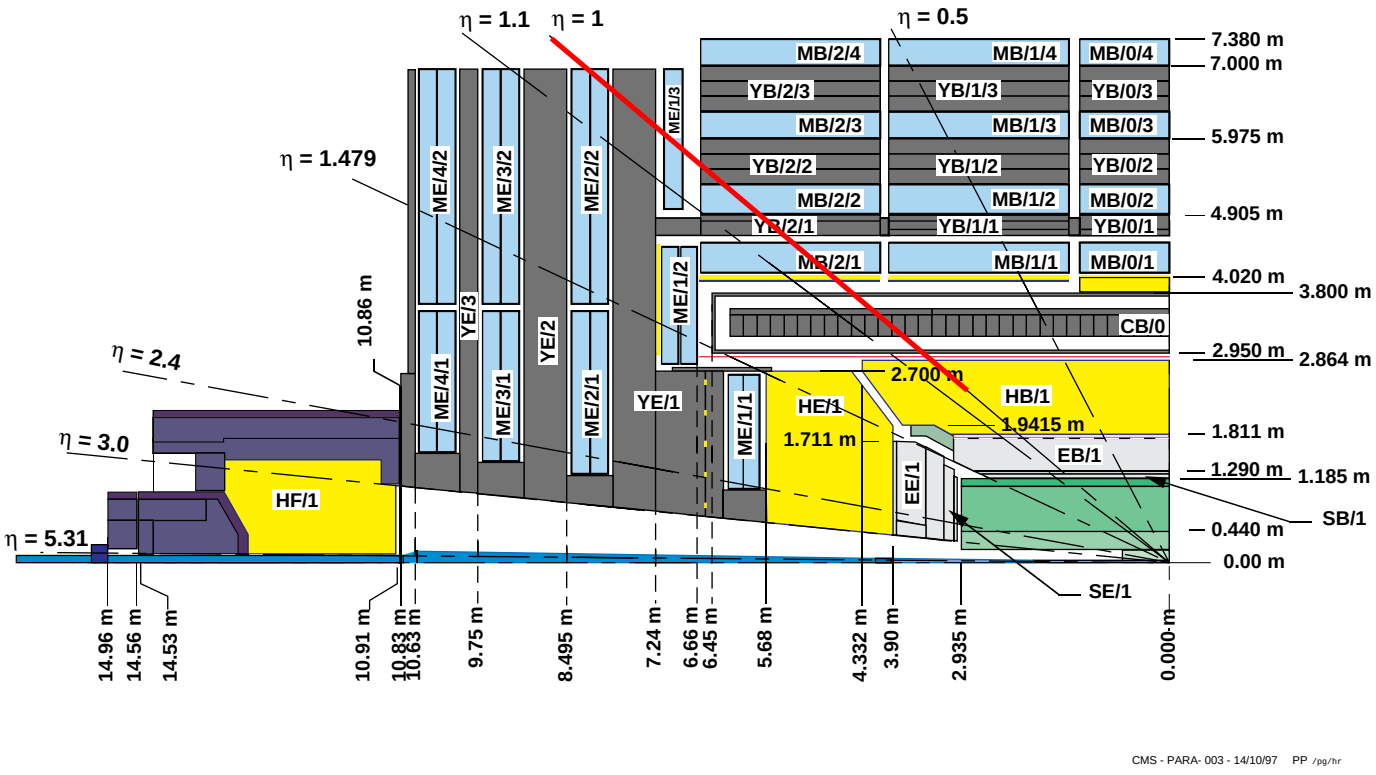
A.Atamanchuk, V.Golovtsov, B.Razmyslovich
St. Petersburg Nuclear Physics Institute

Level-1 Trigger Scheme



Rapidity Coverage of CSC Track Finder

- Require a track stub in ME2 or ME3 for endcap
- Require a stub in ME2 for overlap region
- Limits rapidity coverage to $\eta > 1$
- Allows CSC and DT processing on one board



Track-Finder Architecture

- Track-Finder implemented as 12 Sector Processors

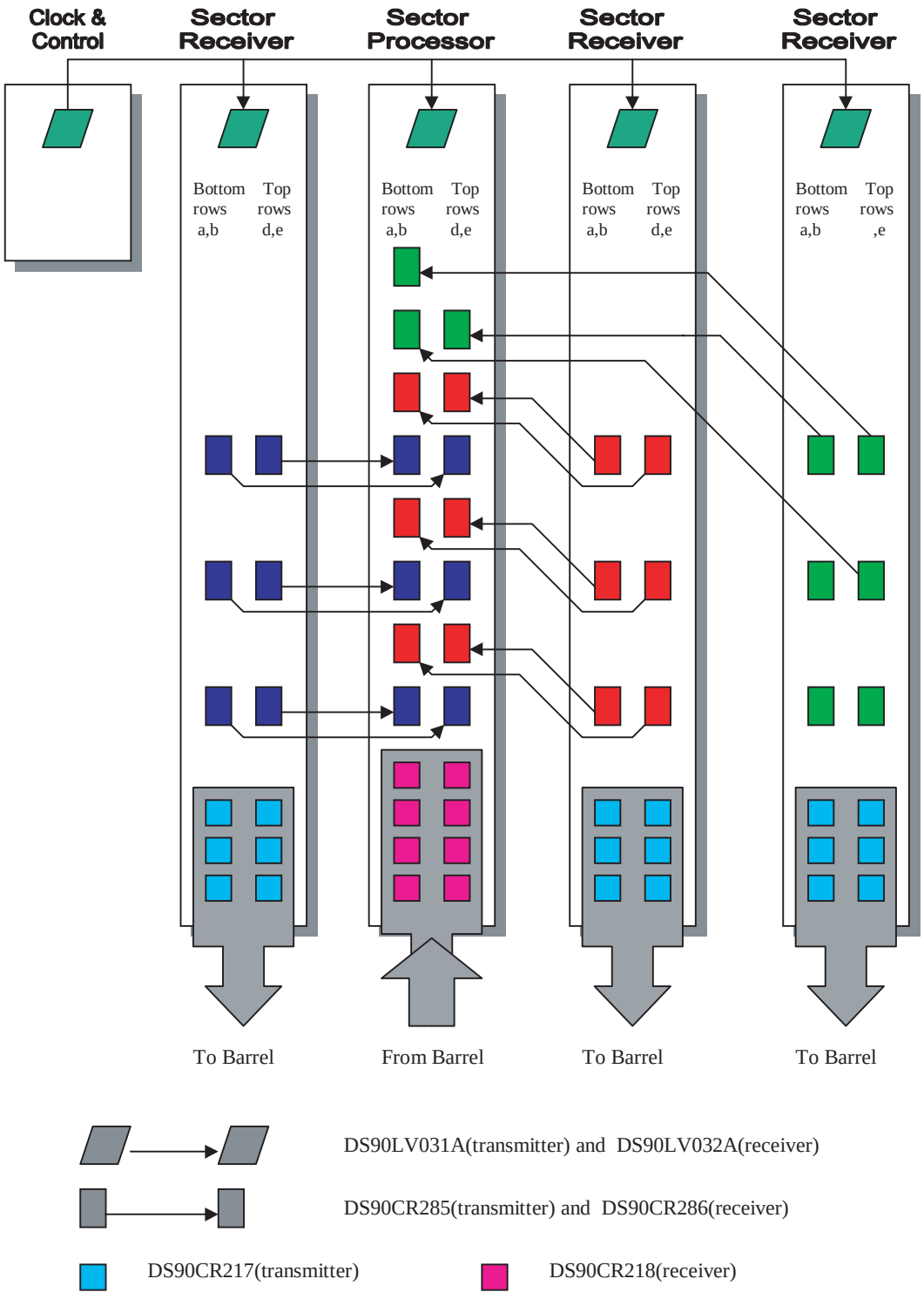
- Each Sector Processor:
  - Implemented on a 9U VME card
  - Processes 15 CSC segments and 8 DT segments
  - Identifies ≤ 3 muons per 60°

- CSC data received by 3 Sector Receiver cards
  - Each receives 6 track segments on optical links
  - Reformats data to φ, φ_b , η
  - Applies alignment corrections
  - Communicates to Sector Processors via custom point-to-point backplane
  - Presently under development at UCLA

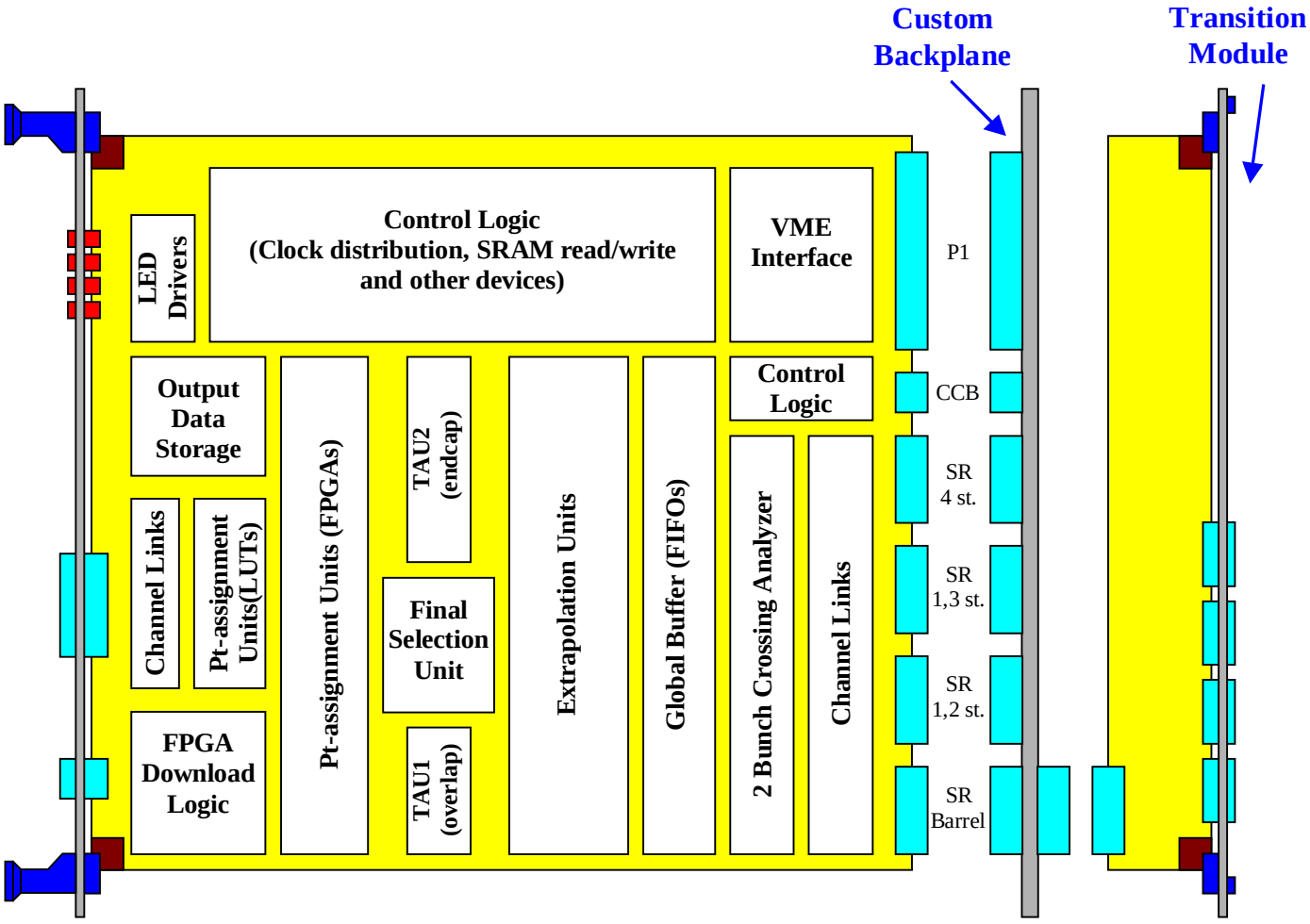
- DT data sent to transition board at back of crate

- Custom point-to-point backplane:
  - Delivers ~600 bits every 25 ns (3 GB/s)
  - Operates at 280 MHz to reduce connections:
    - National Channel Link 28:4 serialization
  - Presently being prototyped in Florida

Track-Finder Backplane



Sector Processor Layout



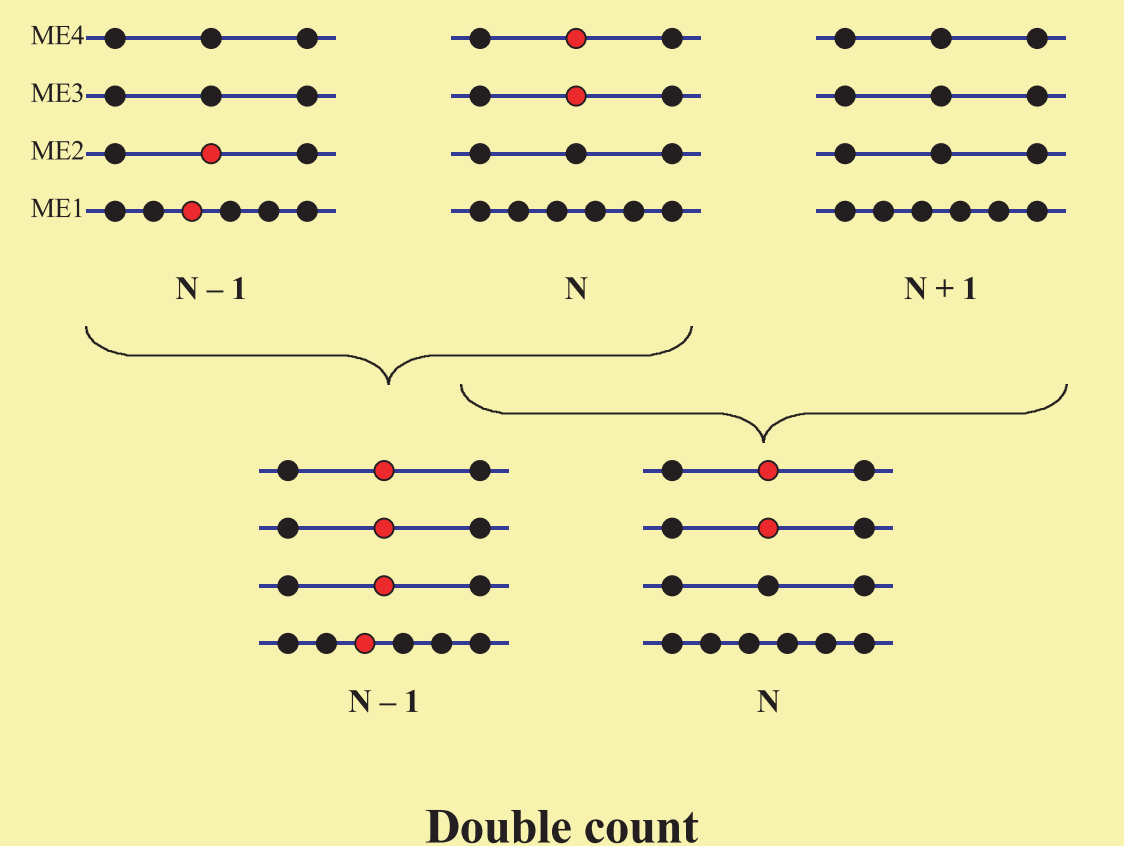
Latency expected to be 14 B.X.

Sector Processor Logic

- Latch input and hold for possibly more than one B.X.
  - Allows for timing errors from trigger primitives
- Perform all possible station-to-station extrapolations in parallel
  - Simultaneously search roads in φ and η
- Assemble 3- and 4-station tracks from 2-station extrapolations
- Cancel redundant short tracks if track is 3 or 4 stations in length
- Select the three best candidates
- Calculate P_T , φ, η and send to CSC muon sorter

Two Bunch Crossing Mode

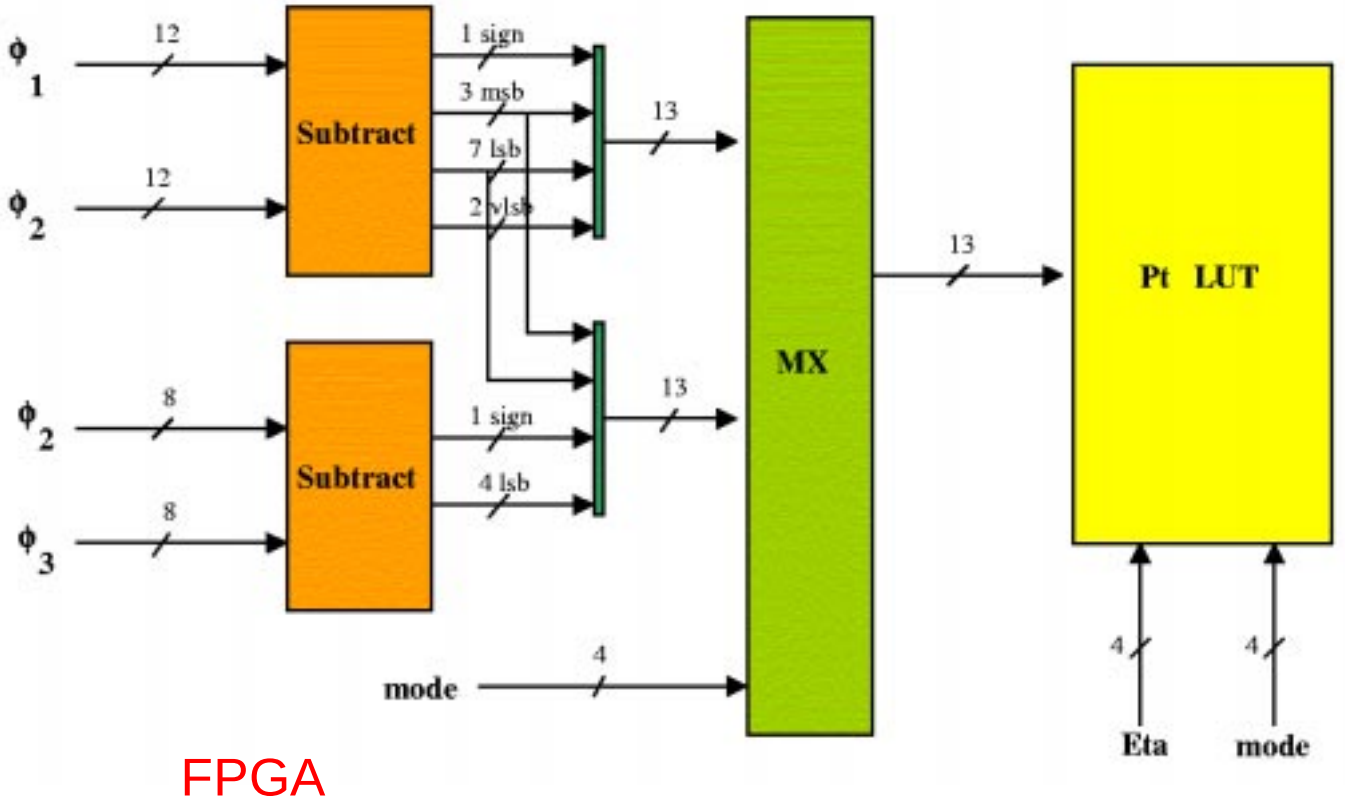
- Input data can be latched for 2 B.X. to accommodate timing errors from trigger primitives
- Sector Processor still reports trigger at correct B.X.
- Assume earliest stub defines correct B.X.
- Select stubs from later B.X. only if Track-Finder input is not full (*i.e.* keep input count the same)
- Cancel double triggers



Assignment Unit

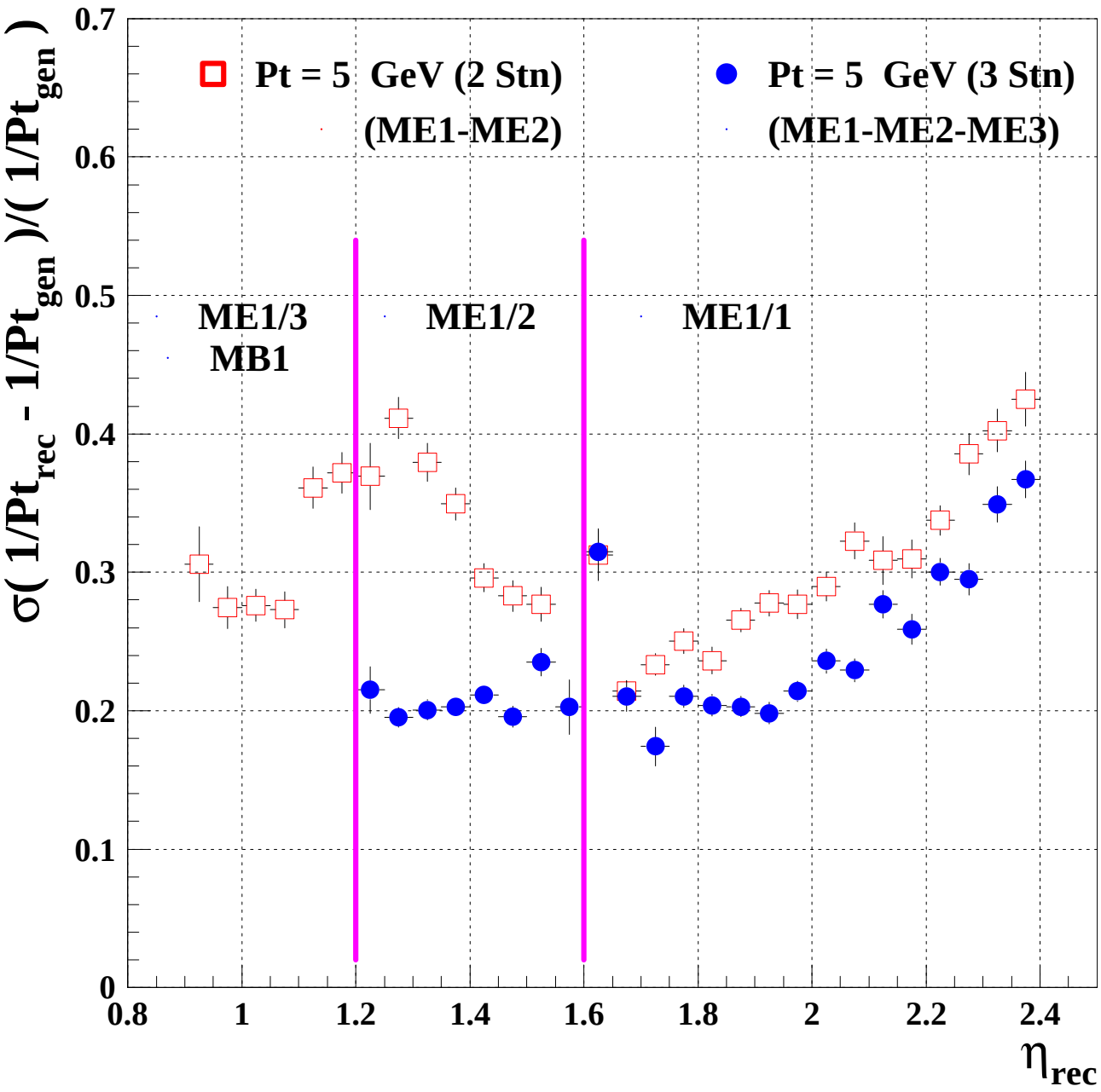
- Determines φ, η, P_T, and quality of the selected 3 best muons. (P_T and quality ⇒ Rank)
- P_T assignment uses φ, η measurements from 2 or 3 stations
  - $\delta P_T/P_T$ ~ 30% with only 2 stations
  - $\delta P_T/P_T$ ~ 20% with 3 stations ⇒ improves Level-1 rate reduction
- Implemented with FPGA preprocessing followed by large SRAM look-up table

2Mb×8 SRAM

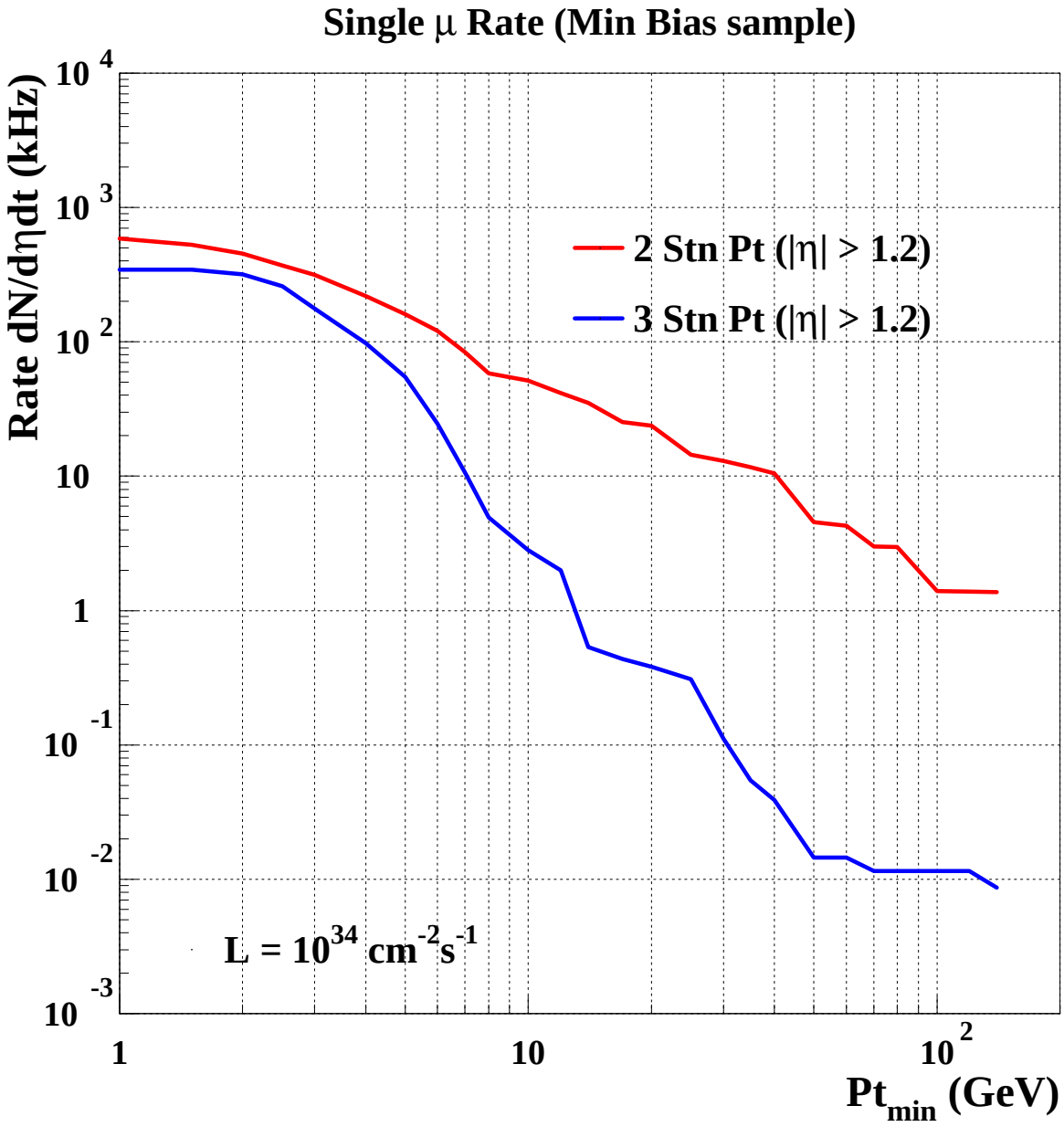


FPGA

P_T Resolution



Trigger Rate



3-station measurement provides a large safety factor in reducing the single μ rate below 1 kHz / unit rapidity

Track-Finder Output

- 5-bit P_T and 2-bit Quality are combined into a 7-bit Rank
- This rank is used by the CSC Muon Sorter
- Output of Muon Sorter can be the rank, or P_T and Quality via LUT
- Depends on how CSC and DT muons will be combined and ranked by the Global Muon Trigger

From Sector Processor to Muon Sorter:

Variable	Precision	Range	Bits / μ	Bits / 3μ
φ	2.5°	0–60°	5	15
η	0.075	0.9–2.4	5	15
Rank	P_T & Quality	2–140 GeV	5+2	21
Sign	–	–	1	3
BXN	–	–	–	4
Error	–	–	–	1
Total			18	59

Add 3 bits to φ and 1 bit to η for Muon Sorter to Global Muon Trigger

Sector Processor Design Status

- Conceptual design complete
  - Documented in CMS Note (and eventually TDR)
- Schematics about 80% complete
- FPGA design about 50% complete
- PCB layout started
- Backplane design started
  - Tests underway at Florida
- Test adapter design about 50% complete
  - Will provide simulated DT signals as well as CSC
- Test software started, but much work to do:
  - Downloading FPGA/RAM configuration
  - Downloading patterns
  - Verification

Prototype Schedule

- February 2000
  - Finish schematics
  - Finish FPGA design
  - Finalize Sector Receiver/Sector Processor interface
- March 2000
  - Finish board layout
  - Begin construction
- May 2000
  - Begin testing of Sector Processor only
- June 2000
  - Begin trigger crate tests with backplane, Sector Receiver, and Sector Processor
- October 2000
  - Finish all tests
- November 2000
  - Finish TDR!

Summary of CSC Track-Finder

- Conceptual design complete
- 12 Sector Processors cover CSC and CSC/DT overlap
  - $1.0 < \eta < 2.4$ and $\Delta\phi = 60°$ on one board
- Track-finding algorithms are three-dimensional
  - Improves background suppression
- P_T assignment includes ϕ,η measurements from 3 stations
  - $\delta P_T/P_T \sim 20\%$ (30% with only 2 stations)
  - Significantly improves rate reduction at Level-1
- Inputs can be latched for 2 B.X.
  - Tolerates timing errors from trigger primitives
- Latency expected to be only 14 B.X.
- Fully re-programmable
- Xilinx Virtex FPGAs and SRAM used
- Board layout and backplane design started