CSC Trigger Electronics in the Counting Room

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TriDAS Review

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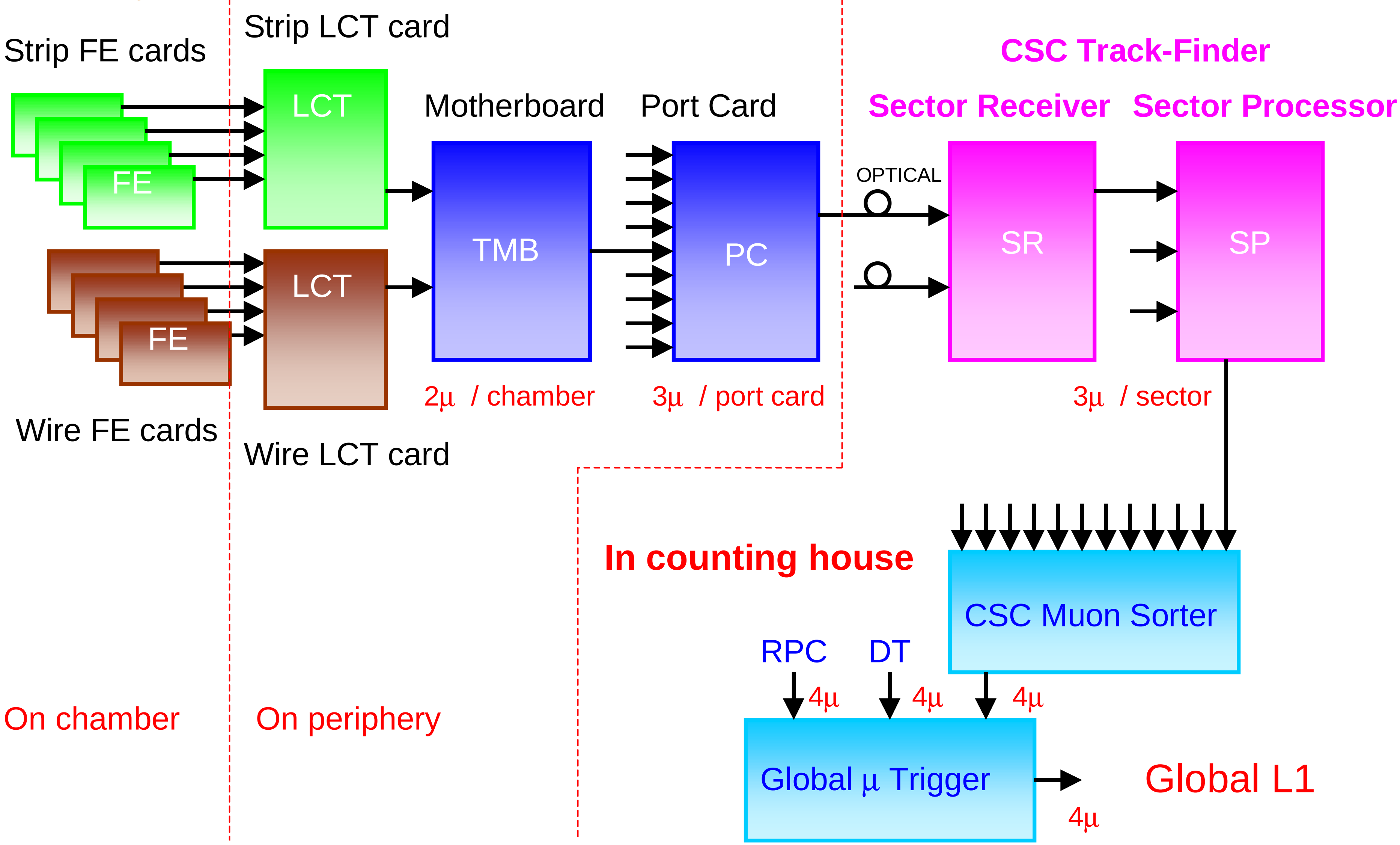
Outline

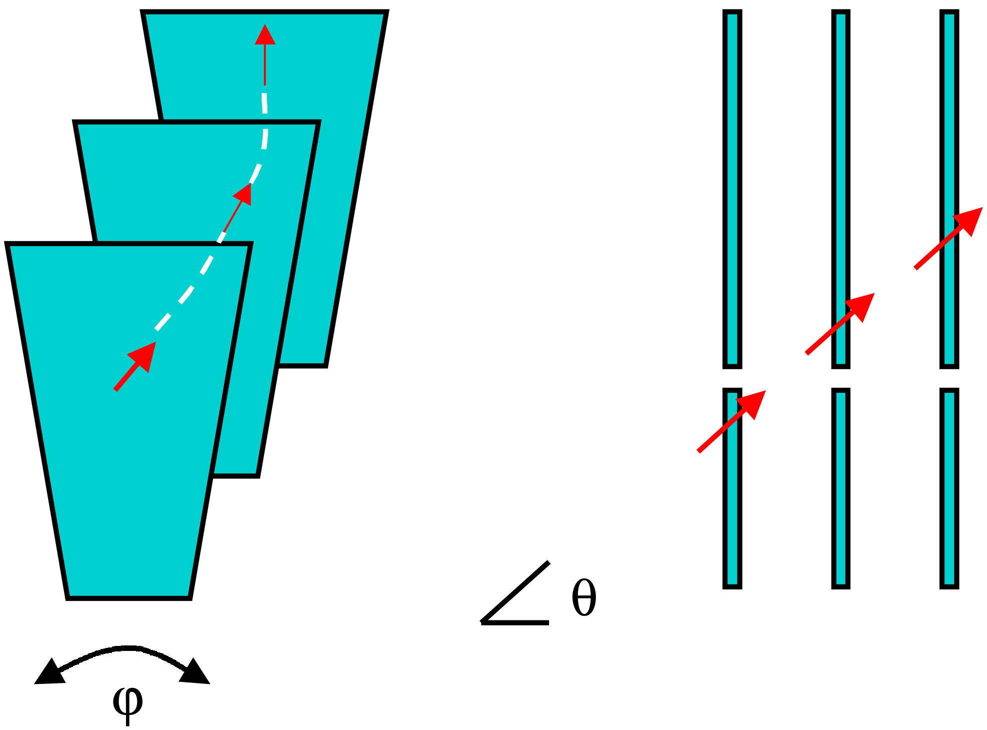
- Overview
- Sector Receiver functionality
- Sector Processor functionality
- Muon Sorter functionality
- Crate design
- Progress
- Plans

CSC Muon Trigger Scheme



Muon Track-Finding

- **Perform 3D track-finding from trigger primitives**
- **Measure P_T, φ, and η**
- **Transmit highest P_T candidates to Global L1**



CSC Track-Finder Requirements

High efficiency

Trigger Rate:

- Single muon rate < few kHz at $L = 10^{34} cm^{-2} s^{-1}$

Resolution:

- $\sigma_{Pt} / P_t \leq 30\%$ (Requires η information)

Multi-muon capability:

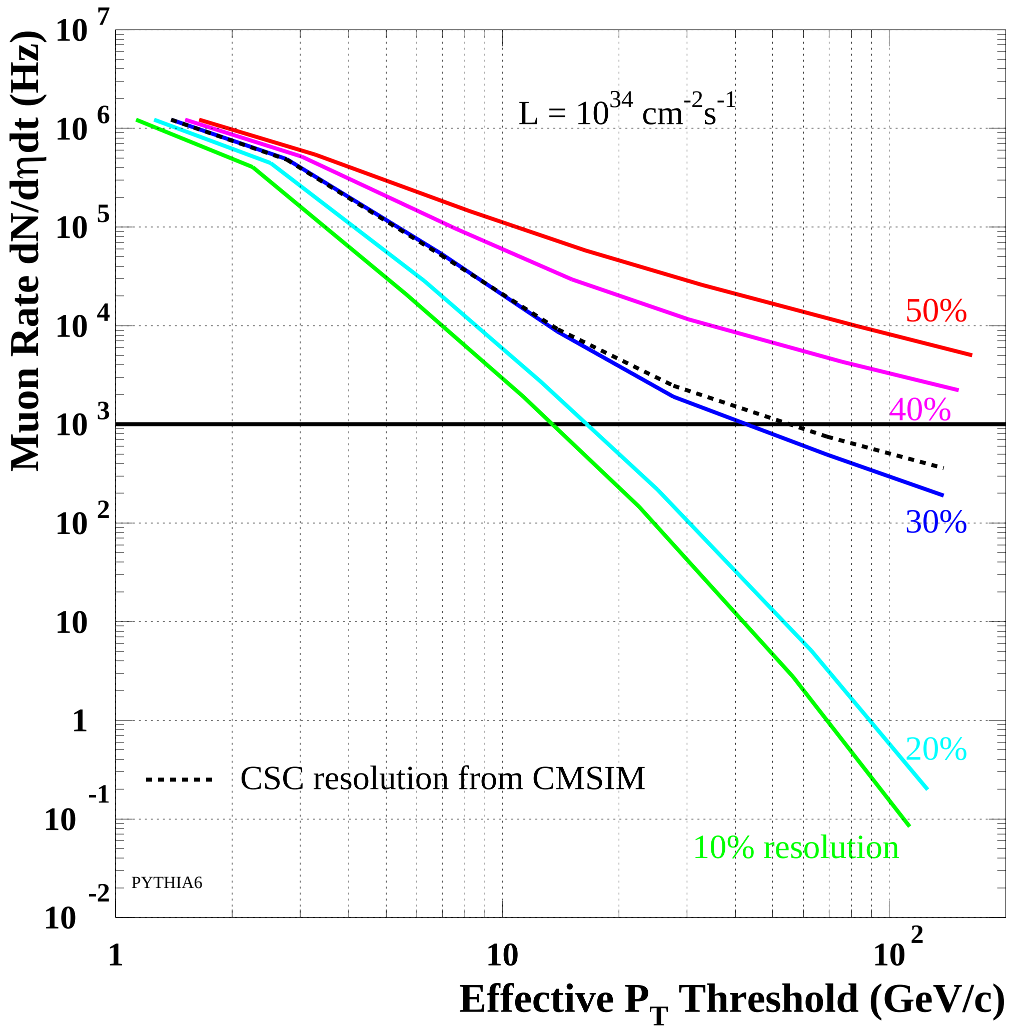
- $\leq$ 3 muons per 60° sector
- Best 4 muons sent to Global L1

Redundancy

- Require only 2 stations out of 3 (or 4)

Minimal latency, programmable

CSC Muon Trigger Rates



- Single μ rate from Pythia, convoluted with efficiency curve
- Thresholds set for 90% efficiency
- Require rates < 1 kHz per unit rapidity
- Not satisfied for P_T resolution worse than 30%

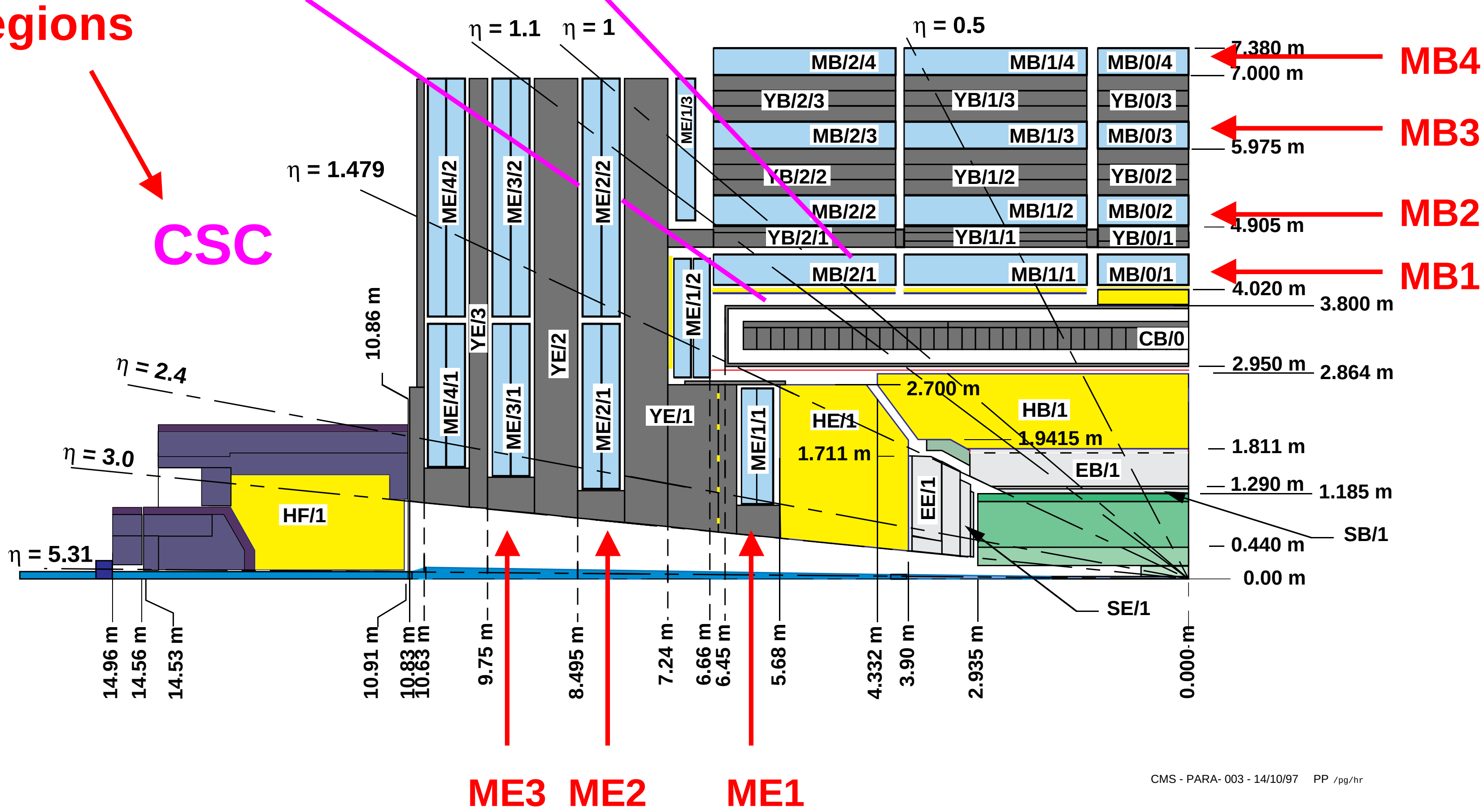
Trigger Regions in η

Separate trigger regions

Overlap 1.2 > η > 0.9

DT

CSC



Trigger Regions in φ

Track-Finding performed in independent 60° sectors

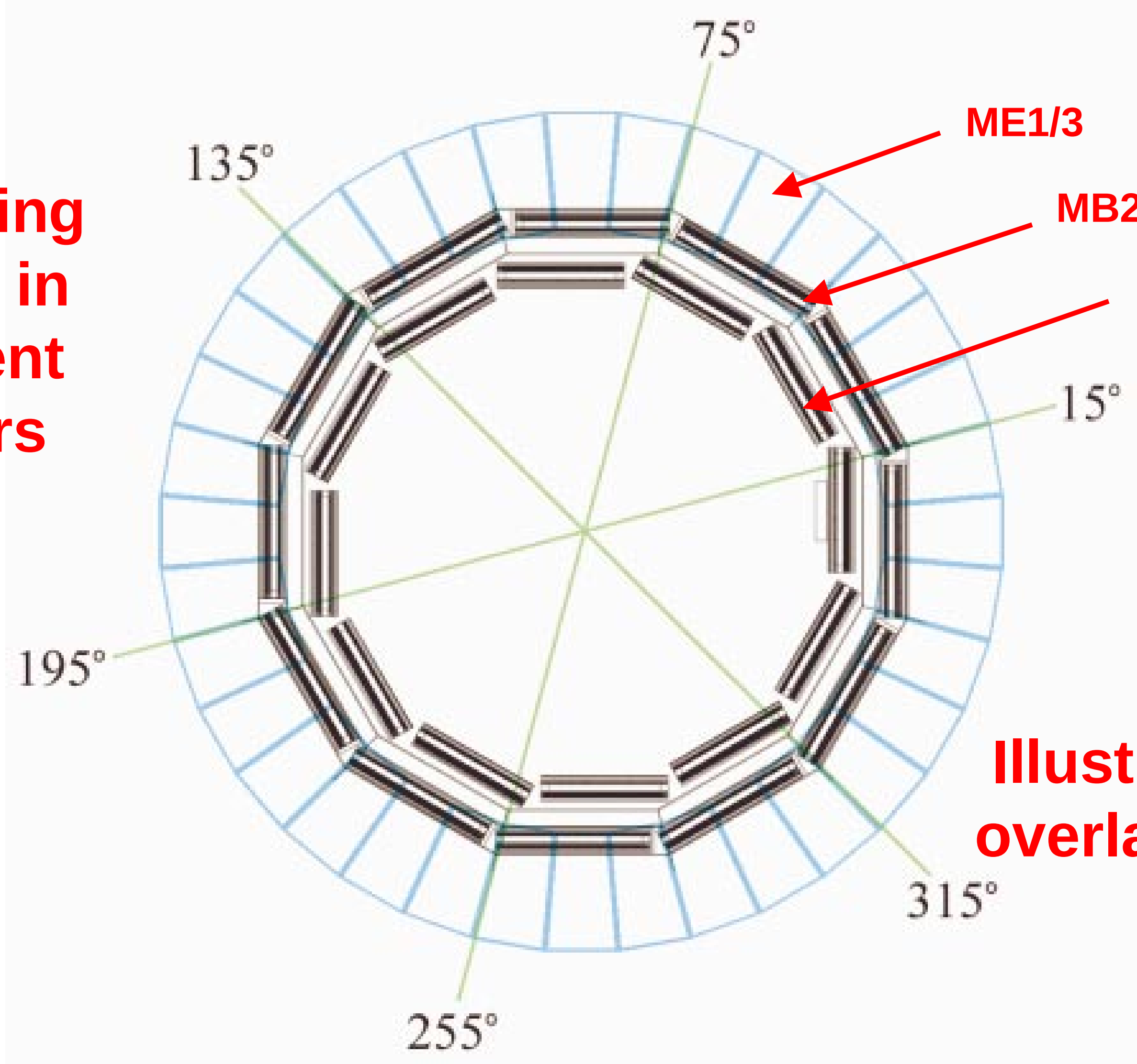


Illustration of overlap region

Overlap Region Issues

- **CSC *and* DT segments are required for efficient coverage of $0.9 < |\eta| < 1.2$**
- **Agreement with Vienna and Bologna on Barrel/Endcap boundary (CMS IN 1999/015)**

  ⇒ Barrel and Endcap Track-Finders are fundamentally different (2D vs. 3D)

  ⇒ Information sent both ways

  - **MB2/1+MB2/2 ⇒ CSC T-F   ME1/3+ME2/2 ⇒ DT T-F**

  ⇒ Programmable sharp η boundary

  - **Avoids duplication of single muon in overlap region**

  ⇒ Separate sorting of CSC and DT muons

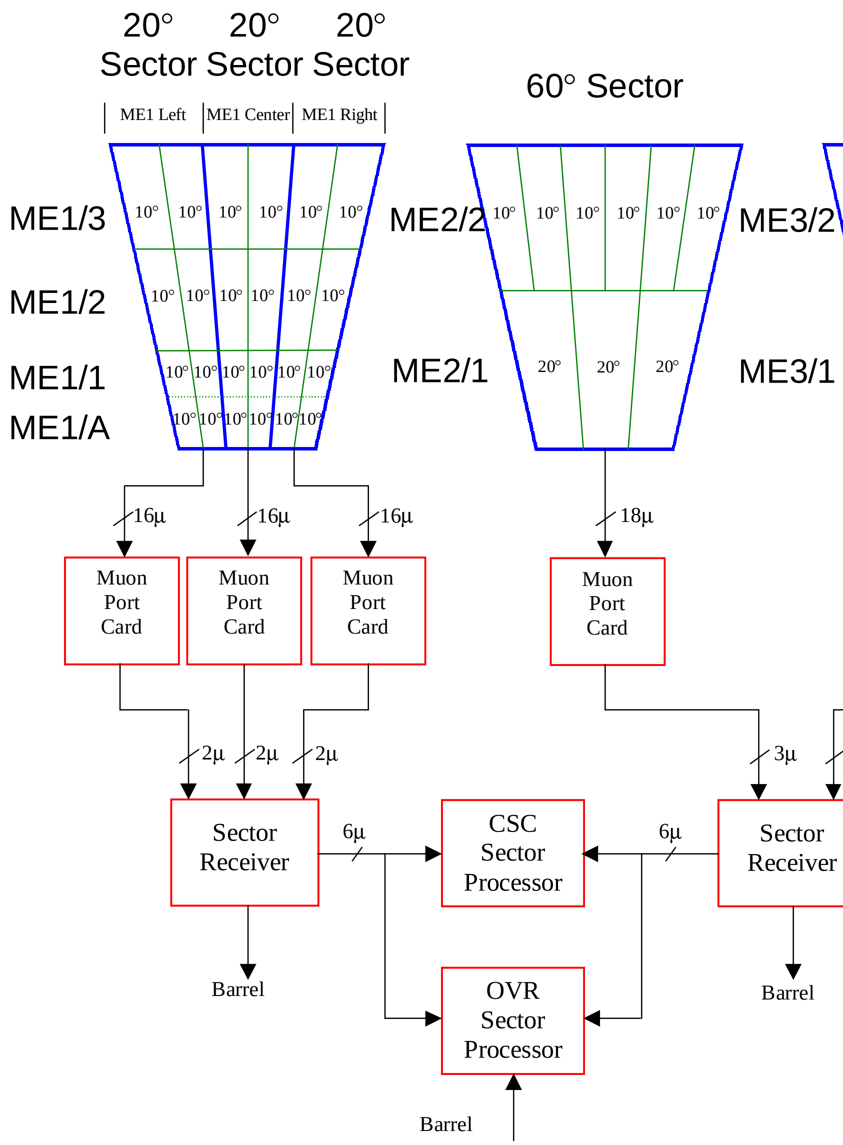
Sector Partitioning

30° or 20° subsectors in ME1

2 or 3 MPC

6 µ / SR

60° sectors in ME2 —ME4



Sector Receiver Functionality

UCLA

- Receives 6 μ segments via 12 optical links from 2 Muon Port Cards
- Synchronizes the data
- Reformats the data

  $\Rightarrow$LCT bit pattern $\rightarrow \eta, \varphi, \Psi, \ldots$ } via LUT
- Applies alignment corrections
- Communicates to Sector Processors via custom backplane (Channel Link)
- Fans out signals to DT Track-Finder

- Functional block diagram developed and board layout started $\Rightarrow$

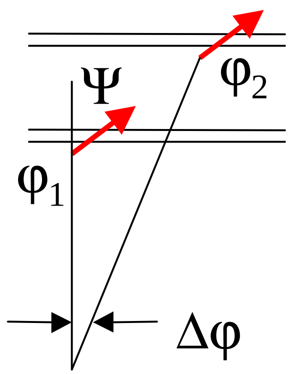
Required Precision of Data

Azimuthal angle φ:

- 12 bits / 60° $\Rightarrow$ 1 bit / 0.26 mrad (0.1 strip)

Bend angle Ψ:

- 6 bits / ±45° $\Rightarrow$ 1 bit / 60 mrad



Polar angle η:

- 6 bits / 1.5 units $\Rightarrow$ 1 bit / 0.025

Quality:

- 3 bits

Chamber i.d.:

- 6 bits

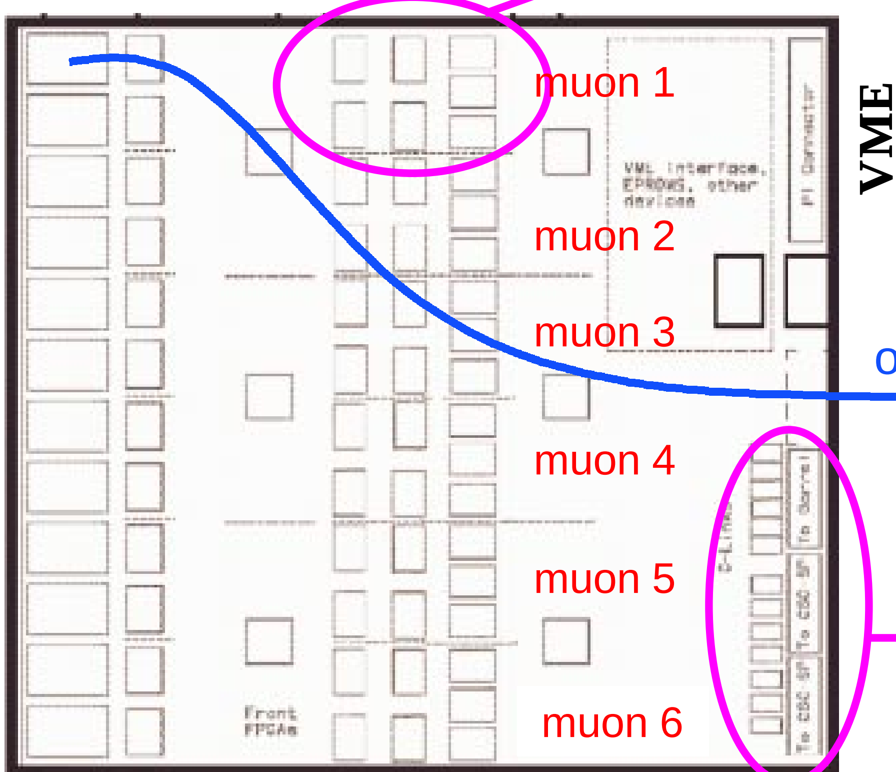
Accelerator μ flag: 1 bit

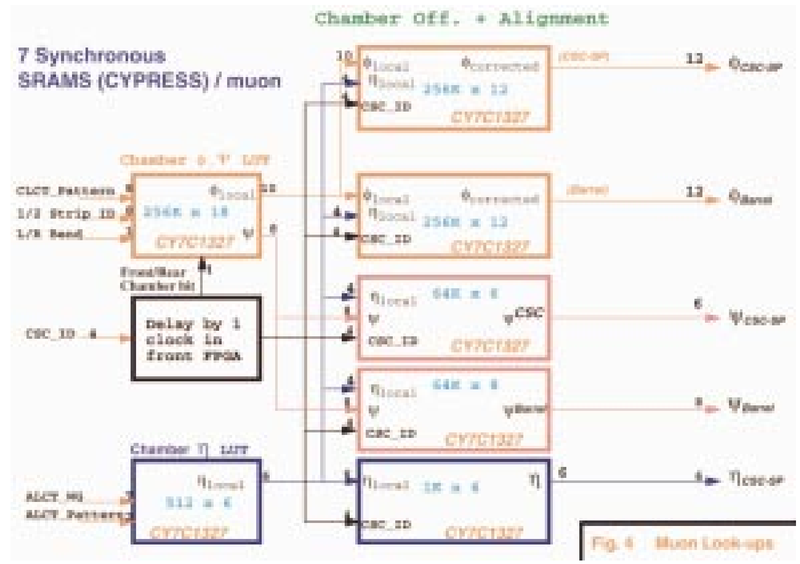
34 bits per CSC segment to Sector Processor

Sector Receiver Board Layout

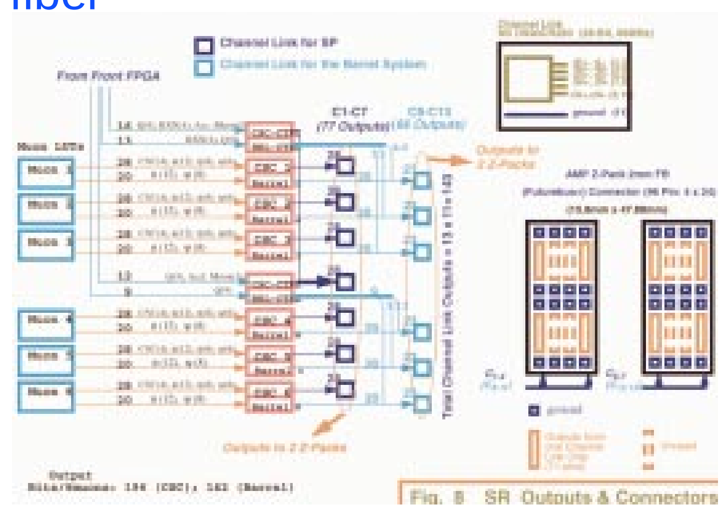
Optical Receivers

SRAM LUTs





optical fiber



Channel Link transmitters & connectors

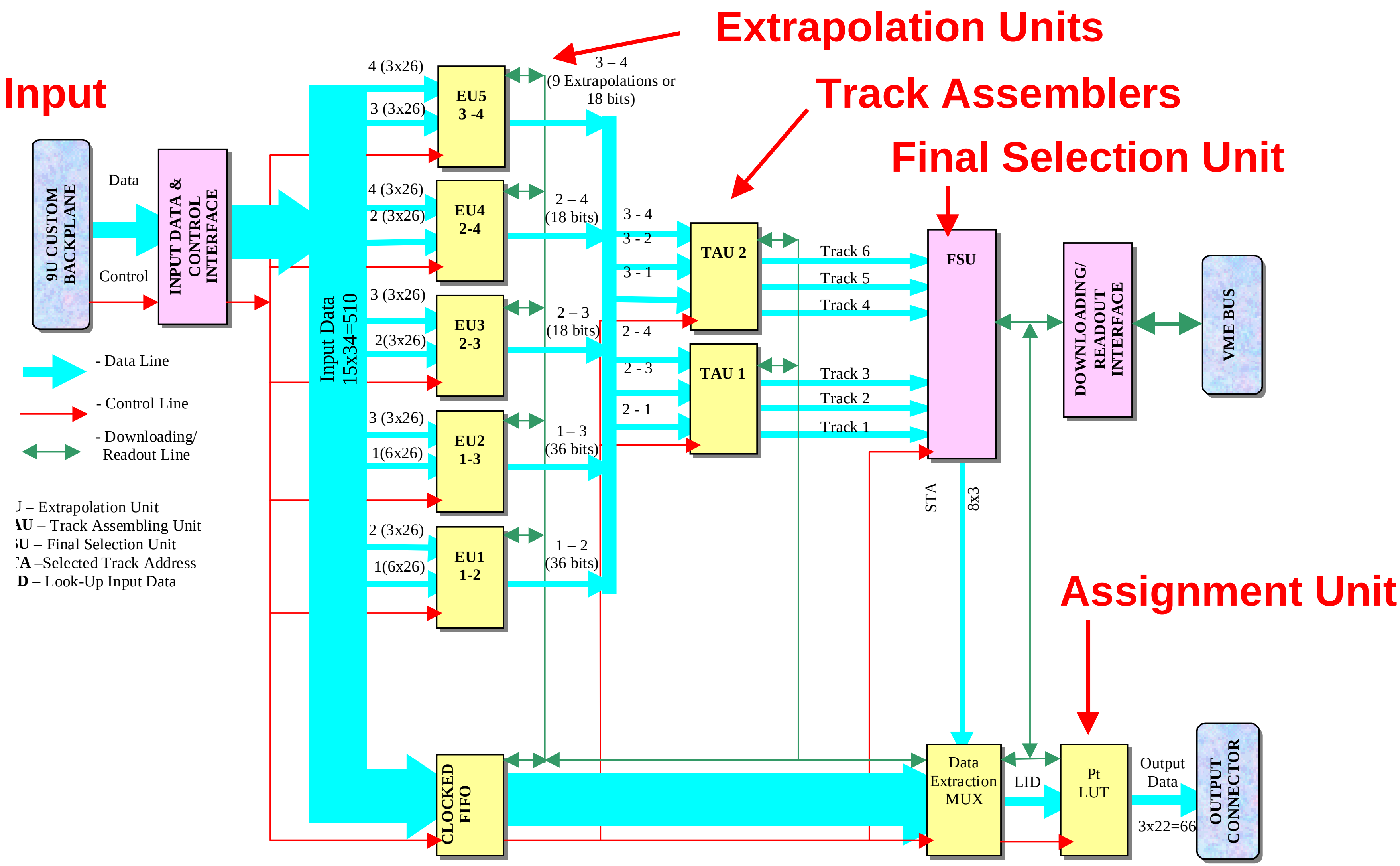
Sector Processor Functionality

Florida

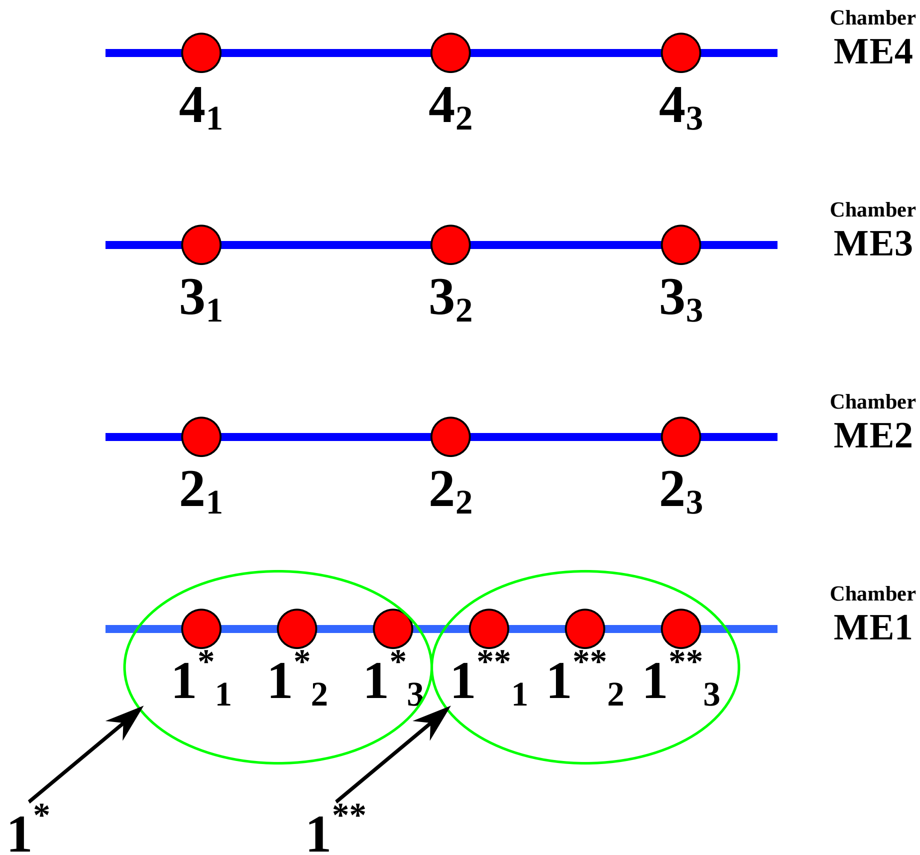
- Identify and measure muons from ~ 600 bits every 25ns (3 GB/s)
- Perform all possible station-to-station extrapolations in parallel

  $\Rightarrow$ Simultaneously search roads in φ and η
- Assemble 3- and 4-station tracks from 2-station extrapolations
- Cancel redundant short tracks if track is 3 or 4 stations in length
- Select the three best candidates
- Calculate P_T, φ, η and send to CSC muon sorter: 22 bits $\times$ 3 = 66 bits
- Functional block diagram developed $\Rightarrow$

Sector Processor Block Diagram



Sector Processor Logic



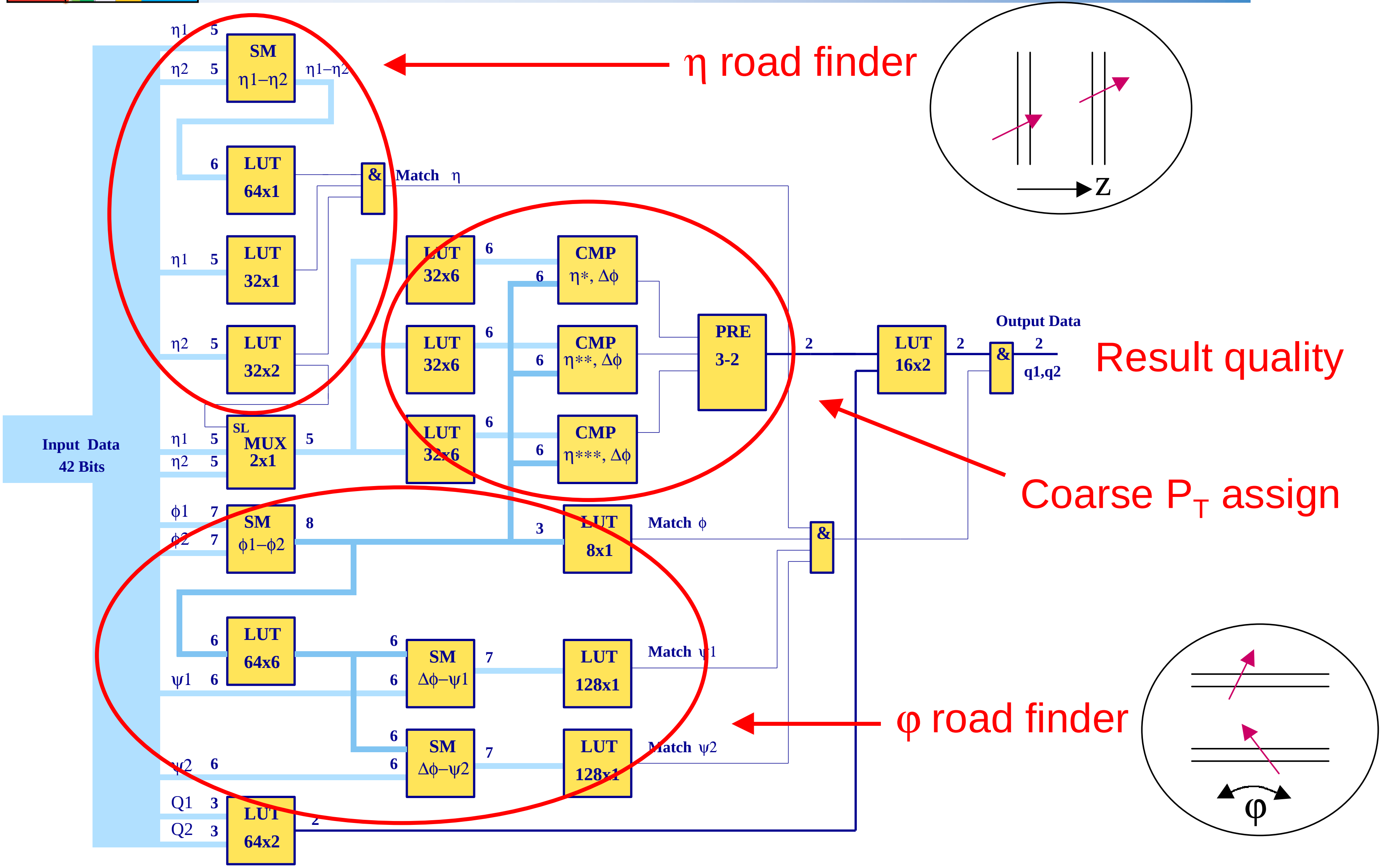
- **Perform all combinations of extrapolations in parallel:**

  $1_i \leftrightarrow 2_k$, $1_i \leftrightarrow 3_k$, $2_i \leftrightarrow 3_k$
  $2_i \leftrightarrow 4_k$, $3_i \leftrightarrow 4_k$

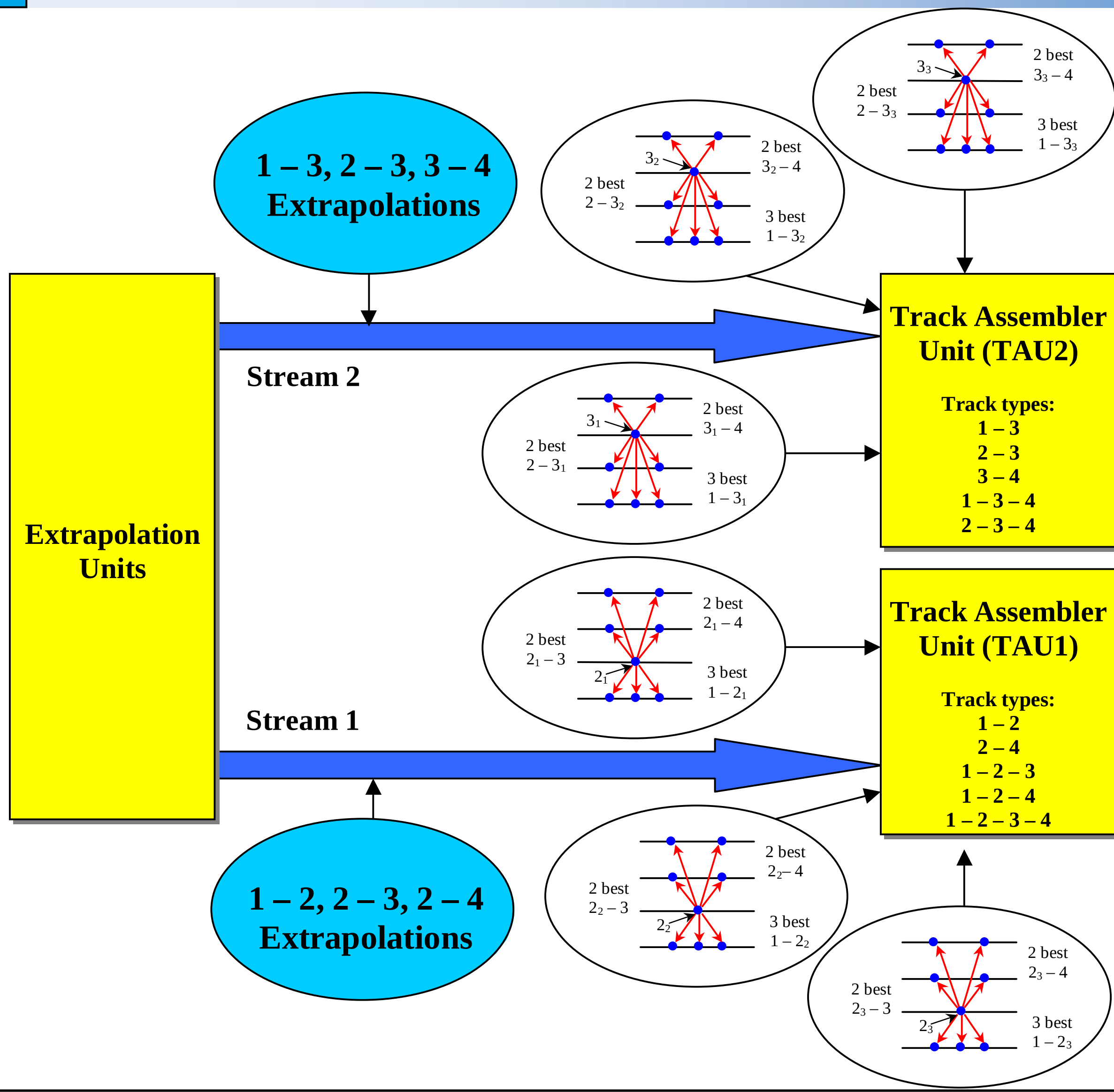
  But not $1_i \leftrightarrow 4_k$

- **Track Assembler takes best 2 or 3 extrapolations per reference segment**

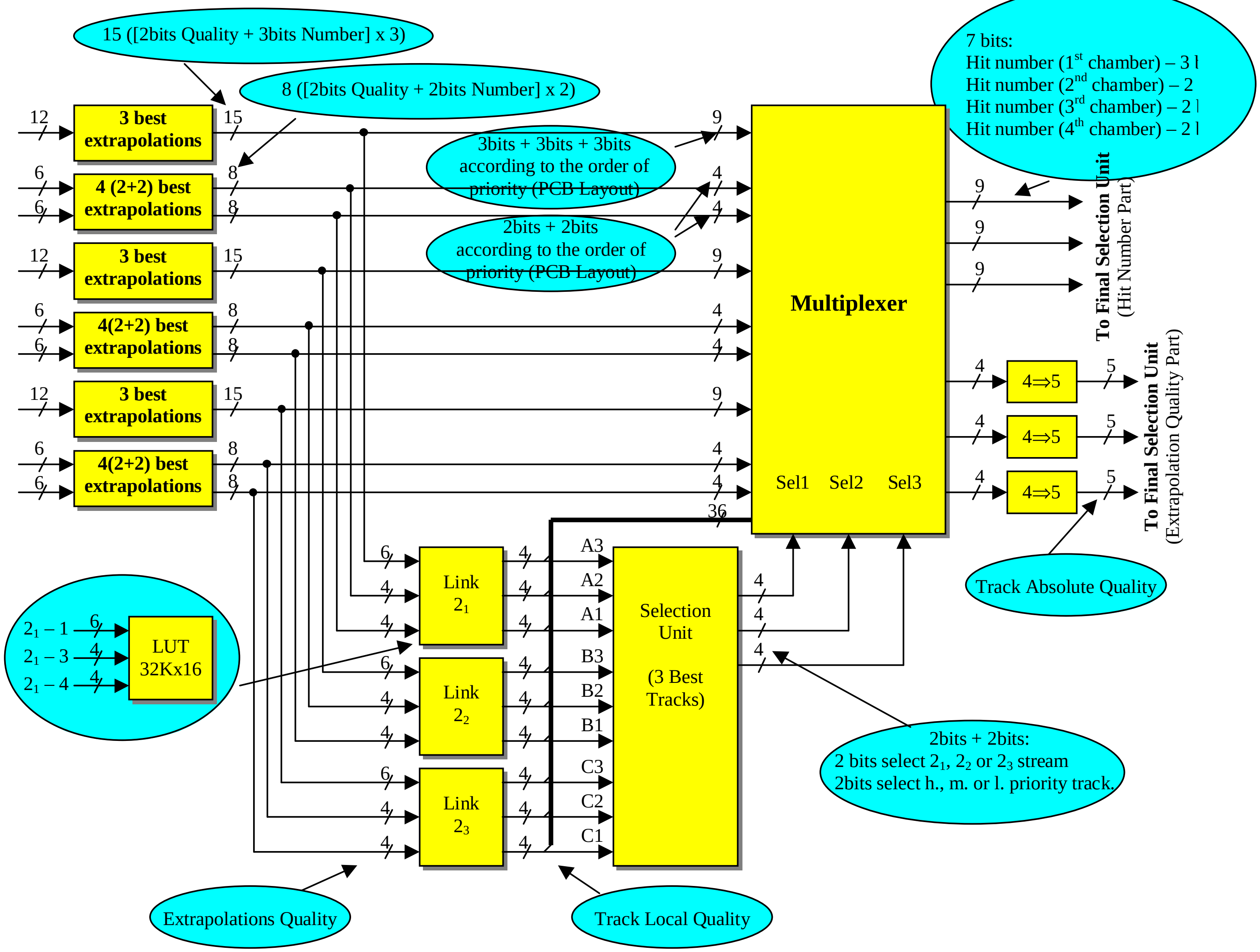
Extrapolation Unit Detail



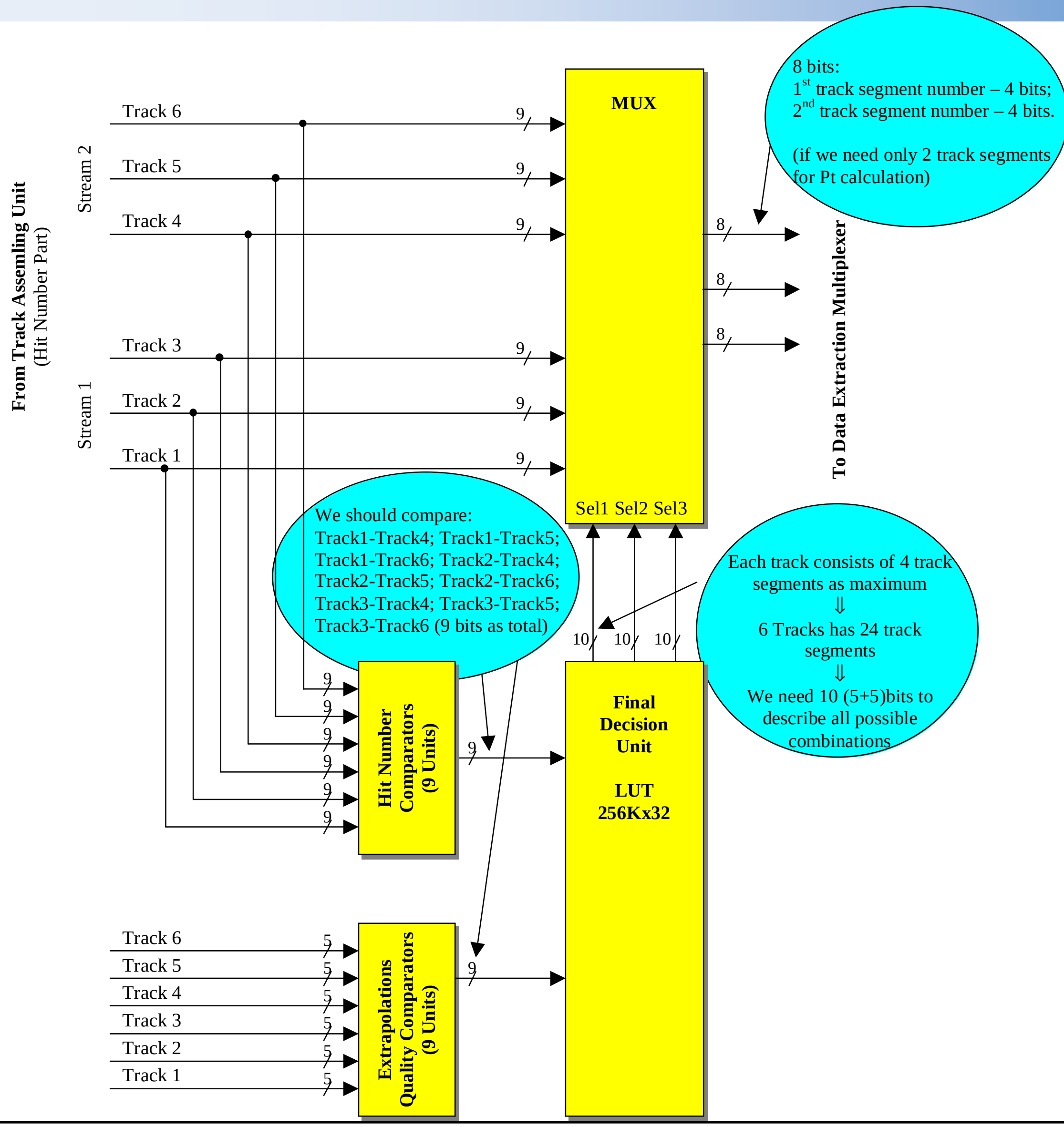
Data Stream Paths



Track Assembler Unit (TAU1)



Final Selection Unit

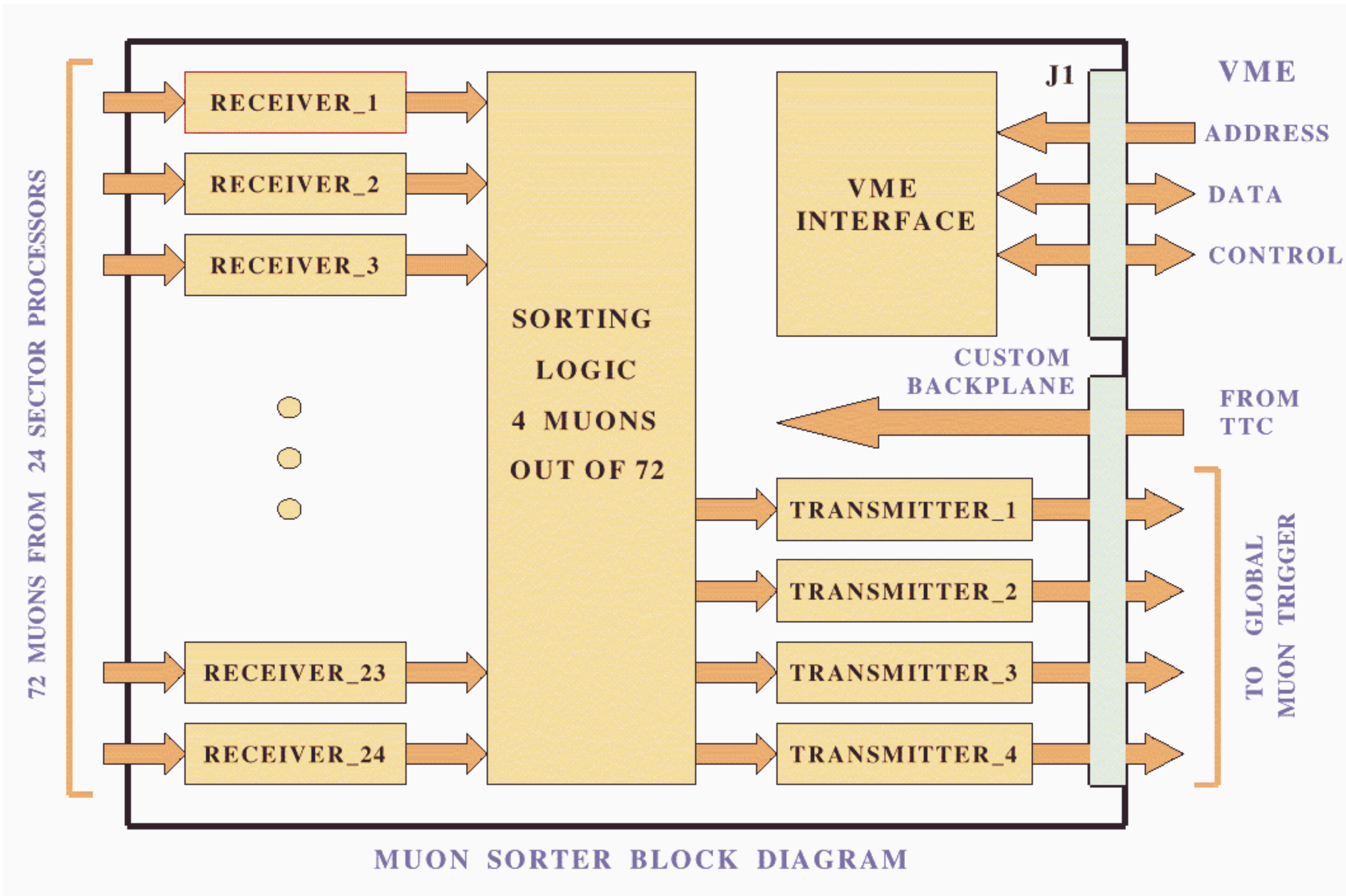


Muon Sorter Functionality

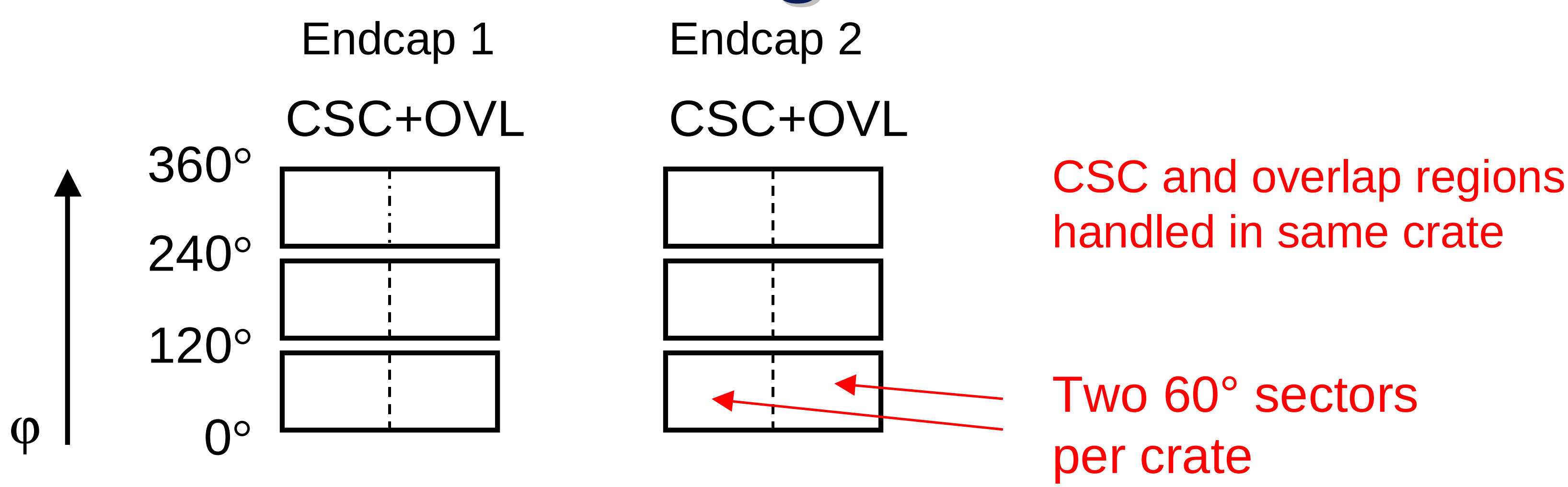
Rice

- The 3 highest rank muons from each Sector Processor are sent to the ***CSC muon sorter,*** which selects the 4 highest rank
- Total muon count:
  - ⇒ 3 muons × 6 sectors × 2 endcaps × 2 regions = 72 muons for CSC and OVL regions
- Sort is based on 7 bits (5 bits for P_T and 2 bits for quality)
  - ⇒ Basic sorting unit design (4 best out of 8) is complete
- Input: 72 × 22 bits = 1584 bits
- Output: 4 × 22 bits = 88 bits
  - ⇒ Sent to Global L1 Muon Trigger for association with RPC and DT triggers

Muon Sorter Block Diagram



CSC Track-Finder Crate Organization



CSC Counting House electronics:

Racks: 3 or 4

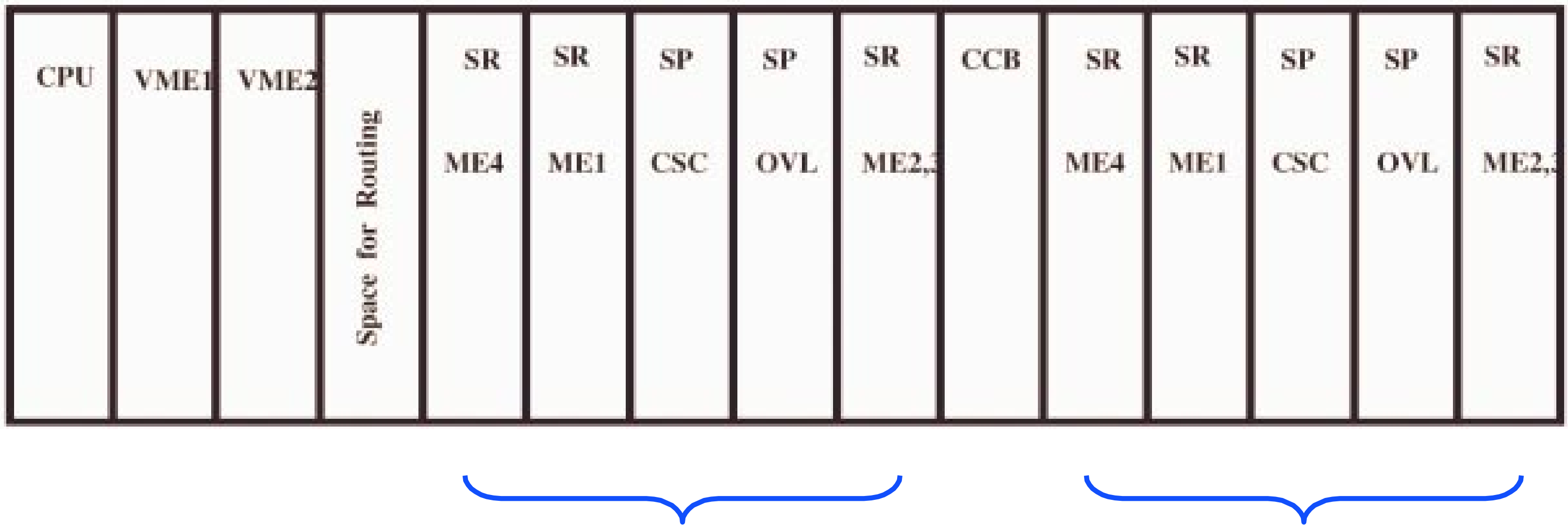
Crates: 6

Sector Receivers: 24

Sector Processors: 24

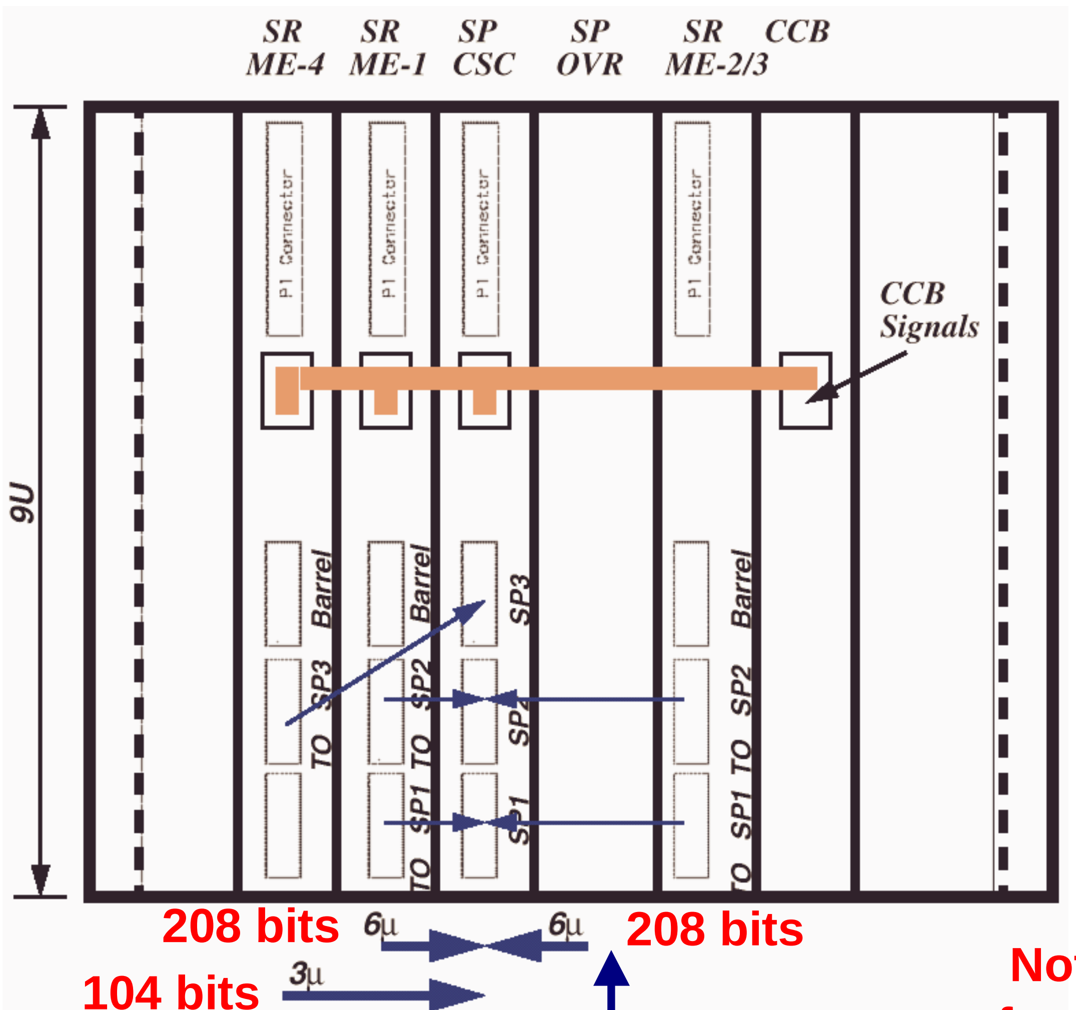
Muon Sorter: 1

Layout for Track-Finder Crate



Two 60° sectors housed in one 9U VME crate with custom backplane

Backplane Connections



- Channel Link custom backplane
- AMP Z-Pack 2mm connectors

Not shown: 204 bits (8 μ) from DT trigger to SP-OVR

Design Progress

- **Full conceptual design from trigger primitives to Global L1 Trigger**
  - ⇒ Bit counts fully documented
  - ⇒ Crate design underway
  - ⇒ Sector Receiver functionality defined
  - ⇒ Sector Processor algorithms defined
  - ⇒ Sort algorithms defined
- **Simulation of Track-Finder performance underway**
  - ⇒ resolution, efficiency, rate, chamber misalignment
- **Prototyping started**

Milestones / Schedule

√ **D387 – 1999 Mar, Sector Receiver Initial System Design (UCLA)**

√ **D331 – 1999 Mar, Sector Processor Initial System Design (Florida)**

D390 – 1999 Sep, Sector Receiver Prototype Design (UCLA)

D332 – 1999 Sep, Sector Processor Prototype Design (Florida)

on schedule

D391 – 2000 Jan, Sector Receiver Prototype (UCLA)

D334 – 2000 Jan, Sector Processor Prototype (Florida)

D335 – 2000 Apr, Sector Receiver / Processor Crate Test

Documentation

- **Sector Processor design and simulation:**
  - http://www.phys.ufl.edu/~acosta/cms/trigger.html

- **Sector Receiver design and overall CSC trigger bit document:**
  - http://www-collider.physics.ucla.edu/cms/trigger/