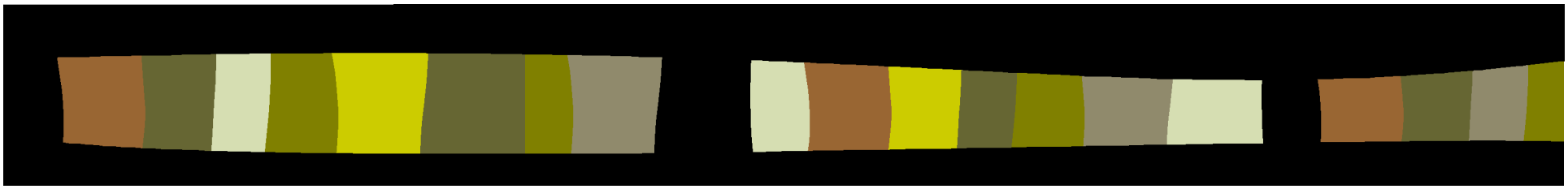
Status of the CSC Track-Finder



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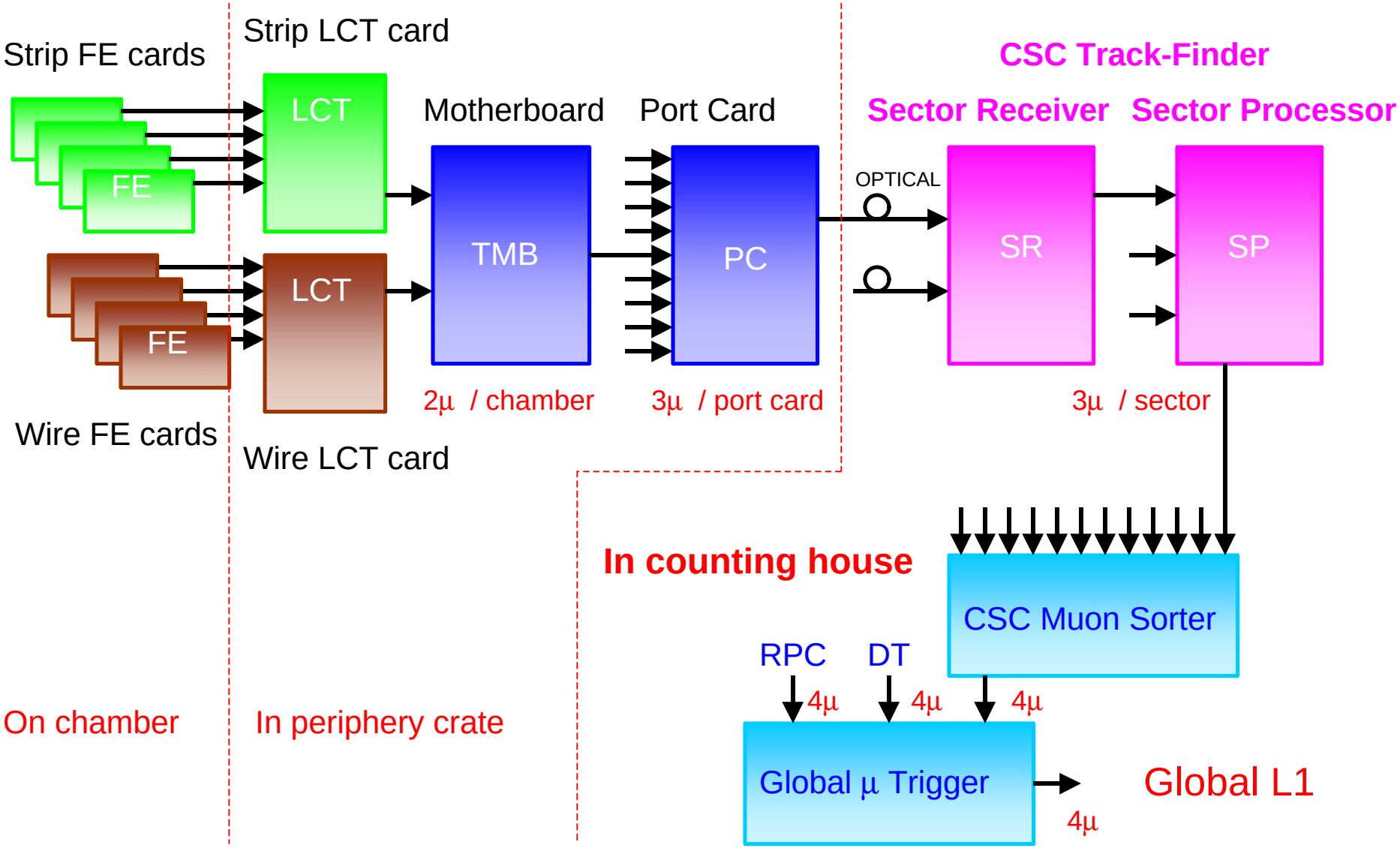
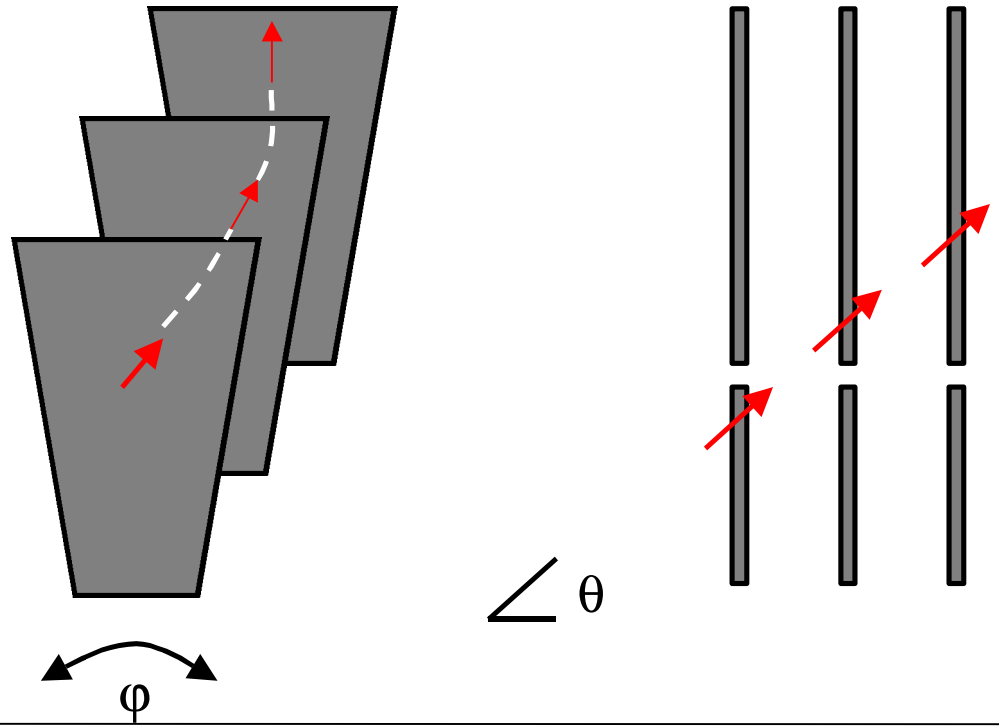
CSC Muon Trigger Scheme



Muon Track-Finding

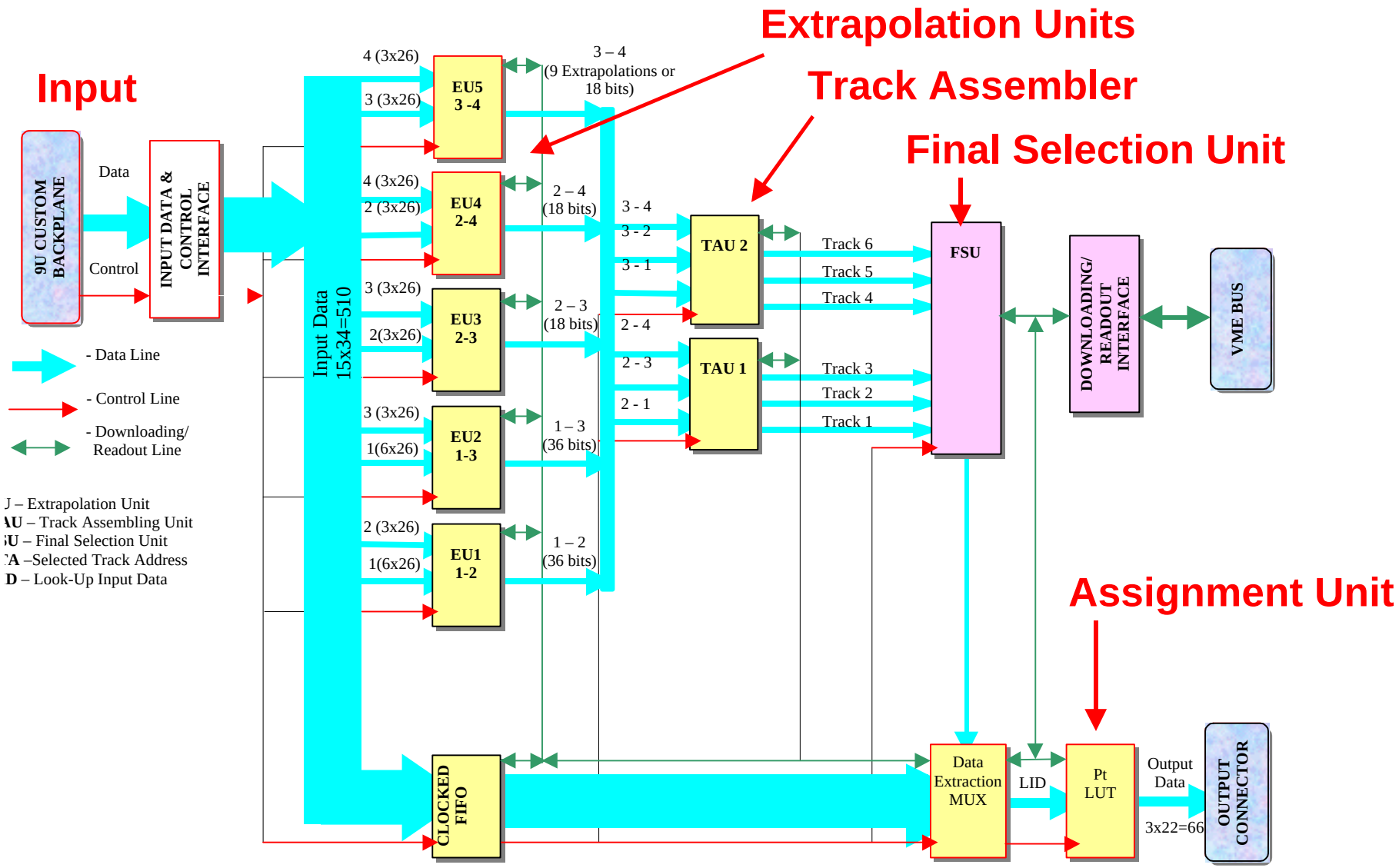
- Link trigger primitives into tracks
- Measure P_T, φ, and η
- Transmit highest P_T candidates to Global L1



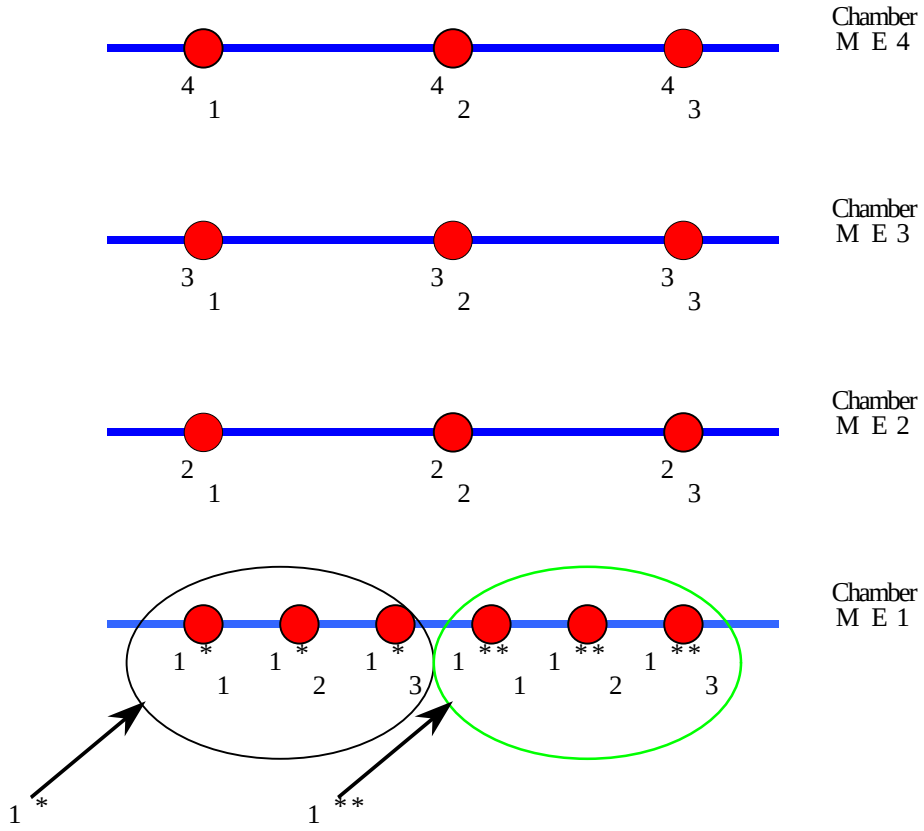
Design Status

- Nearly complete conceptual design presented late March at SR/SP review
- Primary concern is the design of the Track Assembler, the heart of the Track-Finder
  - Digests extrapolation results and must determine the quantity and quality of trigger muons
  - Scheme proposed, but must be validated with physics simulation
  - Must avoid ghost tracks for multi-muon trigger, yet maintain high efficiency for high P_T single muons

Sector Processor Block Diagram

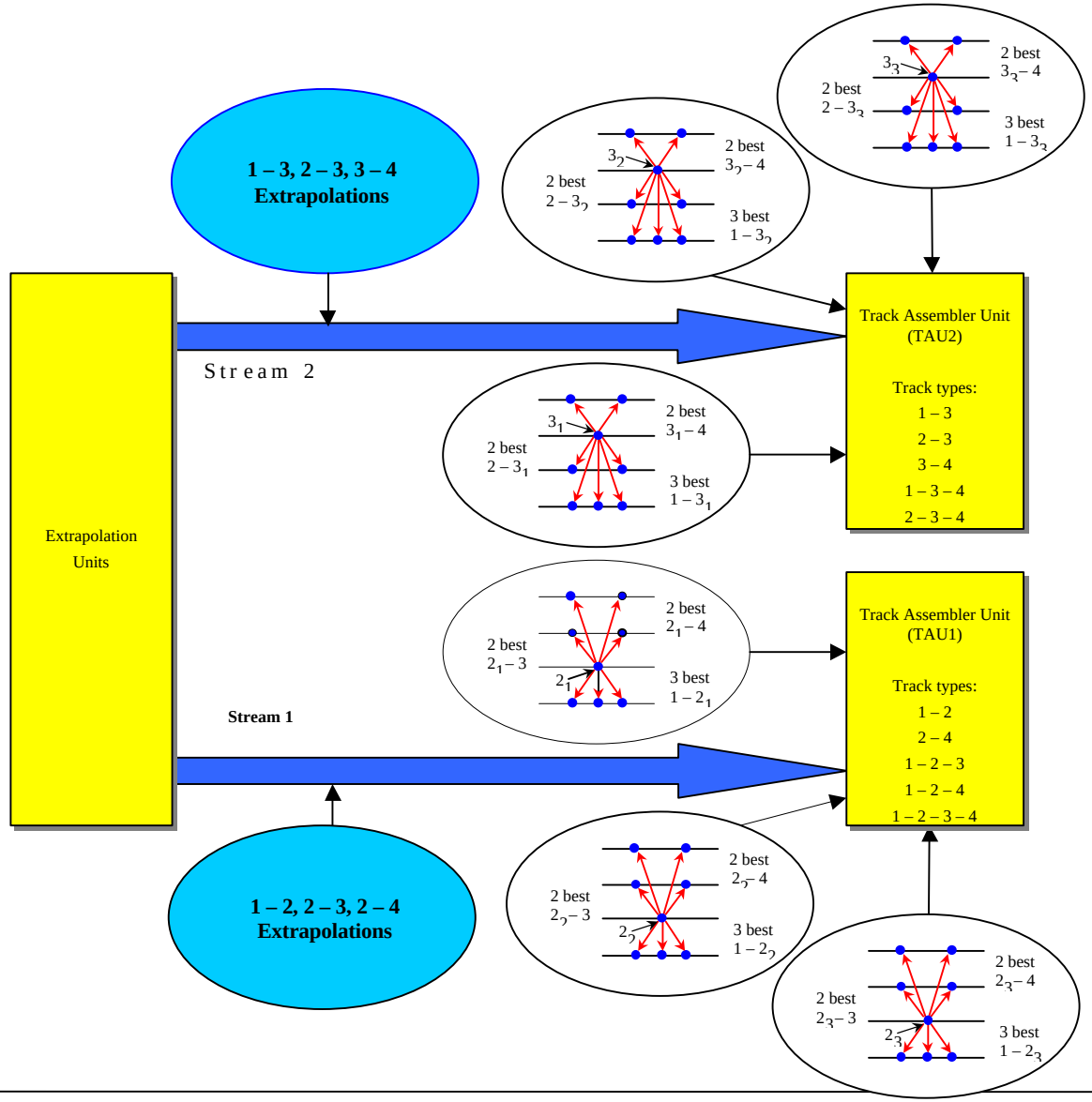


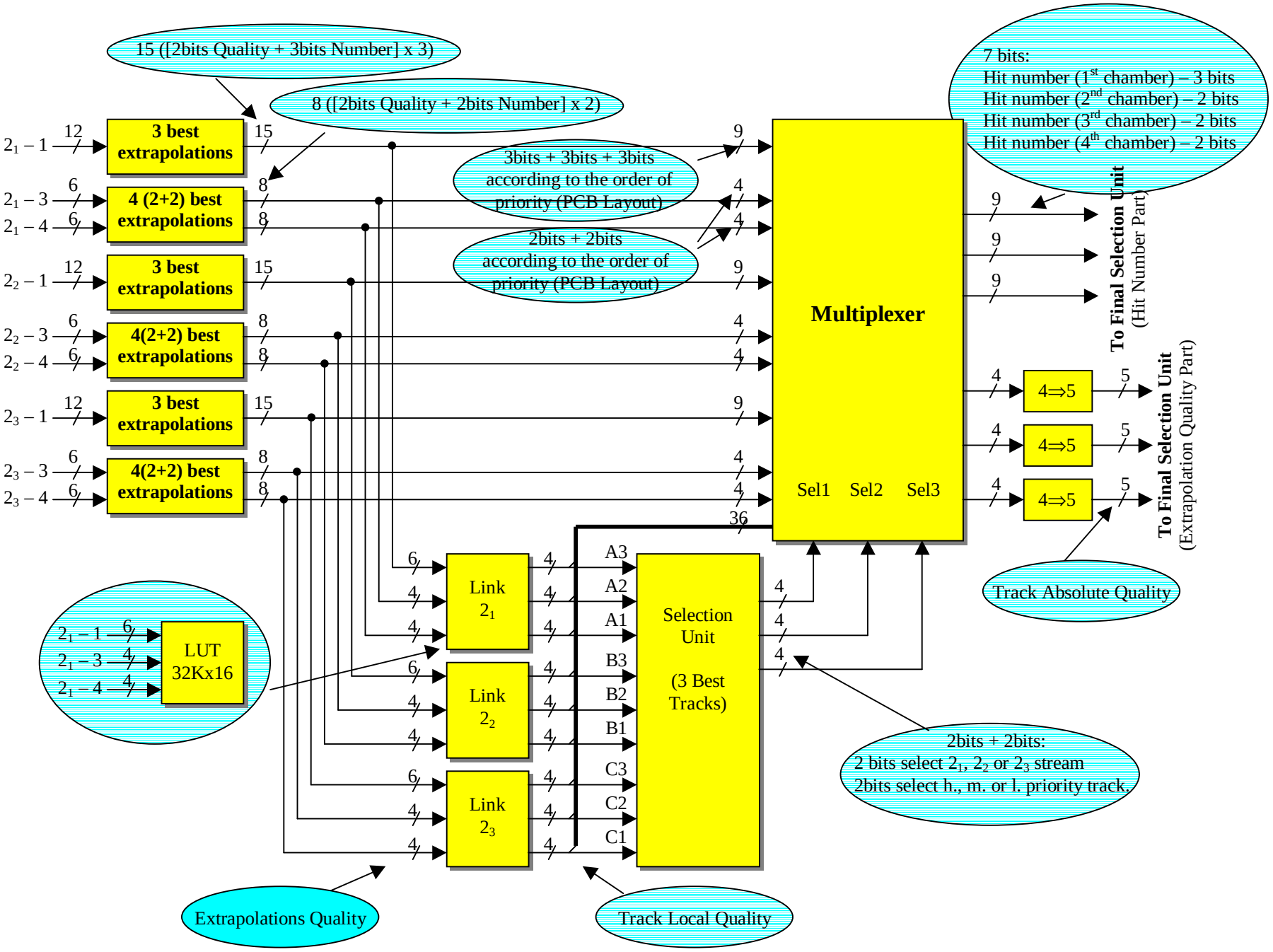
Sector Processor Logic



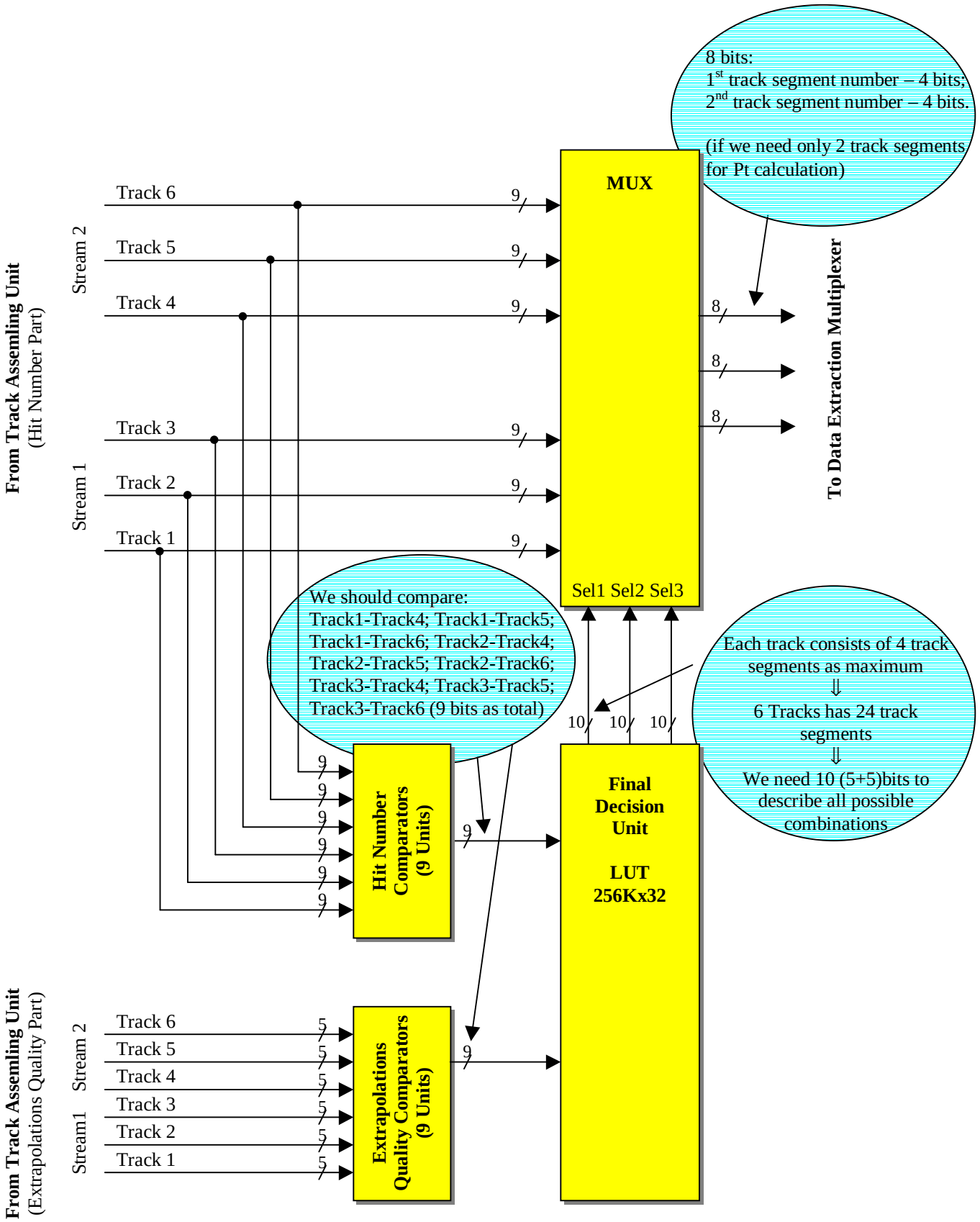
- Perform all combinations of extrapolations in parallel:
  - $1_i \leftrightarrow 2_k$, $1_i \leftrightarrow 3_k$, $2_i \leftrightarrow 3_k$, $2_i \leftrightarrow 4_k$
  - But not $1_i \leftrightarrow 4_k$
- Track Assembler takes best 2 or 3 extrapolations per reference segment

Data Stream Paths

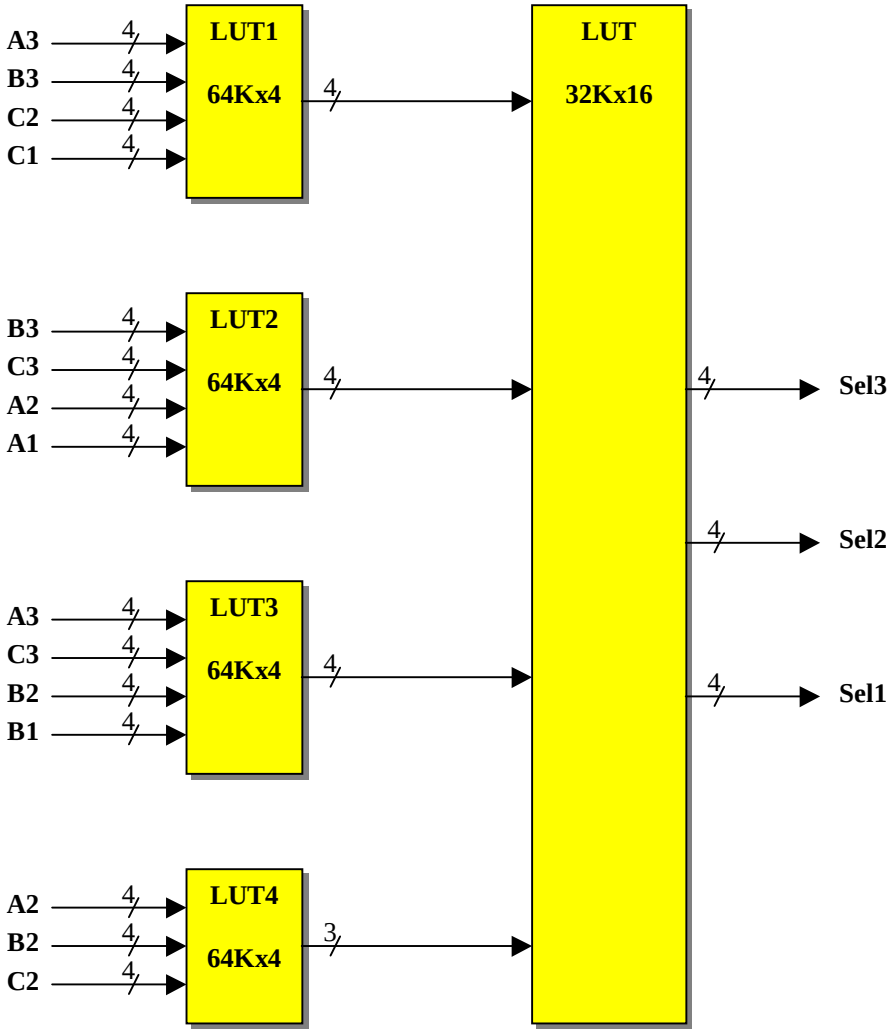




Track Assembler Unit (TAU1)



Final Selection Unit



A3 ≥ A2 ≥ A1 B3 ≥ B2 ≥ B1 C3 ≥ C2 ≥ C1

Selection Unit (TAU1,TAU2) hardware realization

Preparation for full SP review in July

- Finalize backplane and SR↔SP signals, including 4-station capability
- Determine connector space at backplane
- Estimate FPGA and RAM count
- Estimate board area (must fit on 9Ux400mm)
- Estimate cost
- Validate basic scheme with simulations