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# *General Track Finder Issues*

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*3/21/98*



## *Muon Track Finding*

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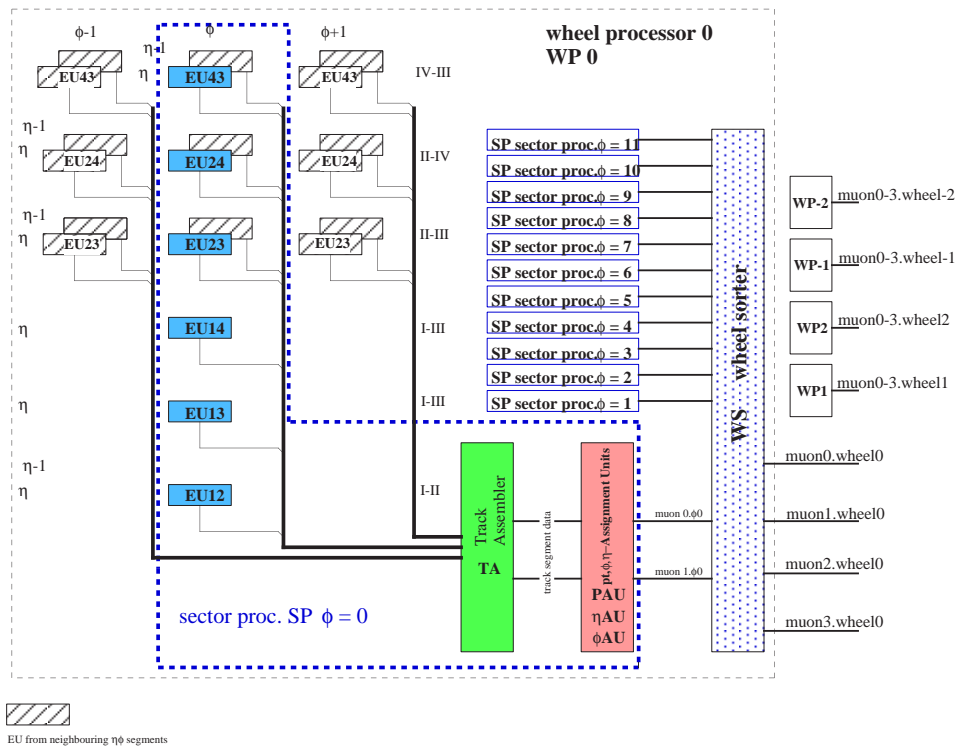
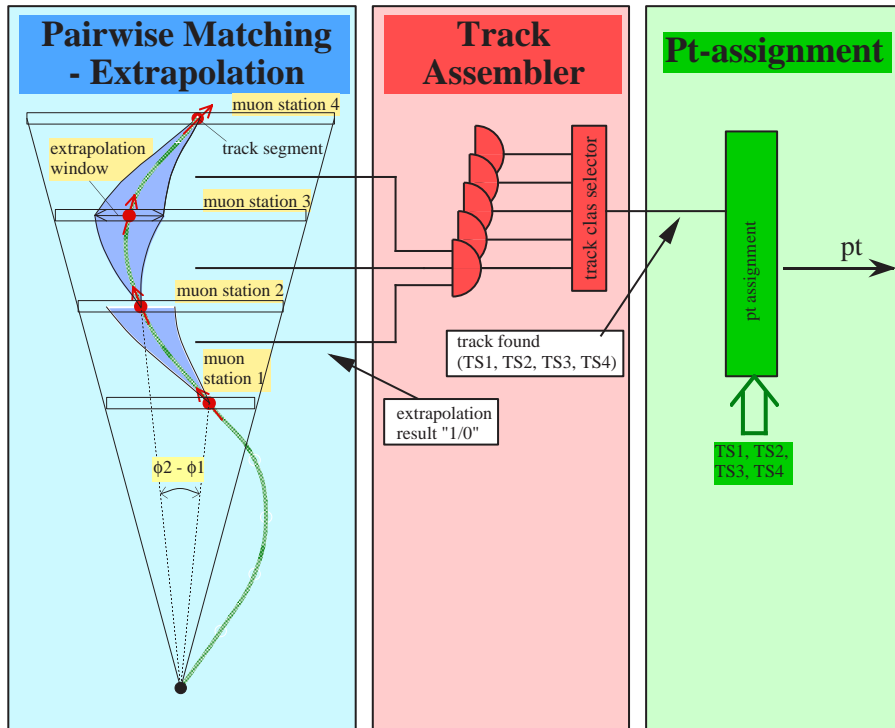
- Link trigger primitives into tracks
- Compute  $P_T$ ,  $\phi$ ,  $\eta$
- Send highest  $P_T$  candidates to Global L1 trigger
- Perform processing in  $\sim 14$  b.x. latency

### Barrel DT System:

- Trigger primitives from Bunch and Track Identifier (BTI) chip -- “mean timer chip”
  - $\phi$  and  $\eta$  measured at each station
  - angular acceptance  $< 45.7^\circ \Rightarrow |\eta| < 0.85$
- Magnetic bending independent of  $\eta$
- 2D linking of primitives in  $\phi$  only
  - station-to-station extrapolation, including neighboring sectors and wheels
  - select best track candidates
- Assign  $P_T$ ,  $\phi$ ,  $\eta$
- Send  $\leq 2$  tracks per sector to wheel sorter
- Prototype built by Vienna group



# Barrel Track Finder (Vienna)

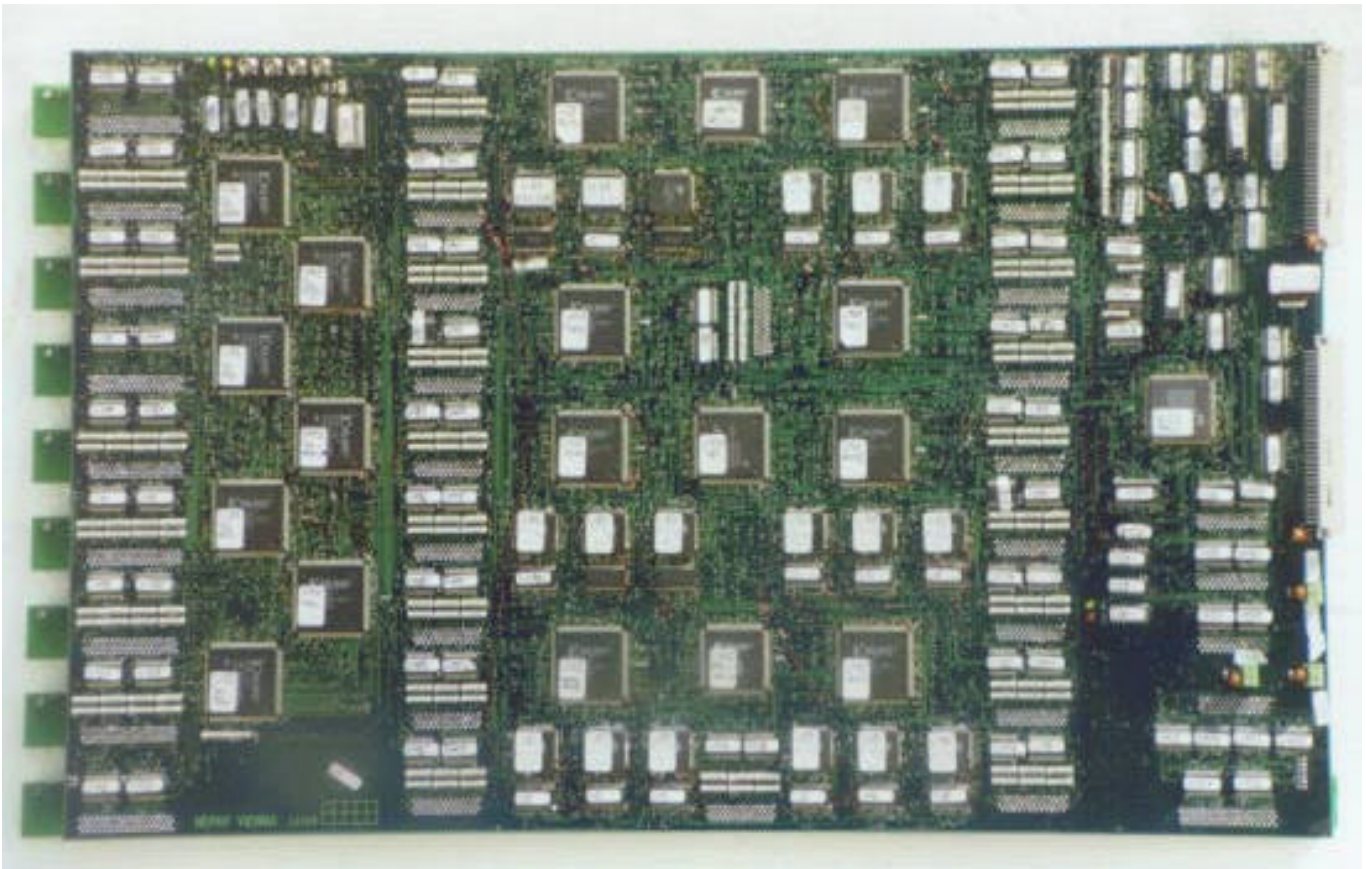


EU from neighbouring  $\eta_0$  segments



## *Barrel Track Finder Prototype*

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- Implemented in 19 Xilinx FPGAs and RAM
- I/O bottleneck  $\Rightarrow$  time multiplex I/O pins
- Runs at 20 MHz



# CSC Muon Trigger

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- Trigger primitives from front-end LCT chips
  - separate anode and cathode LCTs
- Trigger Motherboard (TMB)
  - correlates anode and cathode LCTs
  - sends  $\leq 2$  track stubs per xing from chamber
- Muon Port Card (MPC)
  - collects stubs from 9 chambers
    - ME1:  $30^\circ$  sectors
    - ME2:  $60^\circ$  sectors
  - sends  $\leq 3$  stubs to counting house via optical links

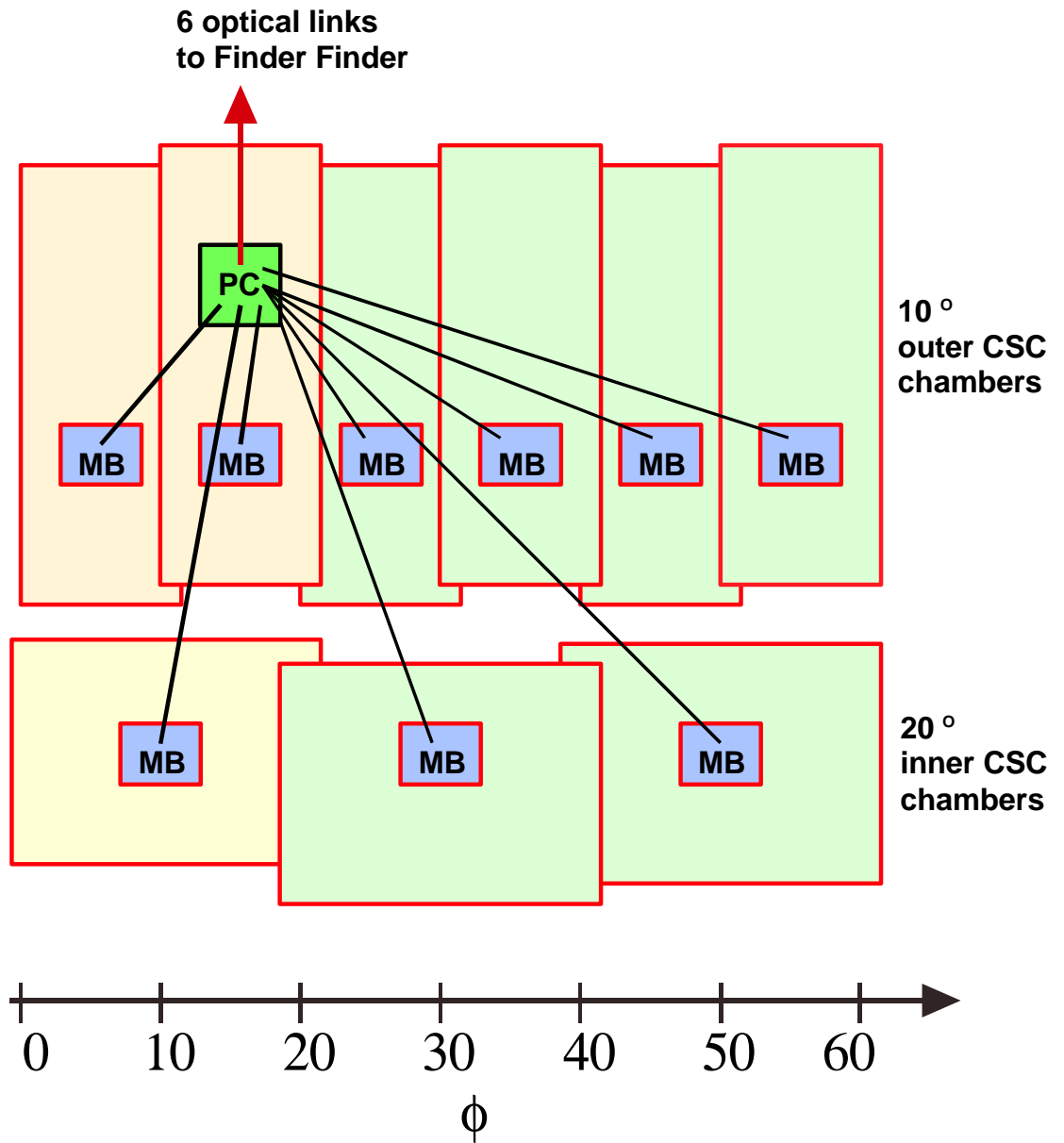
## Track Finder:

- Sector Receiver (SR)
  - receives optical signals
  - transmits signals to CSC-overlap SR via copper
  - reformats data (LCT bit pattern  $\rightarrow \phi, d\phi, \eta, d\eta$ )
  - sends data on VME bus to SP
- Sector Processor (SP)
  - form tracks from trigger primitives
  - assign  $P_T, \phi, \eta$
  - send  $\leq 2$  tracks per sector to wheel sorter



# Muon Port Card Layout

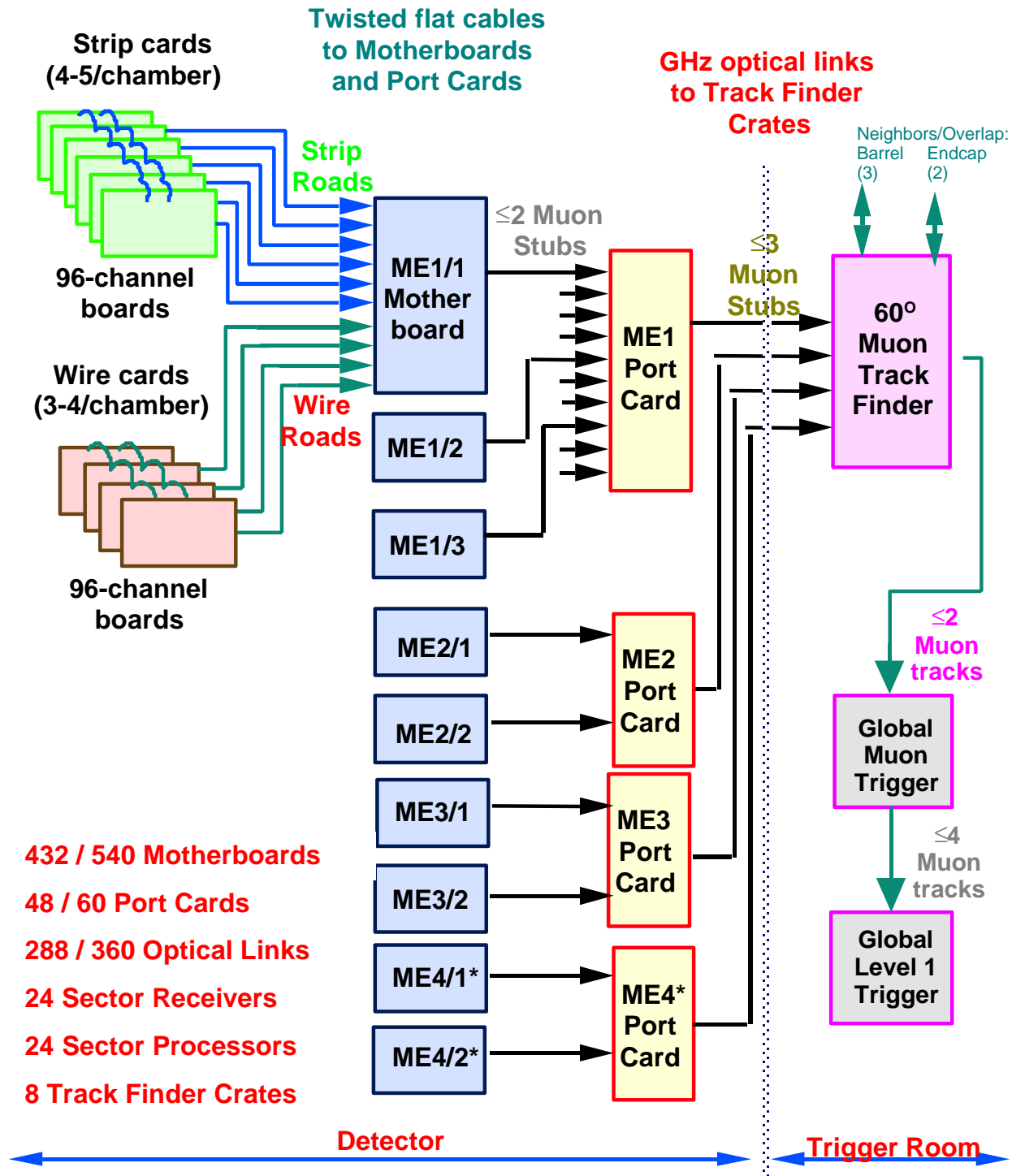
MB = MotherBoard  
PC = Port Card



60° sectors are a better match to barrel



# CSC Muon Trigger



- 432 / 540 Motherboards
- 48 / 60 Port Cards
- 288 / 360 Optical Links
- 24 Sector Receivers
- 24 Sector Processors
- 8 Track Finder Crates



## *Design Considerations*

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- Tracks crossing sector boundaries are not linked by sector processors
  - reduces data flow on VME backplane
  - $P_T > 10 \Rightarrow \Delta\phi_{12} < 2^\circ$
- Magnetic field is non-uniform in endcap
  - Extrapolation in  $\phi$  is more complicated
  - $P_T$  assignment depends on  $\eta$
- 2D or 3D track finding?
  - Track finding in  $\eta$ - $r$  to reduce combinatorics?
- Ghost suppression
  - Try all  $\eta$ ,  $\phi$  possibilities from chamber, or take best matches from MPC?
- Overlap region
  - Problem with ambiguity in  $\eta$
- What is sector occupancy from background?



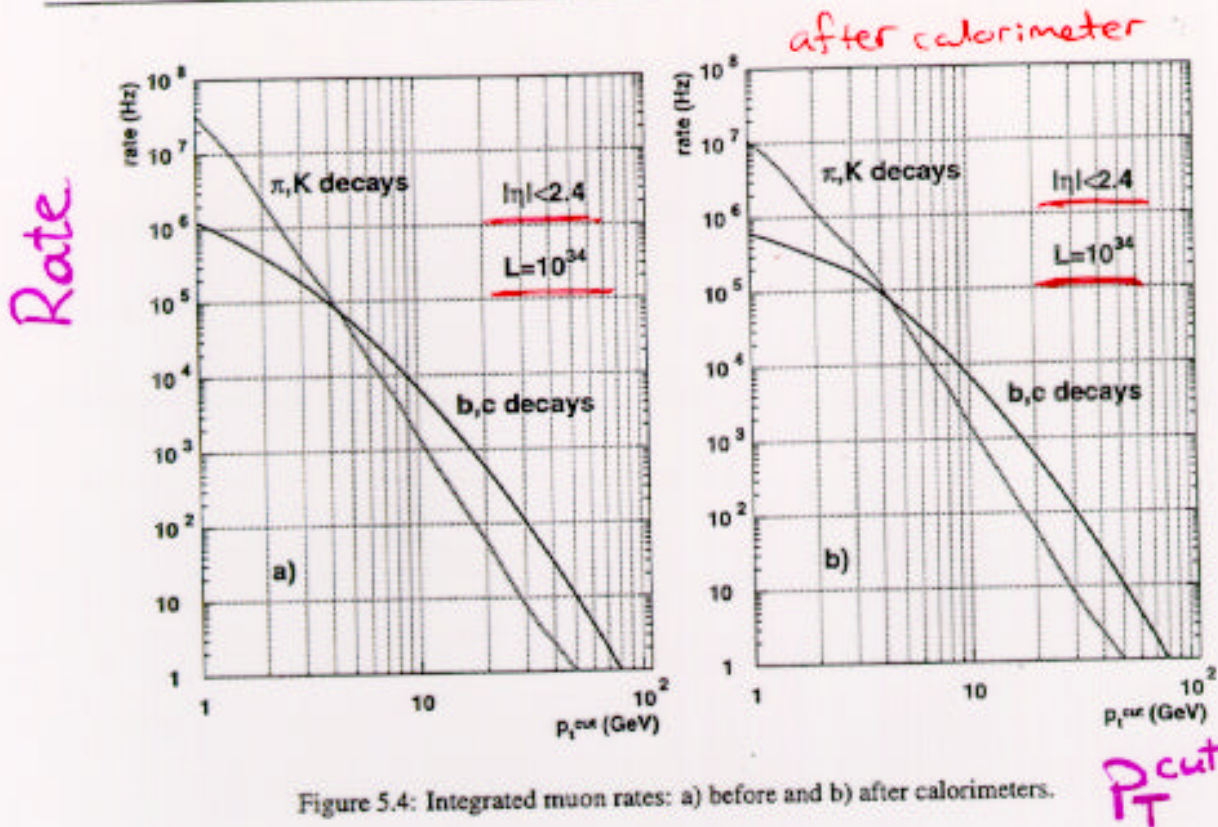


Figure 5.4: Integrated muon rates: a) before and b) after calorimeters.

PROMPT  $\mu$ 's :  $\frac{d^3 N_\mu}{d\eta dP_T dt} = a \cdot \exp\left[-\frac{(x-\mu)^2}{2\sigma^2}\right]$

$x = \log_{10} P_T$     $\mu = -0.725$     $a = 1.308 \cdot 10^6$     $\sigma = 0.433$

DECAY  $\mu$ 's :  $\frac{d^3 N_\mu}{d\eta dP_T dt} = A \cdot P_T^{-b}$

$A = 5.723 \cdot 10^7$     $b = 5.578$



# Real Muon Flux

- Prompt Muons +  $\pi/K$  decay Muons @  $10^{34}\text{cm}^{-2}\text{s}^{-1}$

$P_T$ Cut	Total Rate	Sector Rate	Sector Occupancy
1.0 GeV	1.0E7 Hz	170 kHz	0.43% 30° Sector $1.4 < \eta < 2.4$
2.5 GeV	1.2E6 Hz	56 kHz	0.14% 60° Sectors
5.0 GeV	8.7E4 Hz	4.2 kHz	0.01% $1.0 < \eta < 2.4$
10.0 GeV	8.0E3 Hz	0.4 kHz	0.001%

↑  
 $|\eta| < 2.4$

- Punch-through may approximately double rates
- Occupancy is fairly low
- Is rate of fake stubs from neutrons negligible?



## Design Possibilities

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- **Low occupancy**  $\Rightarrow$  Track finder is just a coincidence unit between all 3 stations
  - **But, still must calculate  $P_T$  accurately**
    - Total  $\mu$  rate is of order 100 kHz
    - Single  $\mu$  trigger rate  $< 6$  kHz
- **High occupancy**  $\Rightarrow$  Track Finder must employ 2D and maybe 3D track finding, resolve ghosts, and prioritize tracks
- **Track Finder should be flexible enough to handle everything in between**



## *Plans*

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- Start initial design of CSC sector processor for overlap region
  - Most difficult case because of ambiguity in extrapolation to DT system and because of the data flow from the CSC and DT systems
- Try to stay with FPGA technology to maintain programmability